1. As stated in Exhibit I, we use a ASIC chip from Microelectronics. The chip is designed with the clock settings listed below.

2. A pulse can contain more than one bit time. There are a total of 63 bits sent per packet. Three bits are latched with a total "ON" time of 976µS. Another bit has a "ON" time of 366µS. The other 59 bits have a "ON" time of 122µS.

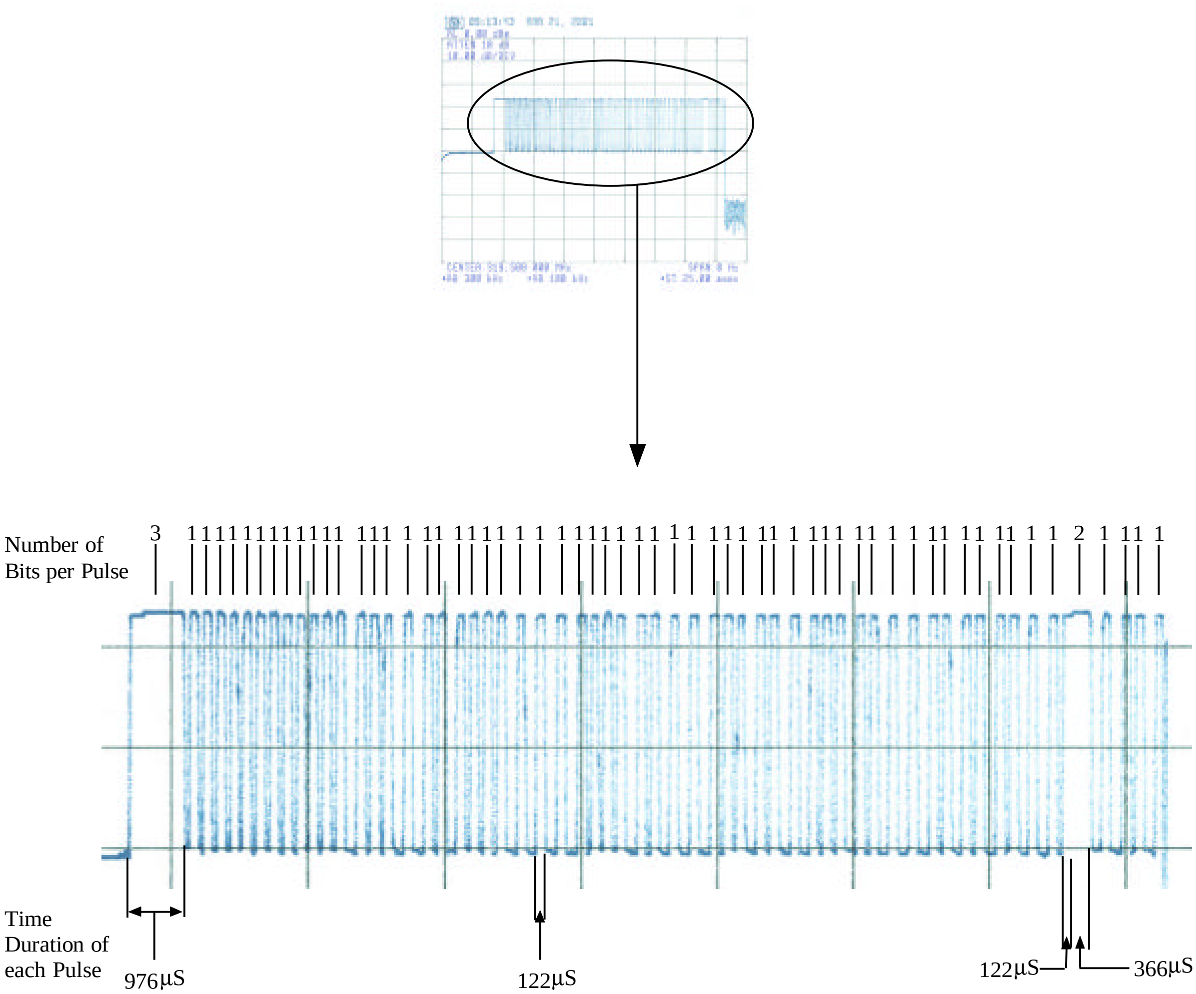
   The total "ON" time of a single packet is:

   $59 * 122\mu S + 366\mu S + 976\mu S = 8540\mu S$ or $8.54mS$

   Duty Cycle correction factor is:

   $20 * LOG(8.54 / 100) = -21.37$ dB

   The plot below, from page 11 in test report, illustrates this:



Number of Pulses = 60
Number of bits = 63

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3. If you have any questions E-Mail me at KenL_Nelson@Interlogixinc.com

Thank you,

Ken Nelson
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Interlogix Security & Life Safety Group

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