Vector-LP Radio Beacon Transmitter

Theory of Operation

VR125
VR250

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Vector-LP Radio Beacon Transmitter
TECHNICAL INSTRUCTION MANUAL

Section 6 THEORY OF OPERATION

6.1 INTRODUCTION
The theory of operation for the Vector-LP Radio Beacon transmitter is presented in this section. Frequent reference is made to electrical schematics (e.g., Figure SD-1). They are located in Section 9 of this manual. Circuits that are shown on electrical schematics, but not described in this section are either beyond the scope of this manual or are not used for NDB applications.

6.2 TRANSMITTER OVERVIEW
The transmitter operates at one fixed frequency in the LF/MF band (190 kHz to 535 kHz) or in the MF band (536 kHz to 1200 kHz and 1600 kHz to 1800 kHz). It provides up to 125 W (VR125) or 250 W (VR250) of continuous carrier power. It automatically transmits specific beacon identification signals at pre-selected repetition rates. Special codes may also be transmitted when commanded from an external source. Provision is made for local or remote operation of the transmitter as well as antenna fine-tuning through controls on the transmitter's front panel. If the standby option is purchased, provision is made for automatic changeover from the selected main side of the transmitter to the standby side when the selected main side's critical parameters are not met. The transmitter operates from a single phase, 47 Hz to 63 Hz ac power supply (170 V to 270 V ac for VR250; 90 V to 270 V for VR125), using switch mode power supplies. A 48 V dc input option (and 24 V dc for VR125 only) can also be purchased. Emission is continuous carrier (NON) beacon keyed identification tone (A2A) and beacon with voice (A2A/A3A).

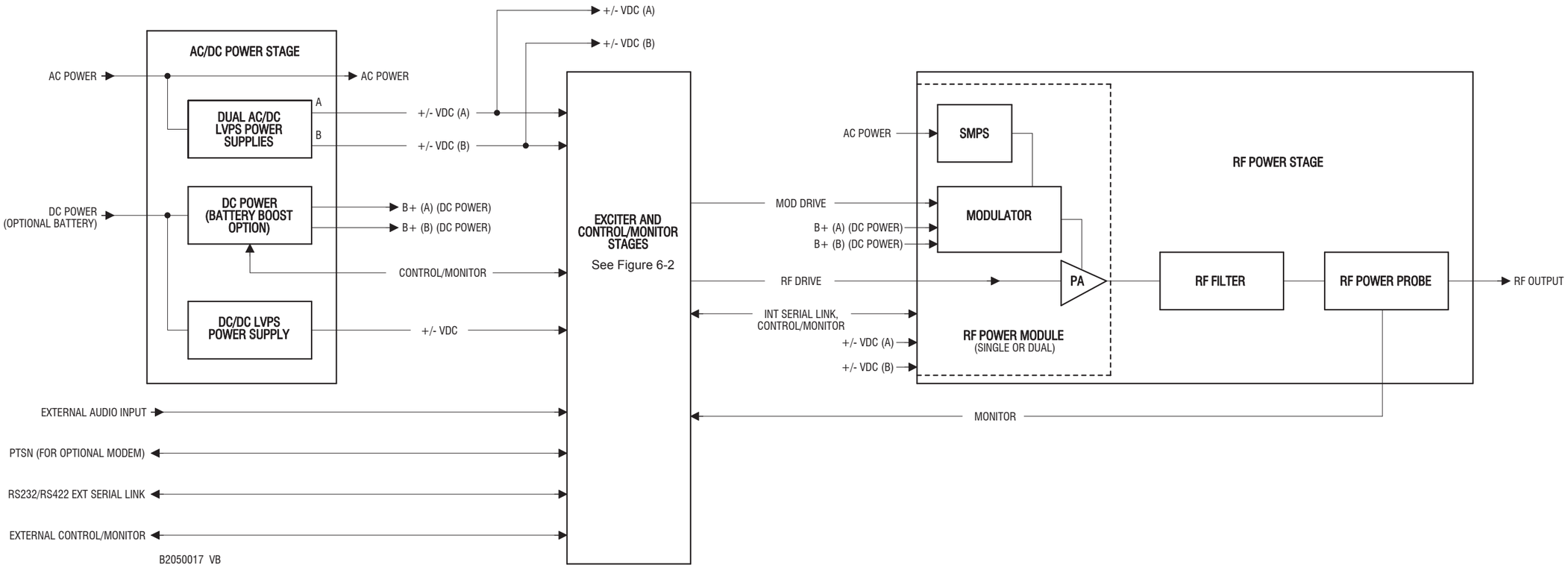
Local control/monitoring is done using front panel membrane switches and a graphic liquid crystal display. Critical parameters such as forward power, reflected power and antenna current can also be displayed on an analog meter on the front of the transmitter.

Remote control and monitoring can be provided over several optional interfaces. The transmitter also has provision to interface with a Nautel antenna tuning unit (ATU), using an isolated RS485 serial link. This ATU link allows the transmitter to regulate antenna current, and therefore maintain constant field strength, by auto-adjusting its output power in accordance with the ATUs antenna current sample.

The transmitter circuitry can be represented using four functional stages (see Figure 6-1):

- Ac-Dc Power Stage
- Exciter Stage
- Control/Monitor Stage
- RF Power Stage

6.3 AC-DC POWER STAGE
See Figures 6-1 and SD-1. The ac-dc power stage accepts the ac power source or optional dc power source and converts it to the necessary low level dc voltages required throughout the transmitter. The ac input voltage is also applied directly to the RF power stage. The ac-dc power stage's primary components are the ac-dc universal input power supplies (U2 and U3, if used) and the interface PWB (A11). If the dc input option is purchased, the transmitter also includes the dc-dc universal input power supply (U10) and the battery boost PWB (A16A1).



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Block Diagram – Vector-LP Radio Beacon Transmitter			
Issue 1.8	Not to Scale	Figure 6-1	Page 6-3 (6-4 Blank)

The ac input is applied through 10 A circuit breaker U5 and line filter U6. The ac voltage for the RF power stage (RF power modules A12 and A13) passes through thermistor RT1 and choke L1. Thermistor RT1 limits the inrush current to the RF power modules. Choke L1 improves the power factor on the ac lines applied to the RF power modules. The ac input is also applied to ac-dc universal power supplies U2 and U3 (U3 optional, for dual side transmitters), which convert the ac voltage to low level dc voltages. The ac input voltage is also applied to the interface PWB (A11) for sampling by the control/monitor stage.

Dc voltage is applied from an external 24 V or 48 V battery connected to A16TB1. The dc voltage is fused by F1 and applied to rectifier U8 and line filter U7 before being distributed to dc-dc universal power supply U10 and battery boost PWB A16A1. The battery boost PWB boosts the dc voltage and applies it to the RF power stage via rectifier U9.

6.3.1 Interface PWB

See Figures SD-1 and SD-21. The interface PWB (A11) provides an interface between the ac-dc power stage and the rest of the transmitter. It also contains voltage regulators (U1 and U2) that provide 9 V for the optional modem (via E5 and E6) and 24 V (limited to 1A) for the ATU (via E3 and E4). It also provides a dc sample of the ac input voltage to the control/display PWB as an aid in determining if the ac input source is at an acceptable level.

6.3.2 Ac/Dc Universal Input Power Supplies

See Figure SD-1. The ac/dc universal input power supplies [U2 (side A) and U3 (side B, if used)] are 110 W, universal ac input, multiple dc output power supplies. The transmitter's ac input is applied to U2 and U3 and the regulated 24.5 V, 15.6 V, 5.6 V and -15.5 V supplies are provided on the output. The outputs are applied through the interface PWB to the remaining functional blocks of the transmitter.

6.3.3 Battery Boost PWB (optional)

See Figures SD-1 and SD-25. The battery boost PWB is a boost type switching power supplies that provide a regulated B+ supply voltage to the transmitter when a 24 V or 48 V battery is acting as the power source.

A 24 V or 48 V supply is applied to the drain of switching FETs Q4 and Q5 through inductors L1 and L4. The gate of FETs Q4 and Q5 is driven with square wave pulses from pulse width modulation switching power supply controller U4 through push-pull buffer stage Q6/Q7. U4 is a fixed-frequency, pulse width modulation control circuit, incorporating the functions required for the control of a switching power supply. The device contains an internal sawtooth oscillator that is set to a nominal frequency of 100 kHz by external components R22 and C14. The output pulse width modulated control pulses to the gate of FETs Q4 and Q5 are generated by the comparison of this sawtooth waveform with a feed-back voltage sample from the output (CR6-cathode) and the bias voltage created from the in-circuit resistors selected by the *Battery Select 1* (J1-18) and *2* (J1-19) inputs.

The resultant variable pulse width, 100 kHz square wave at U4-8 (**E**) is applied to the gate of FETs Q4 and Q5 (through Q6/Q7) and turns it on and off with the appropriate pulses to maintain the desired set dc output voltage.

The *Battery Select 1* and *2* inputs, applied from the control/monitor stage, change the level of *Battery Boost (B+)* voltage based on the transmitter's power level. See Table 6-1 for the logic levels.

Table 6-1: Battery Select Logic

B+ Voltage		Battery Select 1	Battery Select 2
VR250	VR125		
79 V	55 V	0	0
136 V	97 V	0	1
236 V	167 V	1	1
Invalid	Invalid	1	0

6.4 EXCITER STAGE

See Figures 6-2 and SD-2. In dual configuration the exciter stage contains two independent exciter sections (A and B) which can be supplied in a single or a main/standby configuration. In a main/standby configuration, the exciter can be selected automatically or manually by local or remote control. Each exciter section consists of an RF synthesizer PWB, interphase PDM driver PWB and exciter monitor/generator PWB.

6.4.1 Exciter Interface PWB

See Figures SD-9 and SD-10.The exciter interface PWB (A2) provides signal distribution, as well as the interconnection for all the PWBs and assemblies in the exciter control/monitor stage. The RF drive failure detection, changeover/shutdown and monitor fail logic circuits are located on the exciter interface PWB.

6.4.1.1 RF Drive Circuitry and Failure Detection

U3:A, U3:B, U2:A, U2:B, and U2C and their associated components drive the RF signal to the RF power blocks for side A. Q9 and its associated components provide a low when the RF drive is present and a high when it is not present.

U3:C, U3:D, U1:A, U1:B, and U1C and their associated components drive the RF signal to the power blocks for side B. Q8 and its associated components provide a low when the RF drive is present and a high when it is not present.

6.4.1.2 Changeover/Shutdown

U4, Q1 through Q7, K1 and K2 along with their associated components allows for the selection of the main side of the transmitter. If the NDB A/$\overline{B}$ input is held low, the main side will be B, otherwise it will be A. If no changeover or shutdown is indicated (U4 inputs 3, 4, 6, and 7 are all high level), the relay for the main side will be energized, closing the contact and providing voltages to the main PDM driver and RF synthesizer. The relay for the standby side will be open. The RF relay control FET (Q5) selects the main position for RF relay K1. If a changeover is indicated by a low on either U4:3 or U4:4, the relay for the main side will open and the relay for the standby side will close. The RF relay control FET (Q5), will select the standby position for RF relay K1. U4:17, U4:21, U4:22, and U4:15 drive transistors Q1 through Q4 to indicate to the control board information about the active side of the transmitter and the changeover/ shutdown state. If a shutdown is indicated, both K2 and K1 are opened so that neither PDM driver or RF synthesizer has power.

6.4.2 RF Synthesizer PWBs

See Figures SD-16 and SD-17. The RF synthesizer PWBs (A5 and, if installed, A8) use direct digital synthesis (DDS) to generate carrier frequencies within the LF/MF broadcast band (190 kHz to 1800 kHz). The output of a digital synthesizer integrated circuit with internal high-speed 12-bit digital-to-analog converter is low-pass filtered to provide a sinusoidal continuous output. The sine wave is digitized and divided by a factor of four to obtain the carrier frequency. The digitized sine wave is also divided by a factor of N to obtain a $2f_{PDM}$ frequency that ultimately determines the transmitter's pulse duration modulation (PDM) frequency. The RF synthesizer PWB consists of a microprocessor, direct digital synthesizer, low pass filter, digitizer, IPM correction, balanced drive, and N divider.

6.4.2.1 MICROPROCESSOR

The microprocessor consists of an 87C51 integrated circuit (U4), which is clocked at the system oscillator frequency (10.0000 MHz). Firmware resides in U4's internal four kilobytes of EPROM memory. The microprocessor generates control information for the DDS circuit and generates control information for the N divider circuit.

6.4.2.1.1 DDS Control Information

The RF carrier frequency is set using five binary coded decimal (BCD) switches (S1 through S5). When a current-sink-to-ground is applied at the *Reset DDS* input, or during turn on, the *microprocessor* monitors these switches and outputs the appropriate 48-bit value to the DDS Frequency Tuning Word #1 register. The 48-bit value is written in six consecutive bytes to the DDS's six internal registers. The *sclk* signal is enabled on each write cycle.

6.4.2.1.2 N Divider Control Information

The $4f_C/B$ frequency is divided by an 'N' factor to provide $2f_{PDM}$ output frequency between 126 kHz and 134 kHz (when E3 is set in **LOW PDM** mode) or between 245 kHz and 276 kHz (when E3 is set in **HIGH PDM** mode) (see formula below). The microprocessor determines the value of N and outputs the information at pins 2, 3, 4, 5, 6 and 7. The N divider circuit uses this information as the N dividing factor.

- for f_{PDM} = 130 kHz (*HIGH PDM *position):

f_C and f_{PDM} are expressed in kHz

$$2f_{PDM} = \frac{4f_C}{\text{int}\left[\frac{2f_C + 65}{130}\right]}$$

6.4.2.2 DIRECT DIGITAL SYNTHESIZER

The direct digital synthesizer consists of integrated circuit U5 (AD98525Q) and associated components. It generates a frequency of $4f_C$ based on information provided by microprocessor U4 (refer to paragraph 6.5.2.1). Integrated circuit U5 is a CMOS, numerically controlled oscillator with a 48-bit phase accumulator and 12-bit digital-to-analog converter (DAC). The phase accumulator, which is responsible for generating an output frequency, is presented with a 48-bit value from the Frequency Tuning Word 1 registers, whose contents determine the FTW as follows:

$$FTW = \frac{(DesiredOutputFrequency x 2^{48})}{SYSCLK}$$

The 10 MHz clock input is coupled with U5's internal programmable reference clock multiplier. This results in a system clock of 50 MHz (i.e., SYSCLK = 50 MHz).

The 12-bit output from the phase accumulator is input to the DAC, which outputs a stepped sine wave at $4fc$. The $4fc$ output is then low-pass filtered to remove high frequency components.

6.4.2.3 LOW PASS FILTER

A low-pass filter consisting of C21, L1, and C23 removes the high frequency images present in the DDS output signal. The output is a sine wave at a frequency of $4f_C$.

6.4.2.4 DIGITIZER

The output of the low-pass filter is connected to a digitizer circuit consisting of transistor Q4, inverter U10:B, and associated components. Inverter U10:B outputs an approximate square wave at a frequency of $4f_C$, which is applied to a ÷4 circuit and to the N divider circuit.

6.4.2.5 IPM CORRECTION

Not applicable to Vector transmitters.

6.4.2.6 WAVEFORM SYMMETRY

RF DRIVE SYMMETRY potentiometer R32 is adjusted for an RF drive output waveform, which is a symmetrical square wave (50% duty cycle). The position of **SYMMETRY ADJ** shorting jumper E6 determines when the RF drive symmetry circuit is enabled or disabled. E6 should be installed in the **ENABLE** position (shorting pins 1 and 2) when used in a Vector transmitter.

6.4.2.7 BALANCED DRIVE

The balanced drive buffer is a switching circuit that ensures the rise and fall times of its output square wave are minimal. The f_C signal is a 15 V peak-to-peak square wave that is the low level RF drive signal for the RF power stage of the transmitter.

6.4.2.7.1 Balanced Drive Matching

Different values are possible on the balanced drive output, depending on the transmitter's requirements. The position of shorting shunt post E5 on 7-position header XE5 can be changed to choose between different capacitor and resistor values. E5 is factory installed in the **D** position (shorting pins 7 and 8) for Vector transmitters.

6.4.2.8 N DIVIDER

The N divider circuit is a cascade counter made up of U6, U7, and inverters U8:A and U8:F. The $4f_C/B$ signal is divided by N to provide a $2f_{PDM}$ frequency, which is between 126 kHz and 134 kHz (when E3 is set in **LOW PDM** mode) or between 245 kHz and 276 kHz (when E3 is set in **HIGH PDM** mode). The value of N is supplied by microprocessor U4 (see 6.5.2.1.2). The $2f_{PDM}$ output, which is nominal 5 V pk-to-pk pulses, is applied to the transmitter's PDM generation circuit, and ultimately determines the PDM frequency.

6.4.2.9 RF DRIVE SOURCE SELECTION

The RF drive (fc) source is provided by the integral numerically controlled oscillator or an external RF generator. The position of shorting shunt posts E1, E2 and E4 determine which source is selected. Vector transmitters use the internal source.

6.4.2.9.1 Internal fc Source

To use the integral numerically controlled oscillator's output as the RF drive source, set the shorting shunt posts as follows:

- E1 in **INT** position (pins 2 and 3 shorted)
- E2 in **INT** position (pins 2 and 3 shorted)
- E4 in **INT** position (pins 2 and 3 shorted)

6.4.3 Interphase PDM Driver PWBs

See Figure SD-18. The interphase PDM driver PWBs (A6 and, if installed, A9) produce a pulse train of variable width as their PDM output. The PDM repetition rate (f_{PDM}) is a fixed frequency normally between 130 kHz and 133 kHz. The frequency is determined by the $2f_{PDM}$ input, which is produced by the active exciter monitor/generator PWB. The PDM drive signal, which determines the transmitter output power level, is applied to the modulator assemblies in RF power modules A or B (see Figure SD-22).

6.4.3.1 CARRIER LEVEL CONTROL

The carrier level control circuit consists of U6, U7, U2A, U2D, U3B, U3D, U13A and their associated components. U6 and U7 are analog multipliers connected as a variable gain, wide-band, linear amplifier. The modulation reference (U6-X1) is multiplied by a factor determined by the *carrier ref* (U6-Y1) and *B+ sample* (U7-X1) signals to determine the gain and, in turn, the status of U7-Y1.

When there is no *Unbalanced Audio* input at P1-15, U2D's output (TP3), which is the modulation reference, will be a nominal 1.4 V. This voltage is applied as U6's X1 input.

The *Carrier Ref* input at P1-2 is a dc voltage directly proportional to the square of the expected RF carrier level. This voltage is applied to U6-Y1.

The *B+ Sample* input at P1-3 is a dc voltage directly proportional to the B+ voltage being applied to the transmitter's RF power stage. When the B+ voltage is 236 V (for VR250) or 167 V (for VR125), the *B+ Sample* input and, in turn, the output of buffer U3D (TP4), are a nominal 4.0 V (for VR250) or 2.8 V (for VR125). This voltage is applied to U7-X1.

The gain of U6 and U7 and, in turn, the voltage at U7-Y1 is determined by the following formula:

*Unbalanced Audio * Carrier Ref / B+ Ref*

When the *Carrier Ref* input (U6-Y1) is 4.7 V and the *B+ Sample* input (U7-X1) is 4.0 V (for VR250) or 2.8 V (for VR125), the gain of U6 is 1.18 (for VR250) or 1.68 (for VR125) for the dc reference applied to U6-X1. The U7-Y1 current is 1.18 (for VR250) or 1.68 (for VR125) times the U6-X1 current. U3B is connected as a less than unity amplifier and its gain is summed with U7's gain. The end result is the total voltage gain of the circuit, relative to the voltage at the output of U2D (1.4 V), is a nominal 1.11 (for VR250) or 1.58 (for VR125) when **GAIN TRIM** potentiometer R31 is set to the centre of its range. The output of U3B (TP8) is 1.55 (for VR250; 1.4 V x 1.11) or 2.21 (for VR125; 1.4 V x 1.58).

The gain of U7 will change in direct proportion to changes in the *Carrier Ref* voltage. If the *Carrier Ref* voltage is set to 0 V, or it is clamped to ground because Q1 is turned on, U7's gain is minimum (zero). In turn, the dc reference's multiplication factor is minimum (zero). The transmitter's RF output is turned off.

The gain of U7 will change in inverse proportion to changes in the *B+ Sample* input. This feature eliminates the need for sophisticated filtering of the transmitter's B+ power supply and maintains the transmitter's RF output at the original level for B+ voltage variations of ±10%.

GAIN TRIM potentiometer R31 provides a nominal 10% adjustment in the *carrier level ref* output of U3B. In dual exciter applications, it is adjusted to compensate for tolerance differences in the PDM generators of exciters A and B. When it is set properly, the transmitter's RF output is the same when either exciter is selected, provided the same *Carrier Ref* is being applied.

6.4.3.2 PDM DIVIDER

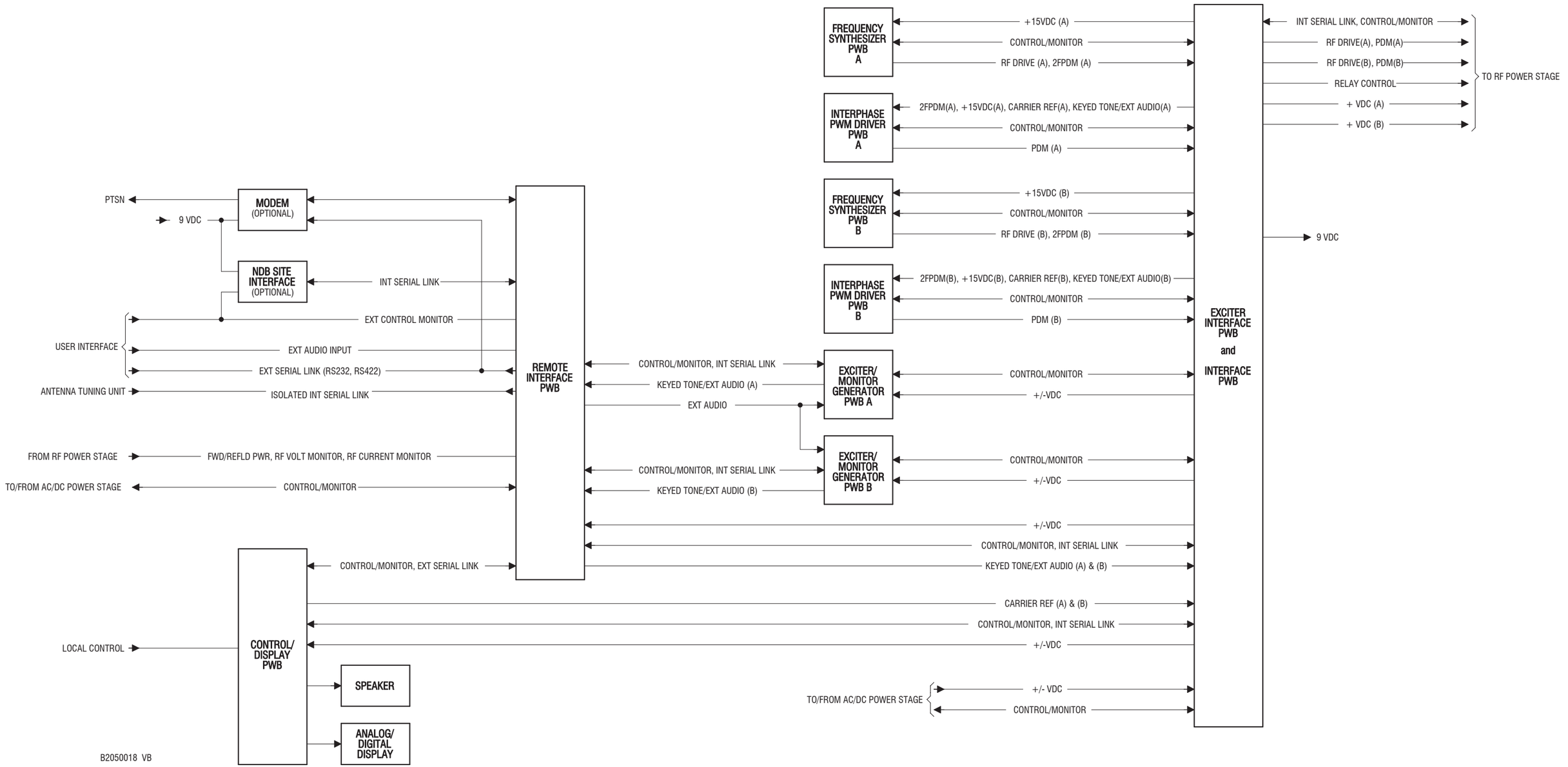
The PDM divider circuit divides the $2f_{PDM}$ input frequency (P1-7) by two. The resulting f_{PDM} output (P1-10) is a 0 V to 15 V square wave. Unless otherwise established during the transmitter's manufacture, it should be a fixed frequency, nominally 130 kHz.

6.4.3.3 LINEAR INTEGRATOR

The linear integrator circuit converts the f_{PDM} square wave input to a triangular waveform. The triangular waveform has negative and positive voltage excursions of equal amplitude and duration. The long R/C time constant formed by C26/R10 ensures a linear rise and fall time. Since the R/C time constant is fixed, the waveform amplitude varies over the frequency range of f_{PDM}. The charge/discharge time and waveform amplitude are maximum at the lowest frequency.

6.4.3.4 INTEGRATOR PEAK DETECTOR

The integrator peak detector circuit detects the positive going parts of the linear integrator's triangular waveform. A portion of the resulting positive dc voltage (nominally 1.8 V) at U2C's output, is applied to the inverting input of differential amplifier U3A. The *carrier level ref* output of U3A is offset by this voltage, which is proportional to the triangular waveform voltage peaks. This offset effectively sets the *carrier level ref's* zero power reference to the triangular waveform's peak voltage. This ensures no RF output is produced when the *Carrier Ref* input (P1-2) is 0 V.



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Block Diagram – Exciter/Control/Monitor Stage			
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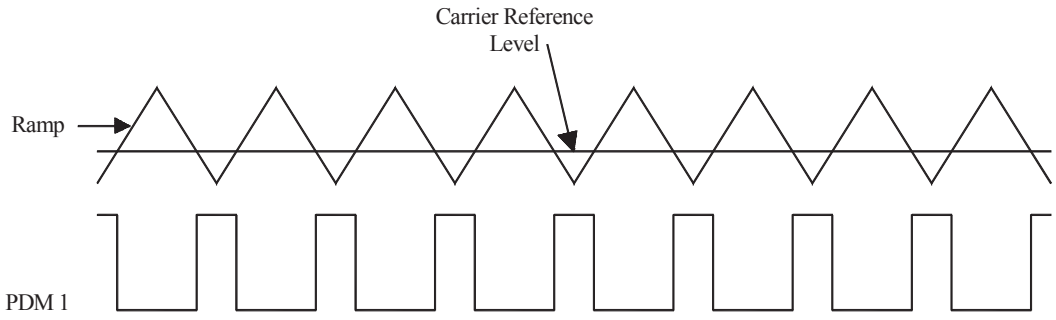


Figure 6-3 Timing Diagram for PDM Differential Amplifier

6.4.3.5 INTERPHASE PDM GENERATOR

The interphase PDM generator consists of two identical variable pulse duration generators (PDM1 and PDM2; PDM1 circuitry is described). The PDM1 generator produces a 0 V to 15 V rectangular waveform at the f_{PDM} repetition rate. The waveform on/off ratio (duty cycle) is directly proportional to the carrier level. The transmitter uses three B+ voltage levels to maximize performance. As the RF output power is increased from 0 W (B+ voltage is 55 V for VR125; 79 V for VR250), the PDM duty cycle increases proportionally. When the RF output is increased so that the PDM duty cycle reaches 45 %, the control/ display PWB initiates a B+ voltage increase (to 97 V for VR125; 136 V for VR250) and a PDM duty cycle decrease (to 27%). When the RF output is increased to a level where the PDM duty cycle again reaches 45%, the control/ display PWB initiates a B+ voltage increase (to 167 V for VR125; 236 V for VR250) and a PDM duty cycle decrease (to 32%).

6.4.3.5.1 PDM1 Generator

The PDM1 generator consists of U10B, transistors Q4, Q5, and associated components. The compensated *carrier level ref* input from the integrator peak detector circuit is applied to differential amplifier U10B's non-inverting input, where it is compared to the triangular waveform from the linear integrator circuit. When the compensated *carrier level ref* is more positive than the triangular waveform, U10B's output is open collector. +15 V is applied through R60 and R62 to the balanced drive formed by Q4/Q5. Q4 turns on and applies +15 V to K1-3 as the PDM1 output (Q5 is off). For the rest of the triangular waveform's period, the compensated *carrier level ref* is less positive than the triangular waveform. U10B's output is a current-sink-to -15 V and Q4 turns off. Q5 turns on and clamps the PDM1 output to ground. The minimum 'on time' (zero RF power) occurs at the negative peaks of the triangular waveform. See Figure 6-3 for a timing diagram.

6.4.3.6 PDM FAULT DETECTOR
The PDM fault detector circuit contains a voltage controlled switch that controls the 'set/'reset' status of the shutback latch circuit and, in turn, controls the on/off status of relay K1.

The PDM1 fault detector circuit consists of U12A and its associated components. R67/C58 form an integrator with a long time constant, relative to the PDM frequency. C58's charge voltage is applied to U12A's inverting input and compared to the 5 V reference voltage applied to its non-inverting input from voltage divider R70/R71/R72. U12A's output is an open collector and has no influence when C58's charge voltage is less positive than the reference voltage. U12A's output will switch to a current-sink-to-ground when C58's charge voltage goes more positive than the reference voltage.

During normal operation, C58 will charge through R67 towards 15 V when the PDM1 output is 15 V ('on time') and CR3 is reversed biased. It will instantly discharge to 0 V, through CR3, when the PDM1 output switches to 0 V ('off time'). The repetition rate of the PDM1 on/off periods ensures the charge on C58 will not exceed 5 V, provided each PDM1 cycle contains an 'off time'. If a PDM failure occurs such that it produces a continuous 'on time', C58 will charge more positively than 5 V. U12A's output will switch to a current-sink-to-ground and toggle the shutback latch circuit to its 'set' state.

6.4.3.7 SHUTBACK LATCH
The shutback latch circuit inhibits the 'on time' of the PDM output and, in turn, the RF output of the transmitter whenever a transmitter originated *Inhibit PDM* (P1-16) command is applied. This circuit provides additional protection to the transmitter's RF power stages when faults are detected or actions are initiated that may cause RF stress current thresholds to be exceeded. Its function is to de-energize K1 and disconnect the *PDM 1* output from the transmitter circuits when the PDM fault detector output is a current-sink-to-ground (logic low). It also inhibits the PDM generator when relay K1 is de-energized or when a logic true *inhibit PDM* command is applied to P1-16.

U9A/U9B form a bistable flip/flop. The flip-flop's output (U9-3) will be 15 V (logic high) in its 'reset' state, and a current-sink-to-ground (logic low) in its 'set' state.

Normally the *inhibit PDM* input and the output of the PDM fault detector circuit, which are the flip-flop's controlling inputs, are open collector. 5 V (logic high) is applied to U9-1 and U9-5 through their pull-up resistors and the flip-flop is latched in its 'reset' state. Relay K1 is held energized and the PDM output is applied to the transmitter circuits.

If a PDM fault is sensed, the PDM fault detector circuit applies a current-sink-to-ground (logic low) to U9-5 and causes the flip-flop to switch to and latch in its 'set' state. Relay K1 de-energizes and disconnects the PDM output from the transmitter circuits. The *PDM latch* output (J1-11) is activated (5 V). This condition is maintained until the flip-flop is reset by the removal of the logic low from U9-5 (no PDM fault) and the application of logic low to U9-1 (a logic true current-sink-to-ground *reset PDM* command is applied to J1-1).

6.4.3.8 PDM INHIBIT
The PDM inhibit circuit consists of U9D, transistor Q2, and their associated circuits. Its function is to instantly clamp the output of the PDM generator to ground (zero carrier level) when a logic true (current-sink-to-ground) *inhibit PDM* input is applied to P1-16, or when the PDM fault detector circuit senses a PDM fault and the shutback latch circuit's flip-flop is latched in its 'set' state. When neither of these conditions are true, the PDM inhibit circuit has no influence.

6.4.4 Exciter Monitor/Generator PWBs

See Figures SD-19 and SD-20. The exciter/monitor/generator PWBs [A7 (exciter A) and A10 (exciter B, if used)] perform the following functions:

- Use the press-to-talk input to select between beacon and voice modes.
- Monitor and control modulation depth
- Selects the parameter, RF current or RF voltage, to be applied to the remote interface PWB for external monitoring.
- Generate the appropriate tone frequency
- Monitors tone and keyer operation
- Monitors the forward power and controls changeover and inhibit functions.

6.4.4.1 MICROCONTROLLER

Microcontroller U11 uses the SPI bus to communicate with shift register U16 which shifts out digital data used to control various signals including changeover, shutdown, RF off, and alarm. Watchdog timer IC U2 and associated components generate a *Keying/Misc Alarm* (J1-4) if the microcontroller falls into an unknown state.

The clock for the microcontroller and the tone oscillator is generated using Y1, U4:E and the associated components.

The microcontroller (U11) continually monitors its internal Flash and EEPROM memory using checksums. If for some reason, the checksum returns as invalid, the microcontroller will detect the error and raise a flag, resulting in the output power being inhibit. U2 acts as a watchdog timer, if the watchdog times out, the monitor fault will also be raised, causing the output power to be inhibited (via the control/display PWB). This will guarantee that the U11 is always operating as intended.

6.4.4.2 PRESS-TO-TALK

The input to U11:11 indicates to the exciter monitor/generator PWB which mode of operation it should be operating in. It will react by adjusting the U16:1 that controls the MUX U1:X.

6.4.4.3 MODULATION DEPTH FUNCTIONS

Modulation depth of the beacon, voice and beacon, and voice are controlled using the digital pots 1, 2 and 3 of U10 respectively. The levels of the pots in U10 are adjusted by the microcontroller U11 over the SPI bus.

A selection between RF Monitor Voltage and RF Monitor Current samples is made using the MUX U14:C. CR9, U9:B and their associated components RF detect the selected RF monitor signal. The RF monitor signal is then used to calculate the modulation depth. The microcontroller (U11) compares the average and peak levels of the RF signal. The average value is detected using U9:A and its associated components. The peak level is detected using U9:C, CR7, and their associated components.

6.4.4.4 TONE GENERATION

The keyer tone is generated using the DDS IC U5. The microcontroller U11 sends an SPI signal to U5 indicating the frequency of the tone to generate. The tone is then amplified using U8:C and its associated components. The microcontroller (U11) then controls keying by toggling the MUX U1:Z.

Correct operation of the keyer is monitored by U8:A, U8:B, CR11, and CR12 and there associated components. The analog samples at U11:27 and U11:28 are compared to the low threshold levels (set up using the GUI) to determine if the keying gate is opened or closed. If at any time the keying gate is opened when it should be closed or closed when it should be opened, and alarm is flagged and output power is inhibited (via the control/display PWB).

6.4.4.5 FORWARD POWER MONITOR

A dc voltage, proportional to the transmitter's forward power, is applied to the *Forward Power Sample* input (P1-1). This voltage is filtered by operational amplifier U9 and associated components and applied to U11's internal ADC. If the forward power sample is above or below user-defined limits for a user-defined time period, the *Changeover* output (J4-15) becomes active (logic low). If a changeover had already occurred prior to this occurrence, a *Shutdown* output (J4-16) will also be generated. All user-defined parameters are established using the front panel GUI and applied to the exciter monitor/generator PWB via the internal serial bus.

6.4.4.6 RF MONITOR PARAMETER SELECTION

Multiplexer U14 and associated components allows the user to select the parameter (RF voltage or RF current) to be applied to the **RF MONITOR** output at the rear of the exciter.

6.5 CONTROL/MONITOR STAGE

See Figures 6-2 and SD-3. The control/monitor stage contains the control/display PWB, which contains the transmitter's embedded microcontroller. The remote interface PWB, graphic user interface (GUI), analog/digital displays and audio speaker are also contained here. The NDB site interface PWB (A4) and a modem (U11) are optional items that can also be part of the control/monitor stage.

6.5.1 Control/Display PWB

See Figures SD-5 through SD-8. The control/display PWB (A1) performs the following functions:

- Produces dc voltage *Carrier Ref (A)* and *(B)* outputs that ultimately determine the forward power (RF carrier) level of the RF output. These voltages are the reference voltages for the variable pulse duration modulation (PDM) generator in each exciter (A and B).
- Monitors critical parameters and turns off (shuts back) or reduces (cuts back) the *Carrier Ref* voltage when defined fault threshold limits are exceeded.
- Identifies out-of-tolerance parameters when the carrier level is shut back or cut back by providing a visual indication for local monitoring or an electrical status output for remote monitoring.
- Selects the main exciter (A or B) that will provide the RF drive and PDM drive to the RF power stage's RF amplifiers, if no changeover has occurred.
- Determines on/off status of RF power stage.
- Interfaces with the diagnostic display.

6.5.1.1 CARRIER REFERENCE VOLTAGE

The *Carrier Ref (A)* (J7-38) and *(B)* (J7-40) outputs are applied to the interphase PDM driver PWB of each exciter to generate the PDM drive pulse that ultimately controls the RF output of the transmitter. DACs U31 and U32, in conjunction with microcontroller U22, establish a dc reference voltage for the *Carrier Ref* outputs. The voltage is buffered through operational amplifiers U27B, U28B and associated components.

6.5.1.2 ALARM THRESHOLD CIRCUITS

Certain parameters that are monitored by the control/display PWB can initiate an alarm indication and appropriate transmitter control if an out of tolerance condition occurs.

6.5.1.2.1 Ac Supply Voltage

The *Ac Power* input (J4-21) is an unregulated dc voltage that is proportional to the ac source. The input is filtered and compared to the *low ac ref* fault threshold on operational amplifier U4C. If the *Ac Power* voltage is below this threshold, the *ac low* signals switch to 0 V. The *Carrier Ref (A)* and *(B)* outputs clamp to 0 V and the *Shutback (A)* (J7 1) and *(B)* (J7-2) outputs switch to 0 V and inhibit the exciter's modulator drive. The transmitter's RF output turns off (shuts back) and remains off until the ac power returns to an acceptable voltage. The system diagram's **AC Mains** lamp displays a fault condition. An *Ac Sample* signal is applied to ADC U9 for application to the diagnostic display.

6.5.1.2.2 Reflected Power Monitor

The *Refld Pwr Sample* input (J1-5) is a dc voltage that is proportional to the reflected power at the transmitter's output. The input is filtered and buffered by operational amplifier U1B and associated components, and then applied to the remote interface PWB via the external serial interface (microcontroller U22). The signal is also compared to a pre-determined *refld pwr shtbk ref* fault threshold on operational amplifier U4A. When the reflected power indicates a VSWR of greater than 2:1, relative to rated forward power, the *refld pwr sample* input exceeds the fault threshold and the *refld_pwr_shutback* signal switches to 5 V. The *Carrier Ref (A)* and *(B)* outputs clamp to 0 V and the *Shutback (A)* (J7-1) and *(B)* (J7-2) outputs switch to 0 V and inhibit the exciter's modulator drive. A clock pulse is also applied to an alarm count/ cutback circuit in complex programmable logic device (CPLD) U18. The RF output is instantly shut back (turn off). The system diagram's **Output Network** lamp displays a fault condition. A *Refld Pwr Sample* signal is applied to ADC U9 for application to the front panel's diagnostic display.

Turning off the RF output reduces the *refld pwr sample* input to 0 V. The *Carrier Ref (A)* and *(B)* outputs are restored to their pre-shutback levels, the *Shutback A* and *B* outputs return to open collector, and the RF output is restored at an exponential rate. If the fault threshold is exceeded before the pre-set power level is reached, the shutback cycle is repeated. If two or more shutback cycle clock pulses are applied within any two second period, the *Carrier Ref* outputs are cut back (reduced) until the carrier level is cut back to a level that results in an acceptable reflected power. When the transmitter enters cutback mode, the system diagram's **Output Network** lamp flashes on and off. When the *refld pwr sample* input returns to or is maintained at a level which is less than the fault threshold, the *Shutback* outputs returns to open collector but the system diagram's **Output Network** lamp continues to display a fault as a maintenance aid. The lamp remains on until reset by the diagnostic display menu.

6.5.1.3 SAMPLE MONITORING CIRCUITS

In addition to the parameters described in paragraph 6.5.6.2, various parameters are applied to the control/display PWB for local (via the front panel's diagnostic display) and external (via the remote interface PWB) monitoring. In some cases, these parameters have associated alarm detection circuitry, but it is not resident on the control/display PWB.

6.5.1.3.1 PDM Drive

The *PDM (A)* (J4-9) and *PDM (B)* (J4-7) inputs are pulses which represent the PDM signal applied to RF power modules A and B. The inputs are filtered through operational amplifiers U7B and U11B and associated components. *PDM (A) Sample* and *PDM (B) Sample* signals are applied to ADC U9 for application to the front panel's diagnostic display.

6.5.1.3.2 Forward Power

The *Fwd Pwr Sample* input (J1-3) is a dc voltage which represents the forward power at the transmitter's RF output. The input is filtered through operational amplifier U2D and associated components. A *fwd_pwr_sample* signal is applied to ADC U9 for application to the front panel's diagnostic display. The *fwd_pwr_sample* input is also applied to the remote interface PWB via the external serial interface (microcontroller U22). The *Fwd Pwr Sample* input is also low-pass filtered through operational amplifier U2C and associated components. A *speaker_ref_level* signal is applied through DAC U32. The analog output (pin 12) is filtered through operational amplifier U28D and associated components and applied to the *Audio (Speaker)* output (J11-1), then applied to speaker LS1 for audio monitoring.

6.5.1.3.3 Battery Voltage

The *Battery Voltage* input (J1-27) is a dc voltage which represents the voltage applied from the transmitter's optional battery supply. The input is filtered through operational amplifier U3B and associated components. The *bat_volt_sample* signal is applied to ADC U12 for application to the front panel's diagnostic display.

6.5.1.3.4 Battery Current

The *Battery Current* input (J1-25) is a dc voltage which represents the current drawn by the transmitter's optional battery supply. The input is filtered through operational amplifier U3A and associated components. The *bat_cur_sample* signal is applied to ADC U12 for application to the front panel's diagnostic display.

6.5.1.3.5 Low Voltage Power Supplies

Attenuated, buffered samples of all low voltage dc power supplies (+24 V, ± 15 V and + 5 V) are applied to ADCs U9 and U12 for application to the front panel's diagnostic display.

6.5.1.3.6 Cabinet Temperature

Low voltage temperature sensor U5 provides a dc voltage (between 0 and 5 V) which represents the ambient cabinet temperature. This voltage is buffered by operational amplifier U8A and associated components and applied to ADC U12 for application to the front panel's diagnostic display.

6.5.1.4 MICROCONTROLLER

Microcontroller IC U22 interfaces between the diagnostic display and its associated soft-keys. It controls the level of the *Carrier Ref* signals (see paragraph 6.5.1.1), which ultimately determines the forward power level of the transmitter. It also acts as an internal and external serial interface for transmitter alarm and status signals.

6.5.1.5 CPLD

Complex programmable logic device (CPLD) U18 continuously reads digital inputs for all transmitter alarm events. It is programmed to perform root cause detection of a fault as well as high-speed fault protection. Depending on the nature of the fault, the CPLD generates transmitter *Shutback* outputs (J7-1 and J7-2) or various digital control/inhibit signals via a parallel data bus.

6.5.2 Remote Interface PWB

See Figures SD-11 through SD-13. The remote interface PWB (A2A2) performs the following functions:

- Buffers all external transmitter remote control inputs and provides the connection for the system's external interlock circuit
- Provides RF filtering for RF power probe samples (forward power, reflected power, and RF current)
- Provides an isolated ATU serial interface
- Converts external serial levels from TTL to RS232 and RS422
- RF monitor conditioning
- Press-to-talk input
- Audio conditioning
- Audio monitoring
- Provides distribution and interface point between the ac/dc distribution stages and exciter control/monitor stage

6.5.2.1 Remote Inputs/Outputs

U7:A and associated components form the circuitry to allow control of RF on/off when in remote mode. U21:C and associated components form the circuitry to control the external interlock. If the link between TB1-19 and TB2-20 is open, U21:C will output a high (external interlock), causing the transmitter to inhibit RF power.

6.5.2.2 Isolated ATU Serial Interface

U9, U11, U13, U14, U15, and U17 provide isolation to the internal serial bus (RS485) to allow for ATU control. The ATU provides 5 V to opto-isolators U13 and U14, which provide isolation between differential transceivers U11 and U17. The ATU controls the DE/$\overline{RE}$ signal (J3-5), allowing the ATU to specify direction of transmission through the isolated link preventing collisions over the serial bus.

6.5.2.3 RS232 and RS422 Interface

U19, U18, U12, convert the TTL levels produced by the control/display PWB to RS232 and RS422 levels for external control/monitoring of the transmitter.

6.5.2.4 RF Monitor Conditioning

U16 and associated components allow the user to specify the RF monitor level from the GUI. U23 and R163 form an adjustable gain amplifier for the RF monitor signal that is able to drive a 50 Ω load.

6.5.2.5 Press-To-Talk Input

Link E4 allows for the selection of phantom feed or normal press-to-talk operation. When in position A, normal operation is selected and grounding TB1-12 indicates press-to-talk mode. When in position B, phantom feed mode is selected and applying -15 V to the shield (TB1-15) will indicate press-to-talk mode.

6.5.2.6 Audio Conditioning

The audio conditioning circuitry on the remote interface board consists of 3 parts, balanced conditioning, audio filtering, and the audio limiting.

6.5.2.6.1 Balanced Conditioning

U3:A and its associated components convert the balance audio signal between TB1-14 and TB1-16 to an unbalanced signal. The level of the audio signal is adjusted using **AUDIO LEVEL** potentiometer R37.

6.5.2.6.2 Audio Filtering

U8:B, U8:C, U8:D and their associated components forms the audio input filter. This filter, along with the poles located on the Exciter Interface PWB and the Modulator Filter, is a band pass filter passing signals from 300 to 3000 Hz.

6.5.2.6.3 Audio Limiting

U10:B, U10:C, U10:D, Q7, and their associated components form the audio limiter. The limiter will raise an alarm at U10:13 when the audio signal goes above a pre-defined threshold. It will then compress the audio signal by adjusting the resistance across the JFET Q7. This is accomplished by adjusting the JFET's base voltage at the output of the comparators U10:B and U10:C.

6.5.2.7 Audio Monitor

U1:B and T1 condition the forward power sample signal to produce an audio monitor signal that can be used to view the modulated signal being output by the transmitter.

6.5.3 Front Panel Metering

The front panel of the exciter control/monitor assembly provides local controls and a graphic user interface to display operating status, root cause fault detection, RF power, and critical dc voltage/current levels. The controller/display PWB is mounted on the rear of the panel. The front panel is divided into three sections – system diagram, diagnostic display and control.

6.5.3.1 SYSTEM DIAGRAM

The system diagram is a functional flow diagram of the transmitter. Each section of the flow diagram contains an alarm lamp, which turns on when a fault occurs in that section. If a lamp is flashing, the transmitter has entered a cutback (reduced power) mode of operation. The lamp that is flashing is likely the cause for the cutback.

6.5.3.2 DIAGNOSTIC DISPLAY

The diagnostic display is a graphic user interface (GUI) screen that is navigated using five associated soft-keys. The majority of the transmitter's local control (exciter selection, power level, etc.) and monitoring (critical parameter levels, alarm events, etc.) may be performed from menus on this display. An analog meter is provided, which can display forward power, reflected power, modulation percentage or antenna current.

6.5.3.3 CONTROL SWITCHES

The control switches determine the transmitter's control location (local or remote) and its RF status (on or off).

6.5.3.3.1 Local/Remote Selection

When **Local** is selected, all remote control functions, except RF off, are disabled and have no influence on the transmitter's operating status or pre-set RF power levels. When **Remote** is selected, all front panel control functions, except **RF Off**, are disabled and have no influence on the transmitter's operating status or pre-set RF power levels.

6.5.3.3.2 RF On/RF Off Selection

When **RF On** is selected (enabled in **Local** mode only), the transmitter's RF power stage is enabled to provide an RF output. When **RF Off** is selected (enabled in **Local** and **Remote** modes), the transmitter's RF power stage is inhibited.

6.5.3.3.3 Power Increase/Decrease

When **Power Increase** is pressed (enabled in **Local** mode only), the transmitter's RF output power is increased. When **Power Decrease** is pressed (enabled in **Local** mode only), the transmitter's RF output power is decreased. Additionally, if both the **Power Increase** and **Power Decrease** switches are depressed simultaneously, the transmitter's RF output power will be reduced to 0 W.

6.5.4 NDB Site Interface PWB (Optional)

See Figures SD-14 and 15. The NDB site interface PWB (A4), if purchased, provides:

- 16 optically isolated monitor inputs.
- 16 form C contact relay closure control points.

6.5.4.1 Site Monitor Points

RFI filtering is provided on all control input lines to ensure transmitter operation is not interrupted due to RF pick-up on control lines. Opto-couplers buffer/isolate the external circuits and prevent unwanted transients from affecting transmitter operation. All isolated inputs are driven by isolated dc to dc converter U1 to prevent unwanted transients from affecting the transmitter's dc supplies. The monitor inputs are shifted in through shift registers U6 and U9. These values are then relayed to the control/display PWB over the internal serial bus using RS485 transceiver U12.

6.5.4.2 Site Control Points

Shift registers U17 and U19, controlled by microcontroller U13 over the SPI bus will control relays K1 to K16. Control point logic levels are determined by the control/display PWB and are communicated to the NDB site interface PWB over the internal serial bus.

6.5.5 Modem (Optional)

See Figure SD-3. An optional modem (U11) can be provided to interface the transmitter's RS232 Ext Serial Link to a PTSN. The link provides remote monitoring and status for the transmitter.

6.6 RF POWER STAGE

See Figures 6-5 and SD-4. The RF power stage produces the transmitter's final RF output. It contains the RF power modules (A12 and A13, if used), the RF filter PWB (A14) and the RF power probe (A15).

6.6.1 RF Power Module(s)

See Figure SD-22. Each RF power module (A12 and, if purchased, A13) produces up to 250 W (for VR250) or 125 W (for VR125) RF carrier power to the transmitter's RF output and contains a wideband power amplifier, a modulator, and a modulator filter. A switch mode power supply PWB is provided to convert the ac input voltage to the high level B+ voltage used by the modulator assembly. Each module's RF output is applied to the RF filter PWB (A14) via RF relay K1 (see SD-4), which determines the 'on-air' module'. A power module interface PWB is provided to interface control/monitor signals between the RF power modules and the exciter and control/monitor stages as required. For VR250 transmitters, cooling air for the RF power modules is provided by fans B1 and B2.

6.6.1.1 SWITCH MODE POWER SUPPLY PWB

See Figure SD-24. The switch mode power supply PWB (A2) converts the transmitter's ac input voltage to the B+ voltage used by the modulator. In the VR250, the ac input voltage range is 170 – 270 V ac and the B+ voltages used by the modulator are 79 V, 136 V and 236 V. In the VR125, the ac input voltage range is 90 – 270 V ac and the B+ voltages used by the modulator are 55 V, 97 V and 167 V.

6.6.1.1.1 Rectifier

The ac input voltage is rectified by diodes U1 and U2, providing a dc voltage across capacitors C12 through C17. Varistors RV1 through RV3 provide protection from high voltage transients. **AC IND** lamp DS1 provides a status indication of the ac voltage on the RF power module.

6.6.1.1.2 Switching Signal

IC U3 is a high current FET driver that provides a switching PWM signal (0-18 V) to the primary of transformer T2. The secondaries of T2 control the on/off status of FETs Q1 and Q2, which in turn switch the rectified ac voltage to the primary of step-up transformer T1/T4.

6.6.1.1.3 B+ Voltage

The secondaries of step-up transformer T1 are rectified by diodes CR9, CR10, CR11, CR13, CR14, and CR15 and combine, through chokes L4, L5 and L6, to form the high level B+ voltage. This voltage is applied to the *Dc Output* (J2-1). Samples of the B+ voltage and current are applied to inputs of current mode PWM controller U8, which provides PWM switching information to regulate the B+ voltage. FETs Q4, Q5 and resistors R10, R11, R24 and R25, in conjunction with opto-couplers U4 and U6, provide a means to adjust the attenuated voltage applied to U8, thereby adjusting the level of the B+ voltage.

6.6.1.1.4 Inhibit PWM

When an RF power module fault occurs, an *Inhibit* signal is provided to J1-7. Opto-coupler U7 will turn on and apply a signal to current mode PWM controller U8 to inhibit the switching signal output of FET driver U3.

6.6.1.2 POWER MODULE CONTROL/ INTERFACE PWB

See Figure SD-23. With the exception of the ac input for the switching power supply and the RF output of the module, the power module control/interface PWB (A1) provides the input and output connections for the RF power module. It performs the following functions:

6.6.1.2.1 Module Status

Module status such as B+ and PA voltage, dc current, and temperature are measured using ADC inputs on microcontroller U7. The *Fan Tach 1* and *2* inputs are also captured using interrupt 0 and interrupt 1 on U7. All information is transmitted to the control/ display PWB using the internal serial bus.

6.6.1.2.2 Gate Bias Drive Signal

U7, Q2 and associated components generate a 15 V square wave at 263 kHz to drive the gate bias drive in the modulator.

6.6.1.2.3 Switch Mode Supply Control

Decodes the serial control (B+ settings) from the control/display PWB and outputs the settings using darlington transistor U1.

6.6.1.3 MODULATOR

See Figure SD-22. The modulator (A5) is a logic level converter that converts the low level (0 to 15 V) logic of the *PDM* input to a high level (0-B+) logic *PDM (B+)* output.

6.6.1.3.1 13 V Power Supply

The 15 V *LO* output (pin 1) of FET driver U1 is full-wave rectified by bridge rectifier CR1 through CR4, at the PDM frequency. The resultant dc voltage is filtered by capacitor C7 and limited to 13 V by zener diode CR5. The power supply's less positive output is referenced to the source terminal of power FET Q1 via resistor R7. Therefore, the positive output is always 13 V higher than the voltage on the FET source terminal. The 13 V output is applied to U1's V_B (+) and V_S (-) inputs as the switched gate drive for the FETs. Transformer T1 provides isolation between the high and low level signals.

6.6.1.3.2 FET Driver

FET driver U1 is an integrated circuit configured to produce outputs as follows:

- When the PDM signal applied to the H_{IN} input is high (15 V), the H_O output is the dc voltage applied to the V_B input.

- When the PDM signal applied to the H_{IN} input is low (0 V), the H_O output is the reference voltage applied to the V_S input.

The H_O output, which contains the PDM data, is applied to the gate of power MOSFET Q1 as its on/off control.

6.6.1.3.3 B+ Switching MOSFET

Power MOSFET Q1 is connected to switch the B+ voltage at the on/off ratio of the PDM data on U1's H_O output, which is applied to its gate. The resultant *PDM (B+)* output contains the PDM data applied to J2-7 at a high (0-B+) logic level. Free-wheeling diode CR6 prevents negative overshoot by providing current flow when MOSFET Q1 is off.

6.6.1.4 MODULATOR FILTER PWB

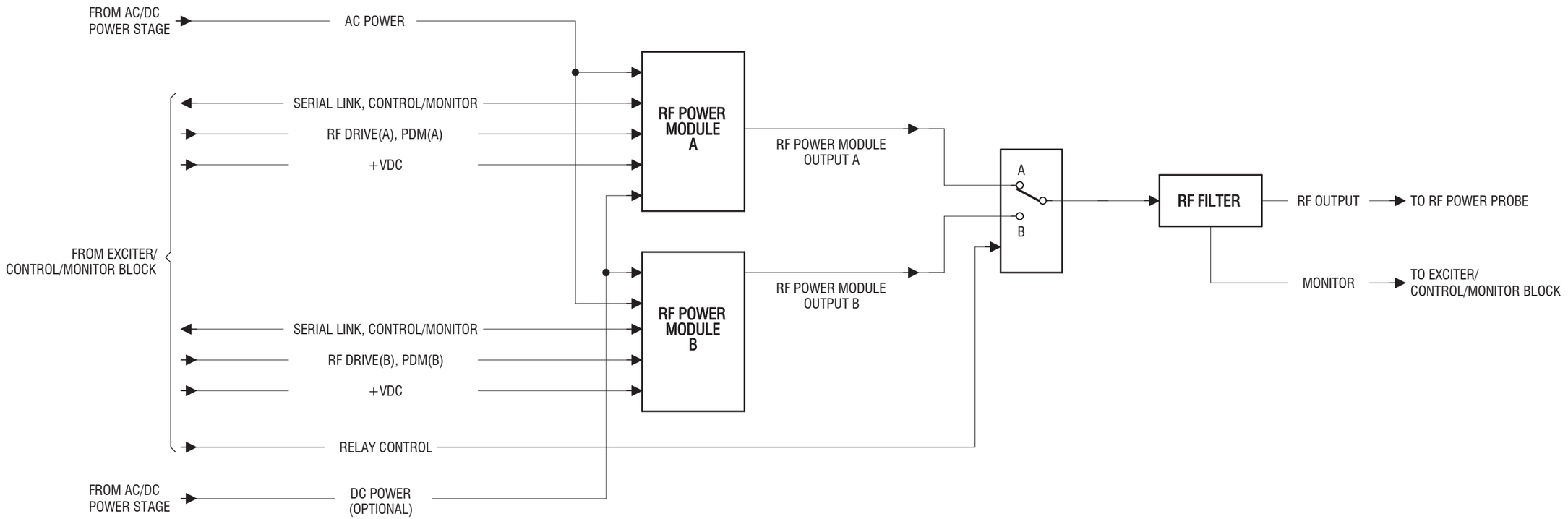
See Figure SD-22. The modulator filter PWB (A4) consists of inductors L1 and L2 and capacitors C1 and C3 as well as C2 of the power amplifier (A3). These components form a low pass filter that passes the audio components but rejects the PDM frequency. When no modulating audio information is present, the *PA Volts* output will be a dc voltage equal to the modulator input voltage multiplied by the duty cycle of the PDM (B+) signal. Capacitor C3 in conjunction with L2 is resonant at a frequency to provide optimal rejection of the PDM frequency.

6.6.1.5 POWER AMPLIFIER

See Figure SD-22. The power amplifier (A3) uses two parallel pairs of MOSFETs to produce an unfiltered, modulated RF output. Q1 through Q4 are connected as cascode or 'H' bridge class 'D' amplifiers, which switch the *PA volts* at the RF drive frequency (see Figure 6-6 for a description of class D operation). Transformer T1 splits the *RF drive* signal and applies it, through buffer amplifier U1 (fused by F1) to the MOSFETs with the required phase relationship. Diodes CR1 through CR4 prevent the output of the RF amplifier from going negative. Transistor Q5 and associated components detect the RF drive level and provide an alarm signal to the control/display PWB. Resistors R5 through R7 provide a *PA Volts Sample* for front panel monitoring.

6.6.1.6 RF TRANSFORMER

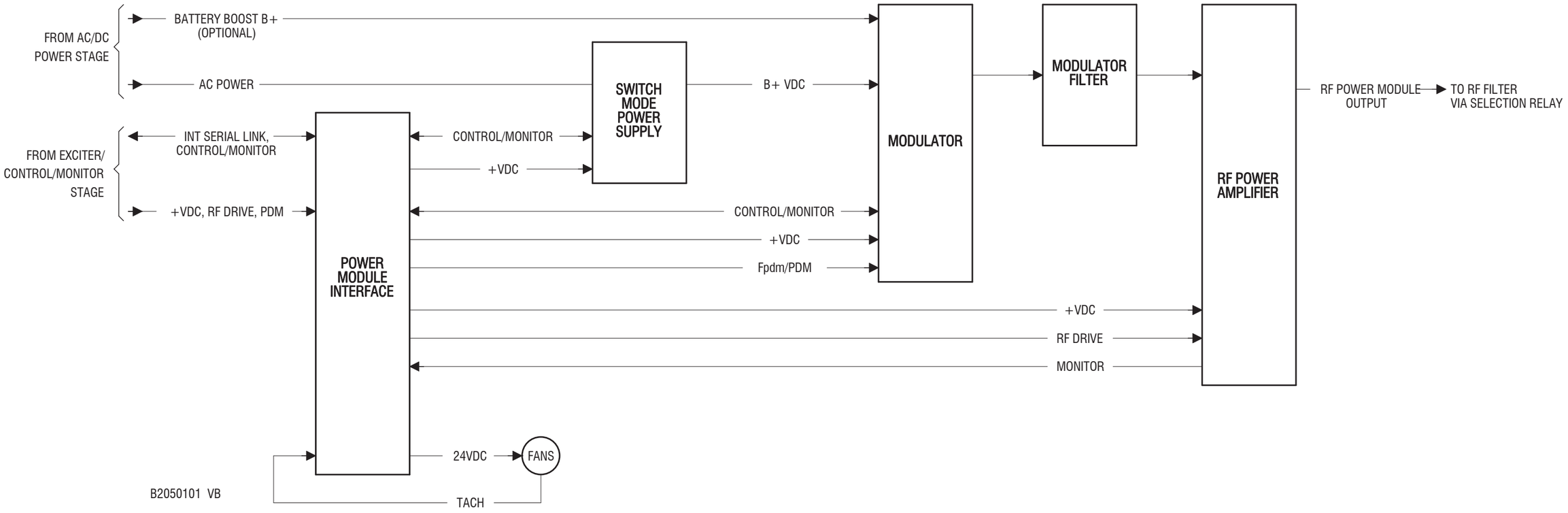
RF transformer T1 provides impedance matching between the power amplifier output and the RF filter PWB.



B2050103 VA

Dimensions = mm (inches)

Block Diagram – RF Power Stage			
Issue 1.8	Not to Scale	Figure 6-4	Page 6-25 (6-26 Blank)



Dimensions = mm (inches)

Block Diagram – RF Power Module			
Issue 1.8	Not to Scale	Figure 6-5	Page 6-27 (6-28 Blank)

6.6.2 RF Filter PWB

See Figure SD-4. The RF filter PWB (A14) is a band pass filter that attenuates the harmonics of the square wave output applied from the selected RF power module before it is applied to the RF combiner/probe. The filter has a flat response characteristic over the operating bandwidth [three PWB options; standard frequency band (190 - 535 kHz), extended frequency band for 125 W transmitters (536 - 1250 kHz and 1600 – 1800 kHz), and extended frequency band for 250 W transmitters (1600 – 1800 kHz)]. It has a nominal input and output impedance of 50 Ω and a loaded Q of 2. The band-pass is selected using frequency dependent link connections (E1 through E36; see Tables 2-7a and 2-7b).

6.6.3 RF Power Probe PWB

See Figure SD-4. The RF power probe PWB (A15) contains various circuits that monitor the RF output and provide RF voltage, RF current, forward power and reflected power monitoring samples to the control/monitor stage.

6.6.3.1 FORWARD/REFLECTED POWER PROBE

The forward/reflected power probe circuit consists of 40:1 RF current transformer T1, 80:4 RF voltage transformer T3 and associated components. These transformers form the current and voltage arms of a forward/reflected power bridge, which samples the RF output.

The current flowing into the RF output passes through transformer T1's primary. The current in T1's secondary develops a voltage across resistors R33, R34, R41, R42, R43 that is proportional to the RF output current. The anti-phase voltage across the secondary of RF voltage transformer T3 is applied (summed) to the centre-tap of T1's secondary. When the RF output impedance is precisely 50 Ω, the RF current waveform is in-phase and of equal amplitude to the RF voltage waveform on one half of T1's center-tapped secondary and equal amplitude, but 180° out-of-phase on the other half.

The in-phase voltages are summed, rectified by CR35, low-pass filtered by L9/C53/L11, resulting in a dc voltage being applied to the *Fwd Pwr Sample* output (J1-1). This voltage is proportional to the RF output's forward power level.

The out-of-phase voltages are summed, rectified by CR36, low-pass filtered by L8/C54/L10, resulting in a dc voltage being applied to the *Refld Pwr Sample* output (J1-5). This voltage is proportional to the RF output's reflected power level.

T3's secondary voltage, which is a true sample of the RF output's voltage waveform, is also applied to the *RF Volts Monitor* output (J1-9). This output is intended for monitoring by a modulation monitor and for test equipment during maintenance.

6.6.3.2 RF CURRENT PROBE

The RF current probe circuit consists of 40:1 RF current transformer T2 and associated components. The current flowing into the RF output passes through the primary of transformer T2. The current in T2's secondary winding develops a voltage across resistors R37 and R40 that is proportional to the primary (RF output) current. This voltage is applied to the *RF Current Sample* output (J1-17), which is used by the control/display PWB's high RF current detector and metering circuit. This high RF current detector produces a high RF current alarm and – via the control/display PWB - causes the transmitter's RF output to shut back (turn off) when the RF current exceeds a threshold that represents the maximum stress current for the RF power modules. The current sample voltage is also applied to the *RF Current Monitor* output (J1-13), which is used for external monitoring purposes.

6.7 MODULATION DEPTH WHEN USING A HIGH ‘Q’ ANTENNA

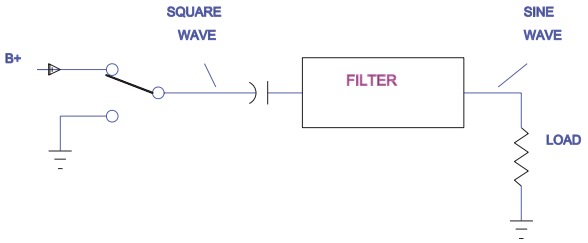
When the transmitter's output is connected to a high 'Q' antenna system, the modulation envelope observed on the RF current waveform may differ from that on the RF voltage waveform. This difference is caused by antenna impedance mismatch at the sideband frequencies, which results in reflected power standing waves on the feed cable. Depending upon feed cable length, the sideband impedance may be more or less than 50 Ω. When the sideband impedance is less than 50 Ω, the sideband current will increase and may place undesirable stress on the solid state devices in modulator/power amplifier.

When calibrating the modulation limits for the monitor (see 3.6.7), the system automatically tests using both current and voltage samples and selects the sample that places most stress on the transmitter (i.e., the highest modulation depth).

The following explanation should assist in understanding this phenomenon.

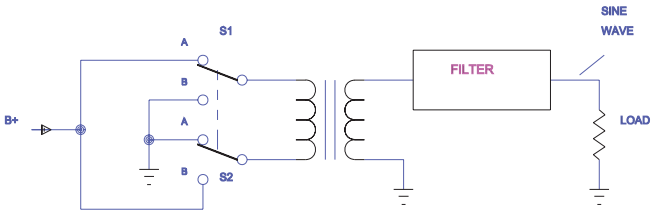
A typical radiobeacon antenna is relatively inefficient, since it is very short when compared with the wavelength of the carrier frequency. The high capacitive reactance of a typical antenna is tuned to the carrier frequency, by an antenna tuning unit's (ATU) loading coils, to produce a series resonant circuit. The resulting net antenna system resistance is then transformed to 50 Ω by a matching transformer. When the antenna is very short compared with the wavelength of the carrier frequency, the series resonant circuit has an extremely high 'Q'. Under these conditions, the antenna system may present a 50 Ω load to the transmitter at the carrier frequency but different impedance at the sideband frequencies.

The mismatch at the sideband frequencies will cause a standing wave on the feed cable. Depending upon the length of the feed cable, the sideband impedance of the antenna system will appear to be more or less than 50 Ω. When the transmitter is connected to a high 'Q' antenna system, the difference between the carrier impedance and the sideband impedance may cause RF stress current limits to be exceeded. When this occurs, remedial action must be taken instantly.



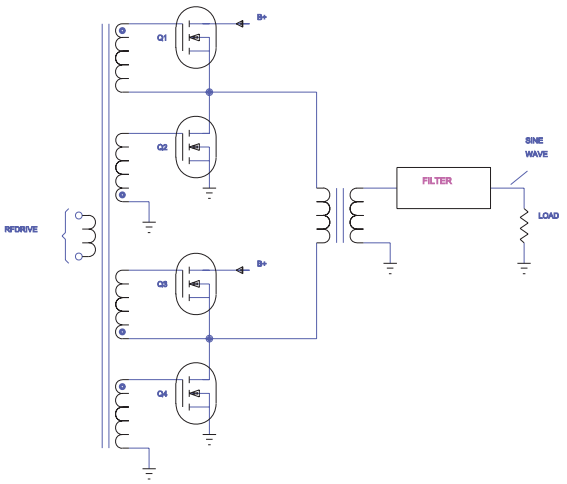
SIMPLE CLASS 'D' OPERATION

If the switch is opened and closed with a 50% duty cycle, a square wave at the switching frequency will result at the filter input. If the filter is designed to pass the switching frequency, but attenuate its harmonics, a sine wave is applied to the load.



PUSH-PULL CLASS 'D' OPERATION

If S1 and S2 are opened and closed with a 50% duty cycle, a square wave of current, at the switching frequency, is passed through the primary of the transformer and transformed to its secondary. If the filter is designed to pass the switching frequency, but attenuate its harmonics, a sine wave is applied to the load.



POWER MOSFET CLASS 'D' OPERATION

Power MOSFETs can be used to replace the switches as depicted in the simple class 'D' operation and push-pull class 'D' operation examples. Note that the switch contacts are replaced by the phase-oriented secondaries of an RF drive transformer. Q1 corresponds to S1-A, Q2 to S1-B, Q3 to S2-B and Q4 to S2-A, as depicted in the push-pull class 'D' operation example. Q1 and Q4 turn on/off together and Q2 and Q3 turn on/off together.

Figure 6-6 Simplified Principles of Class 'D' Operation

Vector LP Model Variants

The Vector LP NDB series transmitter is an amplitude modulated non-direction beacon operating in the 190 kHz to 535 kHz frequency band. The transmitter consists of a number of model variants; however, with the exception of a few optional items, the physical appearance, construction and operation of each model is the same. These optional items include a DC backup option and the duality of specific components.

Nautel's submission for FCC Type Approval pertains to the VR125 model of the Vector LP family. This includes model variants, the VR125S (Single Side System) and the VR125D (Dual Side System) and also includes the DC backup option.

The VR125 has a maximum operating power level of 125W (N0N, no modulation) or 187.5W (A2A, 100% modulation). A universal AC input allows the VR125 to operate from 90Vac to 270Vac supply, but it also has the option to operate from a 24Vdc or 48Vdc DC backup supply. The DC supply option consists of a battery boost assembly along with a DC/DC low voltage power supply. If installed, the transmitter will automatically switch to the DC backup option if the AC falls below a set threshold value. The Vectors switch mode power supply (SMPS), which uses the AC supply option, and the battery boost assembly, which uses the DC supply option, produce a high DC voltage at their output. These voltage's, which are identical between the two supply options, are OR'd together within the power module and then used by the modulator and power amplifier to produce RF power. At all times, the non operating supply option, either the SMPS or battery boost assembly, is inhibited so they both do not produce an output at the same time.

The VR125 can be broken down into a two model variants. These variants include a single side system, the VR125S or dual side system, the VR125D. The dual system includes a full standby side transmitter within the same transmitter assembly, so from the outside the appearance has not changed. The dual system includes a second, but identical; RF Synthesizer PWB, PDM Driver PWB, Exciter Monitor Generator PWB, Power Module and AC/DC low voltage power supply. In a single system these extra components are removed. The control software is identical between the single and dual system and thus the operation of each model variant is the same. The exception is that the dual system allows the transmitter to switch to the standby side in the event of failure on the main operating side.

In the dual side system, both the main operating side and standby side share the same Control PWB, Remote Interface PWB, Harmonic Filter PWB and Power Probe PWB, but the frequency generation and RF power generation is independent of each other. Also, dual monitoring allows each side to monitor the other side's operating parameters. In a dual side system, one side is always inhibited from operating via software controlled relays. When the transmitter switches to the standby side, these relays allow power to the standby side PWB's as well as connecting the standby side power module to the Harmonic Filter and Power Probe at the transmitter's output.

Due to the same physical construction, operation and software, the model variants of the Vector LP family are not considered discrete models on their own and any suffixes, such as "S" or "D", appearing at the end of the model name are for internal use only and do not appear on the model label affixed to the transmitter.