CHAPTER 2.0 HARDWARE THEORY OF OPERATION

2.1 Introduction

The radio contains three Circuit Card Assemblies (CCAs). The Control CCA and Keypad CCA are contained in the Chassis Assembly, and the Transceiver CCA which is attached to the rear panel. The CCAs are attached to each other and to other radio components through 32-pin, wire, and flexi connectors. Figure 2-1 contains the Guardian Interconnection diagram.

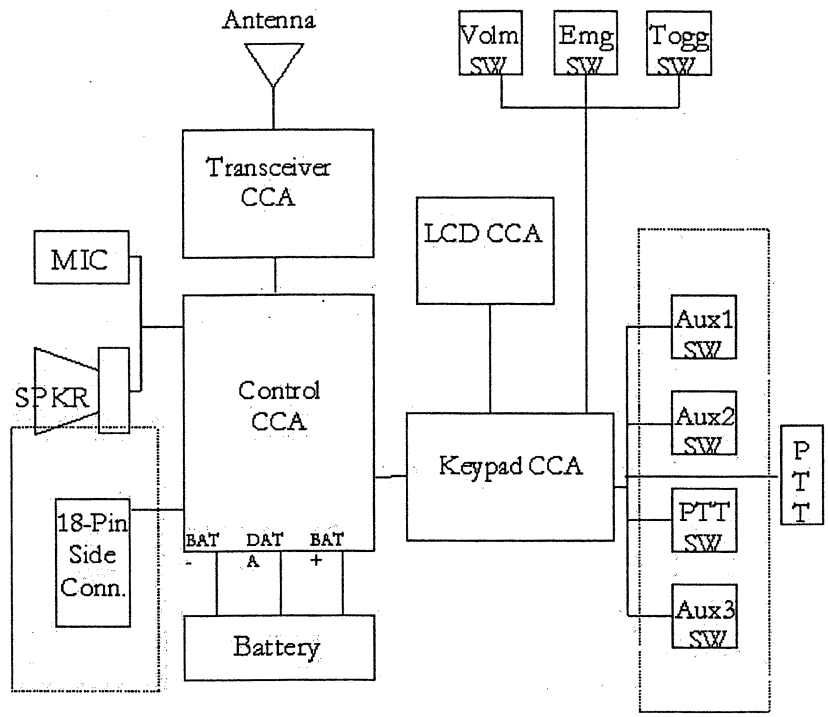

Figure 2-1 Guardian Interconnect Diagram

2.2 Control Board

The control board fits interfaces to the keypad board, transceiver board, internal audio, and side connector. The board implements the main radio control function and all the baseband signal processing. Figure 2-2 shows a block diagram of the Control Printed Circuit Board (PCB). The Control CCA schematic is contained in the schematic section at the back of this document

2.2.1 Power Supply Unit

This block of circuitry takes the raw battery supply voltage and the external power source from the side connector together with a number of control signals to generate a number of power supply outputs. Figure 2-3 shows a block diagram of the Power Supply Unit.

2.2.1.1 Battery/External Power Switching

This block of circuitry generates the 10V CONT supply from either the battery or external power source. In normal operation with a battery, the FPGA sets /BATOFF to connect the battery through to 10V CONT (at power-up the reverse path diode operates before BATOFF is set). In this mode of operation, power from the battery for external ancillaries is available when the radio is switched on through 500mA current limiter. In operation without a battery but with an external power source, power is routed from the external power source through to the 10V CONT line. This input is protected by an overvoltage detector, which switches off this path if the external voltage exceeds 16V.

In the situation where there is an external power source and a battery fitted, the H8 software detects the situation by sensing a battery through the battery serial bus and an external power source through the WRU line. In this situation the software then controls /BATOFF to prevent the external power source damaging the battery.

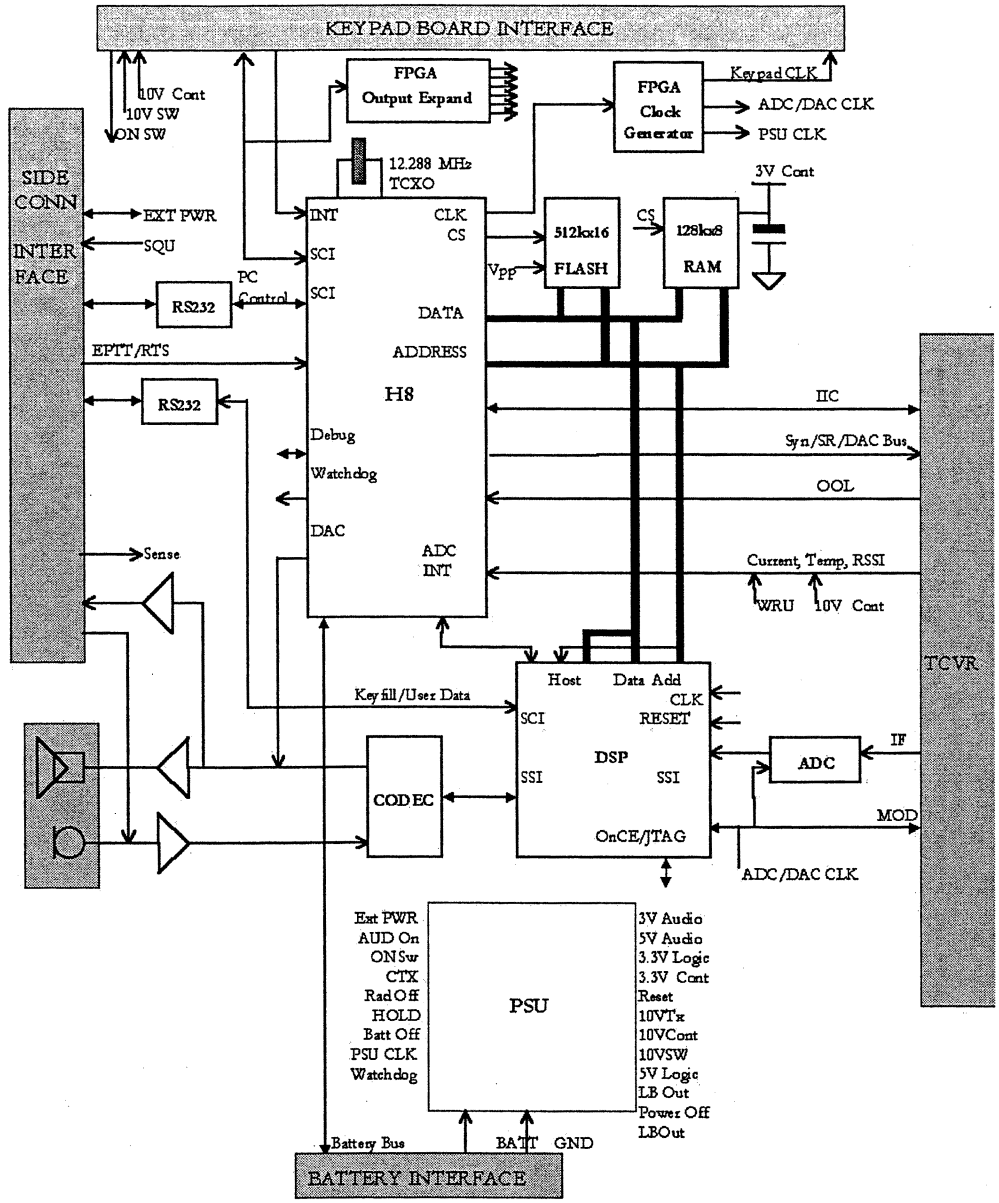

Figure 2-2 Guardian Control Board

2.2.1.2 On/Off Switching

The main continuous supply 10V CONT is passed through an on-off switch to generate 10V SW, the main radio supply. In normal operation with a battery the on/off switching is controlled by the radio on/off rotary switch by the control /RADON. Once switched on the main controller can hold the radio on by setting PWRHOLD. In addition to the radio rotary on/off switch, the on/off switching can be controlled by the external line /RADOFF. This line overrides the /RADON line and can be used to force the radio off regardless of the rotary switch setting. However, the PWRHOLD and PWROFF lines can be used by the H8 controller to implement a clean controlled switch off.

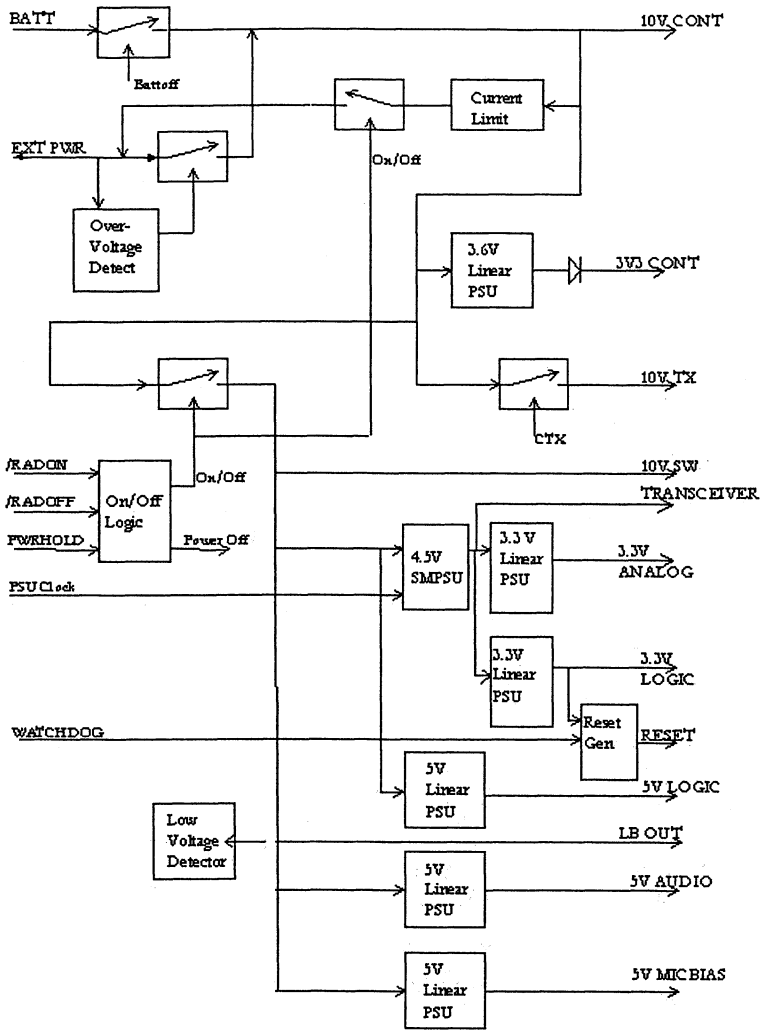

Figure 2-3 Guardian Power Supply

2.2.1.3 Transmit Power Switching

A single FET switch controlled by CTX is used to provide a switched 10VTX high current (1.5 Ampere) supply for the transmitter.

2.2.1.4 4.5V Switch Mode Power Supply

This circuit uses a switch mode power supply device to generate a 4.5 Volt (V) supply at 450 milliAmperes (mA) maximum for the radio logic. The switch mode device is synchronous and uses an externally provided power supply clock at 384kHz. The power supply circuit includes input and output filters to limit the conduction of the fundamental switching components and their harmonics in the VHF band both onwards into the logic and back into the battery.

2.2.1.5 3.3V Linear Logic Supply

The output from the 4.5V switch mode power supply is passed through 3.3V linear power supplies to remove any remaining power supply switching noise on the main logic supply. One 3.3V supply is used for control board logic, the other 3.3V, 50 mA supply is used for control board analog circuitry.

2.2.1.6 Reset Generator

This circuit uses a MPU supervisory device (MAX825) to generate a reset pulse of at least 140ms whenever the 3.3V logic supply drops below 3.08 volts. The circuit also generates a reset signal when the Watchdog input is asserted by the H8 or DSP.

2.2.1.7 5V Linear Logic Supply

This circuit generates a 5V logic supply at 50mA maximum for use on the control board.

2.2.1.8 3V Backup Supply

This circuit generates a 3.3V logic supply at 50mA maximum to power the RAM at all times when a power source is fitted regardless of the on/off switch setting.

2.2.1.9 Low Voltage Detector

This circuit controls the LBOUT output so that it changes state when the main supply drops below about 6V. This signal is used by the H8 controller to implement a clean shut down when the radio battery (or external power) is removed without switching off the radio.

2.2.1.10 Audio Supplies

Two linear regulators providing clean filtered supplies for the audio at 5V are provided. The 5V 800mA audio supply is used by the audio power amplifiers. The audio supply is used for the low current microphone amplifier. A linear 5V bias supply to the internal microphone is also provided.

2.2.1.11 H8 Microcontroller

This is the main controller for the radio, the device used is a HD6433044 ROM-less microcontroller. The H8 is configured with an expanded bus connected to the Flash, RAM, and DSP. The H8 integral bus arbitration logic is used to allow the H8 and DSP to both have access to the Flash and RAM. The H8 is clocked by the external TCXO.

The H8 is powered from the 3.3V logic supply, and reset by the hardware /RES line. A watchdog output to the hardware reset circuitry is provided. The H8 generates chip select outputs to allow the Flash, RAM, FPGA and DSP host port to be separately addressed.

One serial port of the H8 is used to implement a bi-directional synchronous serial interface to the keypad board. This interface is used to communicate with the keypad MPU and directly load the LCD controller. The clock on this interface is sourced by the H8 at c. 100kHz. An associated interrupt input to the H8 is used to initiate transfers from the keypad to the H8. This serial interface is also used to load the output expander in the FPGA, and also to configure the FPGA.

One serial port of the H8 is used to implement a bi-directional asynchronous serial interface to an external PC used for programming, fill and radio control. This interface uses programmable standard baud rates (default 9600 baud) and standard data formats. There are no handshaking parallel lines associated with this interface. Two parallel I/O lines on the H8 are used to generate an I^2C interface to allow the EEPROM on the transceiver board to be accessed. Four parallel output lines on the H8 are used to generate a synchronous serial output bus with clock and data and separate strobe lines for the DAC, control shift register and synthesizer on the transceiver board.

One parallel I/O line on the H8 is used to generate the bi-directional Pulse Width Modulation (PWM) serial bus used to interface to the smart battery. One H8 DAC output is used to generate simple audio tones of varying volume for use as audio alerts. The second H8 DAC output is available for VCTCXOP control. The six channel ADC is used to measure: the raw supply voltage; WRU radio input; reference crystal temperature; PA temperature; PA current; and RSSI. Two I/O lines are used to implement a software UART used for debug outputs in the development environment.

2.2.1.12 H8 Input Requirements

The total requirement for parallel input signals to the H8 which need to be polled on a regular basis are:

- OOL Out-of-Lock (OOL) signal from the transceiver synthesizer
- EXT PTT External PTT
- PWROFF On/off switch position
- CONFDONE Configuration status of FPGA

2.2.1.13 H8 Output Requirements

The total requirement for parallel output signals from the H8 which need to be controlled are as below, the output capabilities of the H8 are expanded by a serial load output latch in the FPGA.

- LCDA0 LCD controller A0 command/ data select
- LCDCS LCD chip select
- SCL I²C & synthesizer clock
- DACSDA Transceiver serial data, synthesizer, DAC, S-R.
- SYNTHENA Synthesizer Framing pulse
- DACENA DAC Framing pulse
- SRENA S-R Framing pulse
- /DINT Interrupt to DSP from H8
- /RESO Watchdog Output from H8

2.2.1.14 H8 Input/Output Requirements

The total requirement for parallel input/output signals on the H8 which need to be read and controlled are:

- BATBUS PWM input/out to smart battery
- SDA I²C data

2.2.1.15 H8 Input Interrupt Requirements

The total requirement for parallel input interrupt signals on the H8 are:

- LBOUT Low battery output
- DSPINT DSP Interrupt

2.2.2 DSP

The DSP56309 (or DSP56302) processor implements all baseband signal processing functions in the radio. It interfaces with the transceiver through one ESSI port, to the user for voice through the second ESSI port. The DSP function is controlled by the H8 through the DSP host port. The DSP has direct access to the main Flash memory through the bus arbitration logic in the H8, this allows it to download program images. The initial power-on code download is through the host port. The DSP is reset by the hardware reset line. The DSP is clocked by the TCXO clock output line at 12.288 MHz. The DSP ESSI 1 port is used to provide a synchronous interface to the IF ADC and the transceiver 12-bit DAC. In receive modes that interface is capable of writing to the DAC at 48 ksps while still reading the ADC at 96 ksps. The DSP ESSI 0 port is used to provide a full duplex synchronous interface to the audio CODEC using 8 kHz sampling rate and 13 bit samples. The data transfer is at 2.048 MHz using a DSP sourced clock and framing pulse.

2.2.3 Flash ROM

A 512k x16 Flash ROM is used as the main program store for the H8 controller and DSP. The Flash ROM uses a protected boot sector that is factory programmed via the DSP JTAG port. Normal reprogramming is implemented by running the H8 from the boot sector and using 3V, programming the bulk of the device. The Flash is used to provide a parameter storage area for non-volatile data storage of frequencies and keys etc. This storage area is capable of in excess of 100k write cycles.

2.2.4 RAM

A 128k x 8 static RAM is used for temporary storage of data by the H8 controller. This RAM is powered by a continuous supply that maintains its contents as long as a power source is present. Additionally the RAM has a backup capacitor to retain its contents over battery changes.

2.2.5 TCXO

This oscillator serves as the reference for all logic and power supply clocks within the control and keypad module. It provides the data rate clocks for radio operation, and is the source of the ADC/DAC/CODEC conversion clocks. The TCXO is at 12.288 MHz, with a temperature tolerance of $\pm$2.5 parts per million (ppm). Additional calibration is performed to provide a typical temperature tolerance of $\pm$ 1.0 ppm A trimmer to set the initial frequency is provided. The TCXO sine wave output is squared up by a Schmitt trigger buffer before being output to the H8 and DSP.

2.2.6 FPGA

The control board uses an Altera 8282 FPGA device to provide a flexible serial data routing function, I/O expansion for the H8 and DSP, clock generation, data multiplexing and to absorb discrete logic functions.

The synchronous serial bus routing function involves routing the synchronous serial port of the H8 either to the keypad and LCD or to the I/O expansion in the FPGA. This routing is controlled by high order address pins from the H8 and a FPGA dummy write with dedicated FPGA chip select from the H8. The FPGA includes a serial load parallel output shift register that is used for parallel output expansion for the H8.

The discrete logic functions of the FPGA, includes logic to control an inverter for one of the LCD control outputs. The data multiplexing function involves re-routing serial pins between the side connector and the DSP SCI port to allow data transmission and keyfill operations.

2.2.6.1 FPGA Configuration

The FPGA is configured at start-up from the main Flash memory using a serial load from the H8. During configuration outputs are tri-stated and pulled to a safe level by committing resistors to prevent audio and RF bursts at power up.

2.2.7 IF ADC

The IF sampling ADC is a 12 bit ADC capable of sub-sampling a 455kHz IF signal at 96kHz sampling rate. It is connected by a serial interface to the DSP ESSI port 1 The serial data interface is clocked at 1536kHz.

2.2.8 Clock Generation

The clock generation logic is used to generate clocks for the synchronous power supplies, the ADC serial interface and the keypad microcontroller. The clock generator logic is implemented in the FPGA.

2.2.9 Logic Audio CODEC

The Audio CODEC is an integrated ADC/DAC and audio filter device capable of full duplex operation on voice bandwidth signals at 8ksps. The samples have a resolution of 13 bits linear. The CODEC is connected to the DSP ESSI port 0 with serial data transfer rate of 2.048 MHz. The CODEC is continuously powered from the 3V logic and 3V audio supplies. Parallel control lines from the DSP is used to mute the input and output sections as required.

2.2.10 Side Connector Interface & Filtering

The side connector interface is implemented as a 20-pin ZIF flexi connector, 2 pins being redundant, yielding 18 contacts. All outputs are filtered to limit their bandwidth to the minimum and current limited to protect them from output short circuits to ground or up to 16V. All inputs are filtered and protected from continuous application of ground or +16V. There is no protection against negative applied voltages. Inputs and outputs are protected from static discharge of at least 10kV air discharge. All inputs and outputs incorporate RF bypass filter capacitors adjacent to the connector, except for ground.

2.2.11 Transceiver Interface & Filtering

The transceiver interface is implemented as a 32-pin interboard connector. Most of the signals crossing the interface are filtered to limit their bandwidth to the minimum consistent with correct operation. Outputs from the control

module are filtered with series resistors on the control module and grounded capacitors on the transceiver module adjacent to the connector. Outputs from the transceiver to the control use the reverse configuration.

2.2.12 Battery Interface & Filtering

The battery interface is implemented as a three-way flexi-circuit, which is fixed by two of the control board mounting screws. The positive power and smart battery connections incorporate RF bypass capacitors as close to the signal pins as possible mounted on the flexi circuit. Additionally, a series ferrite capable of carrying 2A peak is mounted on the flexi close to the main power pin.

2.2.13 Keypad Interface

The keypad interface uses a 18-pin interboard connector. The connector type is a 1.27mm pitch shrouded connector. Some filtering is provided on this interface, but all outputs are protected from short circuits by series resistors. Where possible, inputs are also protected from damage by series resistors.

2.2.14 Audio Interface

The audio interface is implemented with a four-way wire connector directly to the integral speaker and microphone.

2.2.15 Test Interface

The control board is provided with a 18-pin 1.27mm shrouded connector used for factory test. It provides the following functions:

- Joint Test Action group (JTAG) connector access for board test and Flash boot sector programming.
- Board reset and control access.
- Board power supply and on-off switching access.
- H8 serial debug port access.

2.2.16 LED

The control board incorporates a three-color LED used for status information. It is controlled by the FPGA to show red, green, or off. It is optically coupled to the top face of the radio by a light pipe. The hardware is configured such that during hardware reset before the keypad MPU software is running the LEDs are off.

2.2.17 Power Consumption

The control board operates at input voltage from 8V to 13V. Application of voltages above 16V may damage the unit. The mean current consumption of the control board is:

- Standby mode: ≈ 60 mA
- Receive mode @ 500 mW: ≈ 330 mA
- Transmit mode @ 2W: ≈ 1,000 mA
- Transmit mode @ 5W: ≈ 1,500 mA

2.3 Keypad Board

The keypad board is fixed directly into the chassis behind the keypad. The board incorporates the keypad electronics, the LCD interface, and backlights. The board interfaces with the main controller via a bi-directional synchronous serial interface. Figure 2-4 shows a block diagram of the keypad board. The Keypad CCA schematic is contained in the schematic section at the back of this document.

2.3.1 Keypad Microcontroller

The keypad board is controlled by a Atmel AVR4414 microcontroller. This is a flash Programmable device. The microcontroller implements these functions:

- Keypad scanning
- PTT switch input
- Auxiliary keys input
- Volume switch input
- Channel switch input
- Emergency switch input
- Synchronous bi-directional serial interface to main controller at 100 kHz
- Keypad and LCD backlight control

The keypad microcontroller is clocked by a clock derived from the main reference clock at 1.5 MHz. The keypad microcontroller is powered by the same 10V supply as the LCD driver device.

2.3.2 LCD Power Supply

The keypad board uses a locally generated 3.3V logic supply to power the AVR and LCD driver. This supply is a low current (<50mA) linear regulator operating off the main radio switched 10V supply.

2.3.3 Display

The radio display module is a full graphics 80x32 pixels LCD, requiring a temperature compensated differential driving voltage of about 12V and a 1/6 bias, 1/32 duty cycle driving scheme. It is driven by a LCD driver device (Seiko Epson SED 1530). This LCD driver has internal display RAM and copes with all the display refreshing autonomously. Display data transfers from the main controller are only required when the display is changed, selective display RAM updates are also available to minimize serial traffic. The LCD driver display RAM is accessed through a one way synchronous serial interface, connected in parallel with the AVR serial port. The LCD CS input is used to differentiate between serial data for the LCD driver and

The display driver is reset by the keypad board hardware reset line. The hardware is configured such that during hardware reset before serial LCD data is presented the LCD is blank.

2.3.4 Keypad

The radio keypad consists of 16 conductive rubber keys, which contact onto switch contacts on the rear of the keypad board. Each key is provided with an LED backlight.

2.3.5 Backlighting

Simultaneous backlighting of both the LCD and keypad is provided. The backlighting is controlled by the AVR so that it can be turned off or set to one of two brightness levels. Brightness control is by series resistor switching, not by duty cycle control. The hardware is configured such that during hardware reset before the keypad MPU software is running, the backlights are off.

2.3.6 Switch Interface

An interface to the top face switches and the side mounted PTT and Auxiliary switches is provided. This interface is implemented using surface mount ZIF flexi connectors on the keypad board. The connections to the side switches and PTT are by a separate flexi connector.

- Top SW Interface
- Switch common (earth)
- Volume switch outputs (4)
- Channel switch outputs (4)
- Toggle switch outputs (2)
- Emergency switch output
- Side SW Interface
- AUX keys (3)

- PTT
- Switch common

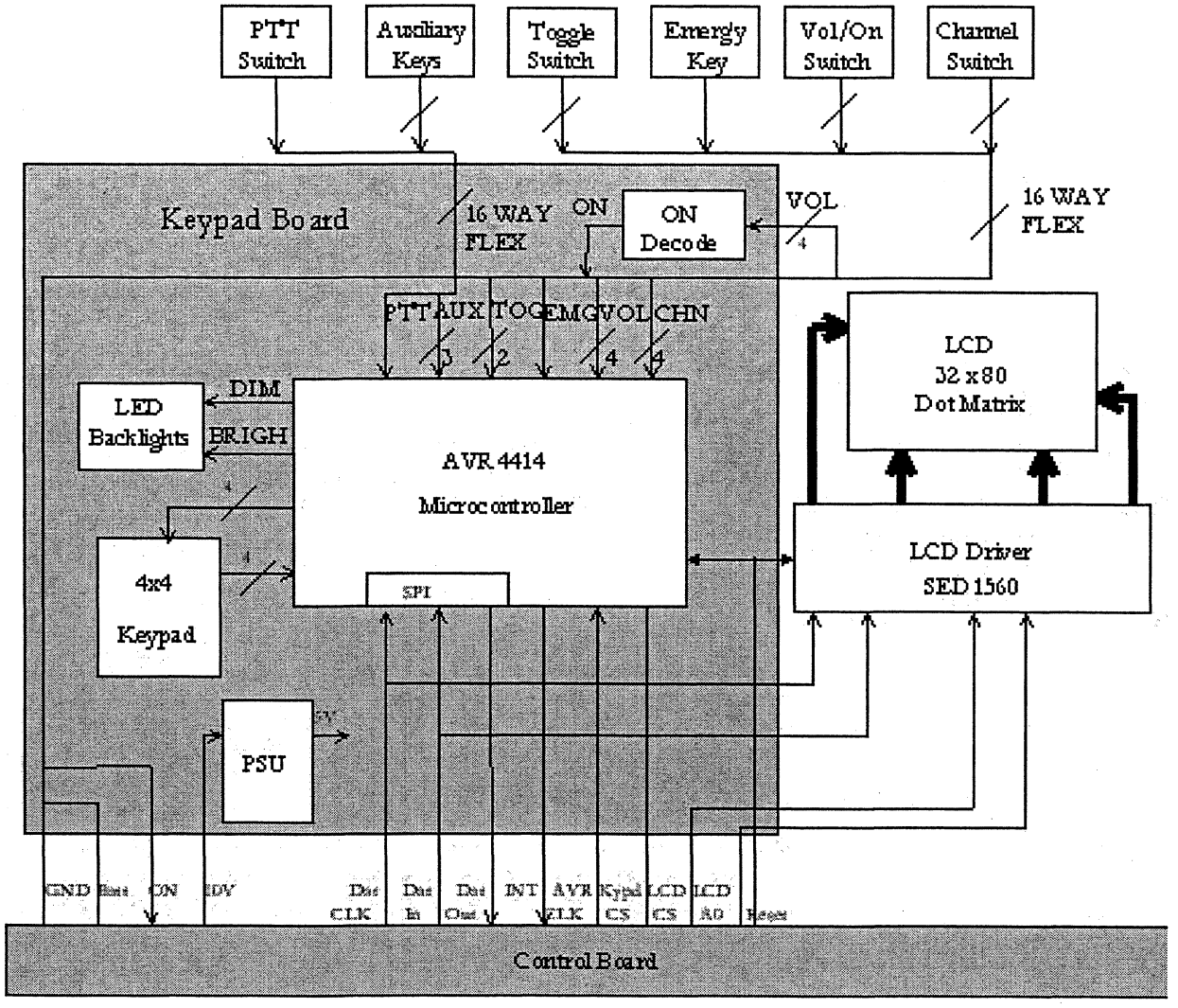

Figure 2-4 Guardian Keypad Board

2.3.7 Control Board Interface

A 18-pin interboard connector is used to implement the interface to the main control board. The signals on this interface need not be filtered, but are protected from short circuits to ground. All logic signals are at 0-3V Complimentary Metal-Oxide Semiconductor (CMOS) levels at the interface. The interface carries the following functions:

- 10VCONT
- Ground
- /RADON
- Switched 10V supply
- Reset
- AVR Clock
- Serial Data Clock
- Serial Data Input
- Serial Data Output

- Key Interrupt
- LCD Chip Select
- LCD A0 (Data \ command select)
- Keypad Chip Select

2.3.8 Power Consumption

The total mean power consumption of the Keypad board in normal operation with the LCD on but the backlight and indicator off, is less than 4mA from the switched 10V supply.

2.4 Transceiver

The circuit card assembly (CCA) is covered by RF shields on the front side and by the partitioned battery bracket on the rear side. The Transceiver CCA schematic is contained in the schematic section at the back of this document

2.4.1 Interface Section

The Interface Section schematic is page 1 of the Transceiver CCA schematic enclosed in the back of this document. J1 is the 32-pin surface-mount transceiver interface connector. The transceiver is powered, controlled, and monitored through this port. The pin names and functions are delineated in the Chapter 9.

J2 is the transceiver antenna connector. RF signals are transmitted and received through this surface mount RF connector. Transmitted and received RF signals are routed from this connector through a short RF cable to the antenna of the radio. J4 is the "455 kHz IF OUT MONITOR" connector. The 455 kHz IF is available for monitoring purposes through this surface mount RF connector when the transceiver is in the receive mode of operation. It is intended for test and troubleshooting purposes only.

2.4.2 Transmitter Section

The Transmitter Section schematic is page 4 of the Transceiver CCA schematic enclosed in the back of this document.

2.4.2.1 Transmit Chain

The pre-driver amplifier (Q7, etc.) amplifies the "TXLO" signal from the synthesizer section. The Q7 output power is typically 13 decibel milliwatt (dBm) measured at C77/R44/ R49 node.

R44, R49, and R52 is a 3 decibel (dB) pie attenuator network. The PIN attenuator circuit is made up of CR5, CR6, and associated components. This circuit yields more than 50 dB of useful attenuation range. The circuit is part of a DAC controlled closed loop system, in conjunction with the detector/power control circuit (U12, U13, and associated components), which controls the transmitter output power level. The Power Amplifier (PA) driver amplifier (Q5, Q8, etc.) utilizes an NPN transistor stage biased class A. Q5 provides an active bias to Q8. The collector current of Q8 is 100 mA typically. The Q8 output power is typically 24 dBm measured at C76/C80/T3-1 node.

The PA (Q6, Q9, etc.) uses a pair of MOSFET power transistors configured as a push-pull power amplifier. The power transistor gates are biased via DAC output lines "PABIAS1" and "PABIAS2" through 10 K ohm resistors R42 and R43. Each transistor is biased for 100 mA of quiescent current. The PA full output power is typically 38.5 dBm measured at the T4-5 C209 node.

The PA temperature sensor (U11) is a thermistor Integrated Circuit (IC) fitted in close proximity to the power amplifier circuit. Under normal operating conditions, the line labeled "PATEMP" is closely monitored by the microprocessor. In the unlikely event of overheating, the transmitter would be disabled to prevent damage to the power transistors.

The harmonic filter (C209, L30, C81, C82, L31, C83, and C84) attenuates harmonics created by the power amplifier. The harmonic filter insertion loss is 0.4 dB typically at 174 MHz. The output of the harmonic filter connects to the 20 dB coupler (U12). This coupler is part of a DAC-controlled closed loop system designed to set the transmitter output power level. The insertion loss through the coupler (U12-1 to U12-3) is 0.2 dB typically.

2.4.2.2 Power Amplifier Control

Transmit output power level is controlled by the Detector/Power Control circuit and the PIN Attenuator (discussed previously) circuit via "VCONTROL." This closed loop system is designed to keep the transmitter output power constant over variations in temperature, transmitter supply voltage ("10VT"), and RF power levels into the transmit chain. The detector/power control circuit is made up of the 20 dB coupler (U12), an RF rectifier circuit (CR11, CR12, etc.), and an integrator (U13). The DAC line labeled "PWRSET" at the non-inverting input of U13 sets the transmitter to the desired power level. U12-2 "samples" the transmit signal. The sampled RF signal is rectified by the temperature stable circuitry of CR11,CR12, etc, and is routed to the inverting input of the integrator at U13-4. The output of the integrator at U13-1, labeled "VCONTROL", controls the PIN attenuator circuit. Any change in transmitter output power level is automatically corrected by the loop.

2.4.2.3 PIN Diode Switch

The antenna PIN diode switch is made up of CR7, CR8, CR9, CR10, and other associated components. This switch is a four-port design. The four ports are Antenna 1 ("TOP RF"), Antenna 2 ("SIDE RF"), receive, and transmit. Receive and transmit ports can be switched to only one of the two antenna ports. Transmit signals are routed from the transmit/receive PIN diode switch (to be discussed in the following paragraph) to the antenna port. The receive signal is routed from the selected antenna port to the transmit/receive PIN diode switch. The antenna PIN diode switch and receiver circuits "share" current in the receive mode of operation via the signal labeled "RXSINK" at Q11 pin 3. This approach conserves battery power. The insertion loss through the antenna pin switch is 0.2 dB typically.

The transmit/receive PIN diode switch is made up of C127, CR13, C114, L42, C115, CR14, C116 and other associated components. C127, C114, L42, and C115 is the 1/4 wave simulator circuit. The 1/4 wave simulator is critical to the design of the switch. In the transmit mode of operation CR13 and CR14 are forward biased. C116 resonates with the internal series inductance of CR14 at 155 MHz and the receive port ("RX INPUT") is RF shorted to ground. With the receive port RF shorted to ground, the parallel combination of C127, C114, and L42 forms a tank circuit resonating at 155 MHz. Consequently, the receive port appears as an open circuit to the transmit signal and is routed to the antenna PIN diode switch. In the receive mode of operation, CR13 and CR14 are biased off so C114/L42/C115 appears as a Low-Pass Filter (LPF) to signals at the antenna port of the switch. The insertion loss through the transmit/receive PIN diode switch is 0.4 dB in the transmit mode and 0.2 dB in the receive mode typically.

Q10-Q19 and associated components are switching transistors used to control the antenna and transmit/ receive PIN diode switches. The current flowing through the entire PIN diode circuit is approximately 45 mA in the transmit mode of operation. In the receive mode of operation the transmit/receive PIN diode switch is disabled, and approximately 85 mA flows through the antenna PIN diode switch.

2.4.3 Receiver Section

The Receiver Section schematic is page 2 of the Transceiver CCA schematic enclosed in the back of this document. The VHF signal enters into the "RX INPUT" via the PIN diode switch (discussed previously). CR1 and CR2 are schottky protection diodes to protect the front end circuitry from RF overloads that could occur if the PIN diode switch failed to work properly or if a transmitter is very close to a receiver. Typical insertion loss is 0.1 dB for the protection diodes. L25/C61 form a Band-Stop Filter (BSF) at the first IF frequency of 45 MHz. Typical insertion loss for the BSF is 15 dB at 45 MHz but less than 0.1 dB in the VHF band.

L14, L6, CR3, CR4, L7, CR27, CR28, L8, and L15 make up the Very High Frequency (VHF) preselector Band-Pass Filter (BPF). The BPF is inductively coupled for improved high side attenuation. This filter provides attenuation to spurious signals such as the first image and the half-IF. The BPF is varactor diode tuned by DAC line "RXVTF." Typical insertion loss (138-174 MHz) is 1 dB for the VHF BPF.

The RF Amplifier (Q1, T1, etc.) utilizes "loss-less feedback" to deliver reasonable gain, low noise figure and a high third order intercept point simultaneously. Typical gain (136-174 MHz) is 11.5 dB for the RF Amplifier.

C14, L1, C9, C15, L2, C10, C16, L3, C11, C17, and L9 form a VHF LPF. This filter provides additional RX spurious attenuation as well as image noise attenuation. L4, C12, L16, C25, L5, and C13 form a BSF at the first IF

frequency of 45 MHz. The insertion loss is 1.0 - 2.0 dB (136-174 MHz) typically for the cascade. The IF BSF insertion loss is typically 40 dB at 45 MHz but less than 0.3 dB in the VHF band.

U1 is a double-balanced mixer (DBM). U1 converts the desired RF signal down to the first IF of 45 MHz. High-side Local Oscillator (LO) injection is used. Therefore, the LO is 45 MHz higher than the receiver tuned frequency. The LO drive level is +10 dBm nominal at U1, pin 1. The conversion loss of the mixer (RF to IF) is 5.5 dB typically.

The LO signal is generated in the synthesizer section (to be discussed later). The LO signal is designated "RXLO" on the schematic diagram. The LO signal is routed to a LPF consisting of C31, L21, C87, C30, L20, C75, and C28. L19 and C28 are also used to impedance match the LO port of the mixer. The insertion loss of the VHF LO LPF is 0.3 dB typically at 174 MHz.

R4, L17, C6, L10, R5, and C23 make up the diplexer network. This network properly terminates the DBM both in and out of band. The diplexer also provides some additional half-IF spurious rejection. The diplexer insertion loss is 0.8 dB typically at 45 MHz.

There are two 45 MHz IF Amplifier circuits. The first (Q2, T2, etc.) utilizes "loss-less feedback" to deliver reasonable gain, low noise figure and a high third order intercept point simultaneously. The second 45 MHz IF Amplifier will be discussed later. Typical gain is 10.5 dB for the first IF Amplifier.

There are two crystal BPFs and a second 45 MHz IF Amplifier. The BPFs provide attenuation for the adjacent and alternate channels, and also for the second image response. FL1 is a four-pole crystal filter with a 20 kHz bandwidth centered at 45 MHz. FL4 is a two-pole crystal filter with a 30 kHz bandwidth centered at 45 MHz. The second 45 MHz IF Amplifier provides high gain to prevent further degradation of receive sensitivity. C57, L12, C18, C19, and L13 are impedance matching elements for the input of FL1. The output of FL1 is impedance matched to the second 45 MHz IF Amplifier (Q36, etc.) by C285, L64, and C242.

The output of the second 45 MHz IF Amplifier is impedance matched to FL4 by C287, L61, C286, C237, L60, and C235. The entire cascade provides 21 dB of gain and has a 3 dB bandwidth of 20 kHz typically. Typical insertion loss is 1.5 dB for each crystal BPF.

The IF IC (U28) contains the second mixer and an IF amplifier chain. The 45 MHz IF signal enters U28 at pin 6 from the crystal BPF (FL4). FL4 is impedance matched to the IF IC input by C294, L62, and C288. The incoming 45 MHz IF signal is mixed with the second LO (to be discussed later). The second mixer IF output is at U28 pin 8 and the second IF frequency is 455 kHz.

The signal from U28-8 is routed to FL3. FL3 is a ceramic BPF operating at 455 kHz. The insertion loss of the ceramic BPF is 6 dB typically in a 1500 ohm system.

The 455 kHz IF signal enters U28-10, is amplified by a cascade of IF amplifiers, and exits at U28-14. The signal from U28-14 then enters a second ceramic BPF, FL2. FL2 is the final ceramic BPF with a typical insertion loss of 8 dB in a 1000 ohm system. The 455 kHz IF signal enters its final stage of amplification at U29-3. U29 is configured as a non-inverting operational amplifier and is capable of driving a 50 ohm load. The amplifier is set for a voltage gain of 2.5. With the receiver set to full gain the signal level at J4 (455 kHz IF OUT MONITOR) is -20 dBm ∀ 3 dB into 50 ohms with a -119 dBm unmodulated 136 MHz signal injected at J2 (TOP RF) or J3 (SIDE RF). The second LO consists of CR26, R33, Y1, L24, C59, C226, C227, and Q35. The oscillator is a Colpitts type with the crystal operating in the series mode. CR24 is a varactor diode used to set the oscillator on frequency using the DAC output labeled "2ndLO." The second LO operating frequency is 44.545 MHz (low side injection). L65 and C223 impedance match the output of Q35 to the LPF (C289, C293, L63, and C284). The signal is then attenuated by R282, R283, and R284 and sent on to the second mixer. The signal level at U28-4 is -16 dBm nominal.

U4 is a voltage regulator used to power the receiver circuits. The DC voltage appearing at U4 pin 1, labeled "RXSINK" on the schematic diagram, is routed from the antenna PIN diode switch. As previously discussed, the PIN diode switch and the receiver circuits *"share"* current to reduce receive power consumption. The control line "+3.3V RXEN" is used to enable the regulator while the transceiver is in the receive mode of operation. The regulator is disabled during the transmit mode of operation.

2.4.4 Synthesizer Section

The Transceiver Section schematic is page 3 of the Transceiver CCA schematic enclosed in the back of this document.

2.4.4.1 Synthesizer and Reference Oscillator

U19 is a fractional-N synthesizer IC programmed for a specific frequency by loading appropriate serial data into the IC. It controls the receive VCO when the transceiver is in the receive mode of operation, and the transmit VCO when in the transmit mode. The programming lines are labeled "3VSCL", "3VSDA" and "3VSYNTHENA" on the schematic diagram. These are all CMOS logic level inputs. R118 (RF) and R123 (RN) are the fractional compensation and phase detector current setting resistors, respectively. These resistors are critical to the operation of the synthesizer system and must be checked when troubleshooting around U19. The phase detector output pins (U19-13 and U19-14) are fed to the passive loop filter (R140, C177, C172, R134, and C173) and then on to the VCO control varactor diodes (CR17/CR19) for frequency control. The buffered, filtered output from the VCO is fed into U19-5 (RF IN) to close the phase locked loop. The level is typically -10 dBm into U19-5. The reference oscillator is made up of CR22, Y2, Q28, C197, and C198 and associated components. The reference oscillator operates at 12.8 MHz. The reference oscillator operating frequency is adjusted by varying the DC voltage at the DAC controlled line that is labeled "REFOSCMOD." This line is also used to modulate the reference oscillator during the transceiver's transmit mode of operation. The 12.8 MHz signal is fed into the synthesizer chip at U19-8 (REF IN) using a coupling capacitor, C194. The AC signal level at U19-8 is 1 Volt, peak to peak (Vp-p) typically.

U22 is the reference oscillator temperature sensor used to monitor the temperature near Y2. It's output is labeled "XTALTEMP" on the schematic diagram. This line is normally monitored by the microprocessor so the reference oscillator can be adjusted for drift due to changes in temperature.

2.4.4.2 Receive/Transmit VCOs and Buffer Amplifiers

The receive VCO operates from 181-219 MHz since high side LO injection is used and the first IF is 45 MHz. The transmit VCO operates from 136-174 MHz. Each VCO is a Colpitts type design utilizing a low noise, bipolar transistor as the active device. The receive VCO uses Q24 and the transmit VCO uses Q21, each in the common collector configuration. The Colpitts capacitors are C169/C180 (receive VCO), and C137/C142 (transmit VCO). These capacitors enable Q24 to oscillate in the

181-219 MHz frequency range and Q21 to oscillate in the 136-174 MHz frequency range. L53 is the resonating inductor for the receive VCO and L45/L46 are the resonating inductors for the transmit VCO. CR20/CR21, and CR16/CR18 are the coarse tuning varactor diodes for the receive and transmit VCO respectively. These diodes are used to coarse tune the VCO such that the LPF, phase detector output voltage (from U19) at TP10 equals 1.65 VDC. The receive and transmit VCOs share the coarse tuning DAC controlled line labeled "CTUNE". Coarse tune DC voltage swings from approximately 1.8-22 VDC. CR19 (receive VCO) and CR17 (transmit VCO) are the fine tuning varactor diodes controlled by U19 as was explained previously. CR15 is the modulation varactor diode for the transmit VCO. The output from the receive VCO is coupled off Q24-E using C174. The output from the transmit VCO is coupled off Q21-E using C139. The signal should be measured at the C174/R146 node (receive) and the C139/R107 node (transmit), and measures -15 dBm typically.

Q26 and Q22, and associated components, form the first VCO receive and transmit buffer amplifiers respectively. These amplifiers buffer the VCO output from changing-output Voltage Standing Wave Ratios (VSWR) that could "pull" the VCO off frequency. The output from each measures -5 dBm typically. The buffer should be measured at the C170/R141 node (receive) and the C138/R131 node (transmit).Q25 is the second buffer amplifier. This amplifier is common to both the receive and the transmit VCOs. R131, R141, and R142 are the combining elements used to make this possible. This buffer outputs a signal large enough, after subsequent attenuation and filtering, to properly drive the RF IN pin of the synthesizer (U19-5). The output from this buffer should be measured at the C167/C53/L52/C175 node and measures 0 dBm typically.

The output from the Q25 buffer is filtered by C175, C53, L52, and C176. This LPF prevents the synthesizer IC (U19) from "locking on" to harmonics of the desired frequency. The insertion loss of the LPF is 0.4 dB typically.

The signal is then split by R138, R139, and R144, and sent on to the appropriate receive or transmit final buffer amplifier. The signal measured at R139/C150/ C186 node is -6 dBm, and the signal measured at R144/R143/C168 node is -6 dBm.

Q23 (receive) and Q27 (transmit) is the final buffer amplifier. Q23 amplifies the signal up to the level needed to properly drive the LO port of the DBM (discussed previously). Q27 amplifies the signal up to the level needed to properly drive the PA pre-driver (previously discussed). The signal measured at "RXLO" is +7 dBm typically. The signal measured at "TXLO" is +7 dBm typically.

U17, Q20, etc. form the voltage regulator for the receive and transmit VCO/Buffer amplifiers. R67, C124, and Q20 form a "super filter" which attenuates voltage regulator noise that may otherwise degrade the synthesizer phase noise performance.

U20, U21, Q29, Q30, CR23, CR24, CR35, C199, C202, C203, etc. create a voltage multiplier. The circuit is configured as a voltage quadrupler. Circuit losses and output loading lower the voltage down from 24 VDC to about 22 VDC. The driver circuit (U21) switches at about 192 kHz. This frequency was selected so harmonics would not land at or near the second IF frequency of 455 kHz. The 22 VDC supply is used to power the DAC supporting quad op-amp U18.

The shift register (U24) is used to control transceiver modes of operation and functions. The line labeled "STD/SIDE" selects the desired antenna port of the transceiver. The line labeled "TX/RX" selects either the transmit or receive mode of operation. "+3.3V RXEN" turns the receiver on and off (previously discussed). Q34/Q32 and Q33/Q31 enable and disable the receive and transmit VCOs and buffers respectively (discussed previously). U16 is the voltage regulator that supplies all 5V digital circuitry on the transceiver board.

2.4.5 Digital/Analog Control

Digital/Analog Control is shown on page 1 of the Transceiver CCA schematic enclosed in the back of this document. The transceiver board is fitted with an EEPROM (U15) (see page 4 of the schematic diagram). The IC is used to store calibration and "curve fit" data which is needed when the transceiver is configured with the Guardian radio. Each transceiver has it's calibration and "curve fit" data stored within the EEPROM. The calibration and "curve fit" data is written to the EEPROM at the successful conclusion of level 2 testing. Two quad eight bit serial DACs, a quad twelve bit serial DAC, and supporting operational-amplifiers (U2, U6, U13, U18, and U30) control much of the transceiver, as has been discussed previously. U32 is a 2.5 VDC reference used by the Quad twelve bit DAC and the variable IF attenuator (discussed previously).

U18D and associated components amplifies the DC signal supplied by U31-3.

As was discussed previously, "REFOSCMOD" is the DC signal, which varies the operating frequency of the reference oscillator. Normally under DSP and microprocessor control, this line is used to FM modulate the reference oscillator which in turn FM modulates the RF carrier in transmit mode. This line is used to temperature compensate the reference oscillator as well.

The DAC controlled line "TXVCOMOD" at U31-4 is transmit data normally controlled by DSP and a microprocessor. This signal is routed to U18C and associated components (see page 5 on the schematic diagram). U18C and associated components form an active LPF/attenuator to shape the transmit data before modulating the RF carrier in the transmit mode. The cutoff frequency of the LPF occurs at 20 kHz. The 1 kHz peak to peak signal level at the active LPF output (U18-8) is one fourth "TXVCOMOD" at 2.5 VDC.

The synthesizer reference oscillator and the transmit VCO are simultaneously modulated to balance the FM modulation. We refer to this technique as "two point modulation". The DAC values required to balance the modulation are dependent on RF frequency.

The DC signal at U31-17 is routed to U30 and associated components. This op-amp is configured for a voltage gain of 2. The DC signal "VATT" controls the variable IF attenuator (discussed previously) in the receiver chain. Under DSP and microprocessor control, the attenuator is normally set for a desired amount of attenuation by this DAC controlled signal.

Q37, Q38, Q39, Q40, Q41, and associated components are used to enable and disable the 14 dB step attenuator in the receiver chain (discussed previously). Normally under DSP and microprocessor control, the attenuator is set to

the desired state of operation via U31-13. A logic level "1" at this pin enables the attenuator. Conversely, a logic level "0" at this pin disables the attenuator (bypass mode).

U18B and associated components amplifies the DC signal supplied by U33-2. As discussed previously, "CTUNE" is the DC signal which coarse tunes the receive and transmit VCOs. Under microprocessor control, the appropriate VCO is normally coarse tuned to a desired frequency based on "curve fit" data stored in the EEPROM (U15). "Curve fit" data is obtained and stored in the EEPROM during coarse tune calibration procedures performed at level two testing.

The DAC controlled DC signal "2ndLO" sets the 2nd LO (discussed previously) on frequency at 44.545 MHz. Normally under microprocessor control, the 2nd LO is set on frequency based on a DAC value stored in the EEPROM (U15). The correct DAC value is obtained and stored in the EEPROM during the 2nd LO calibration procedure at level 2 testing.

The DAC controlled DC signal "RXVTF" appropriately sets the varactor tuned BPF (discussed previously) based on the receiver tuned frequency. Normally under microprocessor control, the varactor tuned BPF is set based on "curve fit" data stored in the EEPROM (U15). The "curve fit" is based on statistical data obtained during the testing of hundreds of units.

The DAC controlled DC signal "PWRSET" sets the power amplifier (discussed previously) to a desired power level. Normally under microprocessor control, the power amplifier is set to the desired level based on "curve fit" data stored in the EEPROM (U15). The "curve fit" data is obtained and stored in the EEPROM during transmit power calibration procedures at level 2 testing. The power calibration procedure obtains "curve fit" data for five power level settings (0.1, 0.5, 1.0, 2.0, and 5.0 watts) over the entire transmitter operating frequency range (136-174 MHz).

The DAC controlled DC signals "PA1" and "PA2" set the gate bias for each power transistor (Q6 and Q9 respectively) in the power amplifier circuit (discussed previously). These two signals are routed to op-amps U2 and U6 (see page 4 of the schematic diagram) which are configured for a voltage gain of 2. The outputs at U2-1 and U6-1, labeled "PABIAS1" and "PABIAS2" respectively, are then routed to the gates of the power transistors. The correct DAC values for the bias current are stored in the EEPROM (U15). The correct DAC value is obtained and stored in the EEPROM during the power amplifier bias calibration procedure at level 2 testing. Each gate is biased such that 100 mA of current flows through each power transistor with "PWRSET" set to a DAC value of zero in the transmit mode. Level 2 software monitors the U10 output line labeled "IMONITOR" (see page 4 of the schematic diagram) when calibrating PA bias.

2.5 External Interfaces

The external interfaces of the radio are described as follows.

2.5.1 Side Connector

The Side Connector will be used for PC Programming, including keyfill; cloning; and audio accessory connection. It uses 18 flush-mounted electrical contacts in a non-conductive molding. Pin assignments and functions are delineated at Chapter 9.

2.5.2 Battery Connector

The battery interfaces with the radio through a reliable, long-wearing, connector.

2.5.3 Antenna Connector

The antennas screw into an SMA connector mounted on the top rightmost corner of the radio (as viewed from the front of the radio).