G25AMK005

GUARDIAN 110W MOBILE RADIO

TECHNICAL MANUAL

Datron World Communications Inc.
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Guardian™ Technical Manual for use with the Guardian 110W mobile radio.

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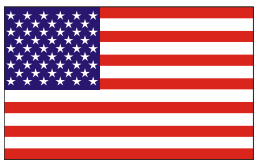

Made in the USA

NOTICE TO USER

WARNING! Maintain a distance of at least 3 feet (1 meter) between the antenna and people.

To satisfy RF exposure compliance, you, as a qualified user of this radio device must control the exposure conditions of bystanders to ensure the minimum distance is maintained between the antenna and nearby persons. The operation of this transmitter must satisfy the requirements of the Occupational/Controlled Exposure Environment for work-related use. Transmit only when people are at least the minimum distance from the properly installed, externally mounted antenna.

This radio is designed for initial setup by authorized technicians using a computer and the Guardian™ programming software. Programming can enable or disable many of the radio's features from user access per user agency security policy and legal restrictions. All, some, or none of the features and functions described in this manual may be available to the user. To successfully operate the radio, it is important to understand how the radio is programmed prior to issuance by the user agency. Consult authorized agency personnel for features and functions made available or restricted to the user. FCC licensees are prohibited by federal law from enabling the radio to directly enter transmit frequencies using the radio's controls.

NOTICE TO INSTALLATION TECHNICIANS

Use only a manufacturer- or dealer-supplied antenna.

Antenna minimum safe distance: 3 feet (1 meter).

The Federal Communications Commission (FCC) has adopted a safety standard for human exposure to Radio Frequency (RF) energy that is below the Occupational Safety and Health Act (OSHA) limits.

Antenna mounting: The antenna supplied by the manufacturer or radio dealer must be mounted at a location so that during radio transmission people cannot come closer than the minimum safe distance to the antenna, i.e., 3 feet (1 meter).

To comply with current FCC RF exposure limits, the antenna must be installed at or exceeding the minimum safe distance, and in accordance with the requirements of the antenna manufacturer or supplier.

Base station installation: The antenna should be fixed-mounted on an outdoor permanent structure. Address RF exposure compliance at the time of installation.

Antenna substitution: Do not substitute any antenna for the one supplied or recommended by the manufacturer or radio dealer. You may be exposing people to harmful RF radiation. Contact your radio dealer or manufacturer for further instructions.

CONTENTS

FIGURES

CHAPTER 1: GENERAL INFORMATION

1.1 Scope

This manual provides technical information for the Guardian 110 Watt mobile radio system.. This chapter gives a general description and provides a system block diagram. Chapters 2 and 3 provided detailed theory of operation for hardware and software portions of the radio. Chapter 4 provides general operation of the radio. Chapter 5 is the physical description of the radio components and the available accessories. Chapters 6 and 7 describe servicing, testing, and troubleshooting the radio system. The remaining chapters provide additional technical information and schematics.

1.2 General Description

The Guardian 110W mobile radio system is compliant with the APCO project 25 FDMA common air interface, and is also compatible with conventional wideband FM systems and newer narrowband FM systems. It provides fully digital encrypted communication suitable for use by modern public safety and commercial users. The radio system is built from a remote power amplifier and a control head. The 110W RF power amplifier mounts in a remote location such as a vehicle trunk, while the control unit is mounted in the cabin. The two are connected by a single coaxial cable. The cable carries both the RF signal and control signals (PTT, and power level setting).

1.3 Performance Specifications

Model Designation	**Guardian VHF Mobile Radio**
General	Model G25RMV110
Frequency Range	136.000 to 174.000 MHz
Banks, Zones, Channels, Shadow	4 banks, 16 zones, 256 channels, 7 shadow
Voice Digital Mode Voice Coding Frame Re-sync Interval Error Correction Method	IMBE™ 4.4 kb 180 msec RS, golay, hamming
Input Voltage	13.6 Vdc, negative chassis ground
Current Drain @ 13.8V: Standby Receive @ Rated Audio Transmit @ Rated Power	0.5A 3.0A 28.0A
Mounting	Dashboard mounted, including bracket
Dimensions	2.75” x 7.1” x 5.5” (H x W x D)
Weight Control Head Remote Unit	 2.5 lb 12 lb
Case	Metal and plastic
Temperature Range	-30° to +60°C
Channel Spacing	12.5 and 25 kHz, selectable in 2.5 or 3.125 kHz steps
FCC Type Acceptance Number	Pending
Industry Canada	Pending

Model Designation	Guardian VHF Mobile Radio
Receiver (Measurements per TIA/EIA 603 Standards)	
Sensitivity Digital Mode: 5% BER Analog Mode: 12 dB SINAD	-116 dBm or greater
Spurious	-70 dB
Intermodulation	-70 dB
Audio Output Power	10W, 4Ω external, 5W, 8Ω internal speaker
Audio Distortion (at 1000 Hz)	3%
Frequency Stability (-30° to 60°C)	± 1 ppm
Maximum Frequency Separation	Full-band split
Transmitter (Measurements per TIA/EIA 603 Standards)	
RF Power Output	25W to 110W, adjustable
Spurious and Harmonic Emissions	-70 dB
FM Hum and Noise (wideband)	-46 dB @ 25 kHz/-40 dB @ 12.5 kHz
FCC Modulation Designators	16K0F3E, 11K0F3E, 20K0F1E
Audio Distortion (at 1000 Hz)	2%
Audio Response (1000 Hz Ref.)	± 3 dB, 300 to 3000 (EIA/TIA 603)
Frequency Stability (-30°C to 60°C)	± 2.5 ppm
Maximum Frequency Separation	Full bandwidth

Environment Specifications (MIL-SPEC)						
Environment	**810C**	**810D**		**810E**		
	Method	Procedure	Method	Procedure	Method	Procedure
Low Pressure	500.1	I	500.2	I	500.3	II
High Temp.	501.1	I, II	501.2	I, II	501.3	I, II
Low Temp.	502.1	I	502.2	I	502.3	I
Temp. Shock	503.1	I	503.2	I	503.3	I
Solar Radiation	505.1	I	505.2	I	505.3	I
Humidity	507.1	II	507.2	II (5)	507.3	II (5)
Salt Fog	509.1	I	509.2	I	509.3	I
Dust and Sand	510.1	I	510.2	I	510.3	I, II
Vibration	514.2	VII(W)	514.3	I (1)	514.4	I (1)
Shock	516.2	I, II, V	516.3	I	516.4	I

CHAPTER 2: HARDWARE THEORY OF OPERATION

2.1 Introduction

The Control Module contains the Receiver Exciter Control Module (RECM), Audio amplifier board, Interface board, and display and keypad assemblies. The RECM is a shielded assembly containing the transceiver and all control and signal processing hardware and firmware, except the RF and audio power amplifiers. The trunk-mounted RF power amplifier contains a single PC assembly.

Schematics for all the boards are located in the back of the manual.

2.2 System Specifications

Table 2-1: Guardian G25RMV110 Technical Specifications

Specification	Description
General	
Frequency Range	136.000 to 174.0000 MHz
Banks, Zones, Channels, Shadow	4 banks, 16 zones, 256 channels, 7 shadow
Voice Digital	
Mode Voice Coding	IMBE™ 4.4 kb
Frame Re-sync Interval	180 msec
Error Correction Method	RS, golay, hamming
Mounting	Under dashboard using bracket
Dimensions	2.94”x7.13”x7.06” (H x W x D)
Weight	5 lbs. Approximately
Case	Metal and plastic
Temperature Range	-30° to +60°C
Channel Spacing	12.5 and 25 kHz, selectable in 2.5 or 3.125 kHz steps
FCC Type Acceptance Number	Pending
Industry Canada	Pending
Receiver (Measurements per TIA/EIA 603 Standards)	
Sensitivity	
Digital Mode: 5% BER Analog Mode: 12 dB SINAD	-116 dBm maximum
Spurious	-70 dB
Intermodulation	-70 dB
Audio Output Power	5W internal, 10W external speaker
Audio Distortion (at 1000 Hz)	5%
Frequency Stability (-30° to +60°C)	±2.5 ppm
Maximum Frequency Separation	Full-band split
Transmitter (Measurements per TIA/EIA 603 Standards)	
Duty Cycle	3%, 3 min continuous
RF Power Output	25W, 50W, 110W; also bypass mode
Spurious and Harmonic Emissions	-70 dB
FM Hum and Noise (wide/narrowband)	-48/-47 dB typical
FCC Modulation Designators	11K0F3E, 16K0F3E, 22K0F3E, 14K6F1E
Audio Distortion (at 1000 Hz)	5%
Audio Response (1000 Hz Ref.)	±3 dB 300 to 3000 (EIA/TIA 603)
Frequency Stability (-30° to +60°C)	±2.5 ppm

Specification	Description
Maximum Frequency Separation	Full bandwidth
DES Encryption	
Encryption Keys	16
Code Key Generator	External
SBCF Analog DES Encryption	Standard feature
Environmental Specifications MIL-STD-810F	
Test	Method/Procedure
Low Pressure (Altitude)	500.4/II
High Temperature	501.4/I, II
Low Temperature	502.4/I
Temperature Shock	503.4/I
Solar Radiation (Sunshine)	505.4/I
Humidity	507.4/I
Salt Fog	509.4/I
Sand and Dust	510.4/I, II
Vibration	514.5/I
Shock	516.5/I
Standard Accessories	**Optional Accessories**
5W Internal Speaker	10W External Speaker
Palm Microphone	DTMF Microphone
Mounting Bracket	Key Variable Loader
14 ft Power Cable	25 ft Power Cable

2.3 System Block Diagram

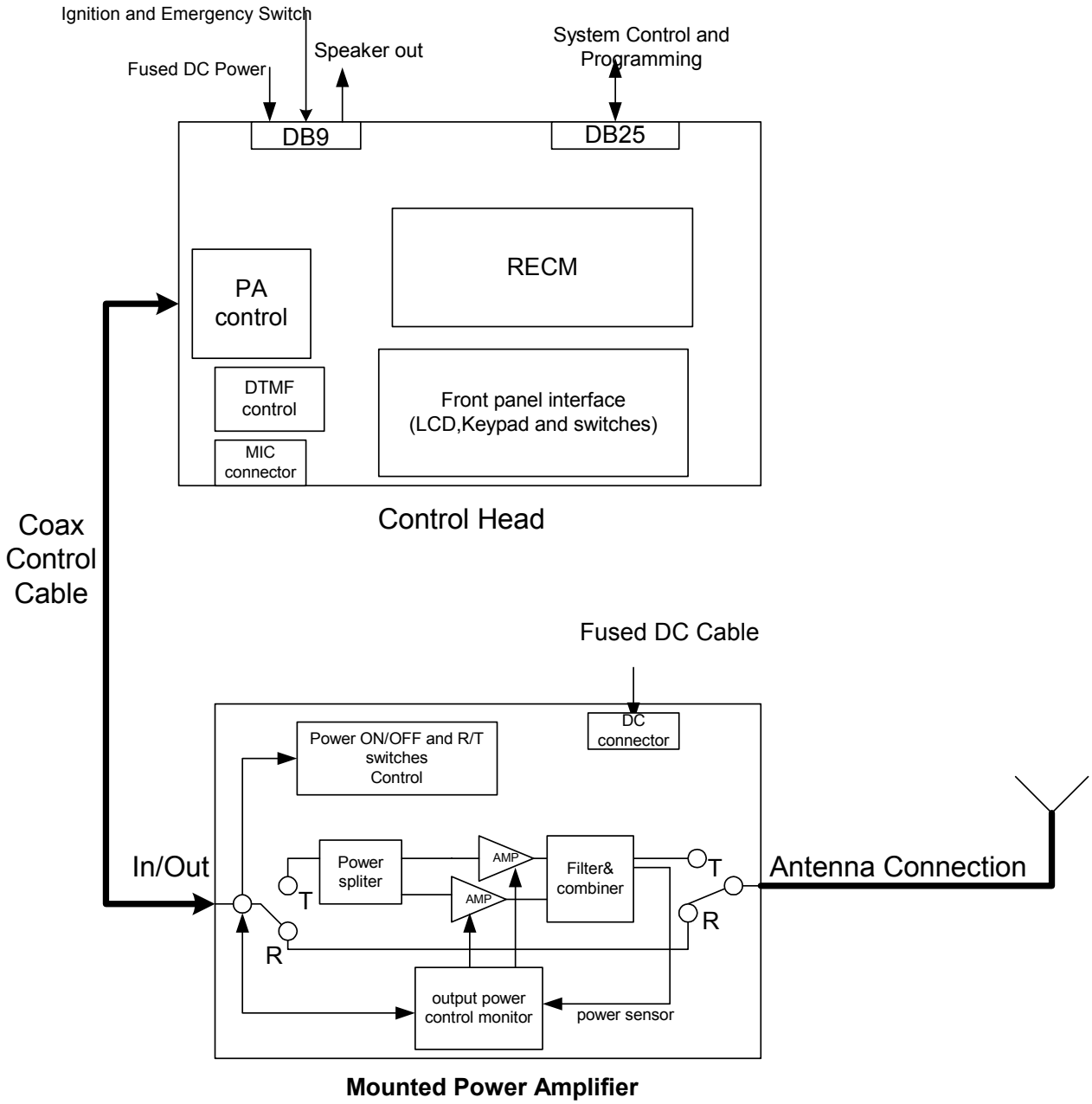

Figure 2-1: Interconnect Block Diagram

2.4 RECM Control Hardware Theory of Operation

2.4.1 Control Logic

The control logic interfaces to the keypad logic, transceiver, internal audio, and Motherboard. The control logic implements the main radio control function and all the baseband signal processing.

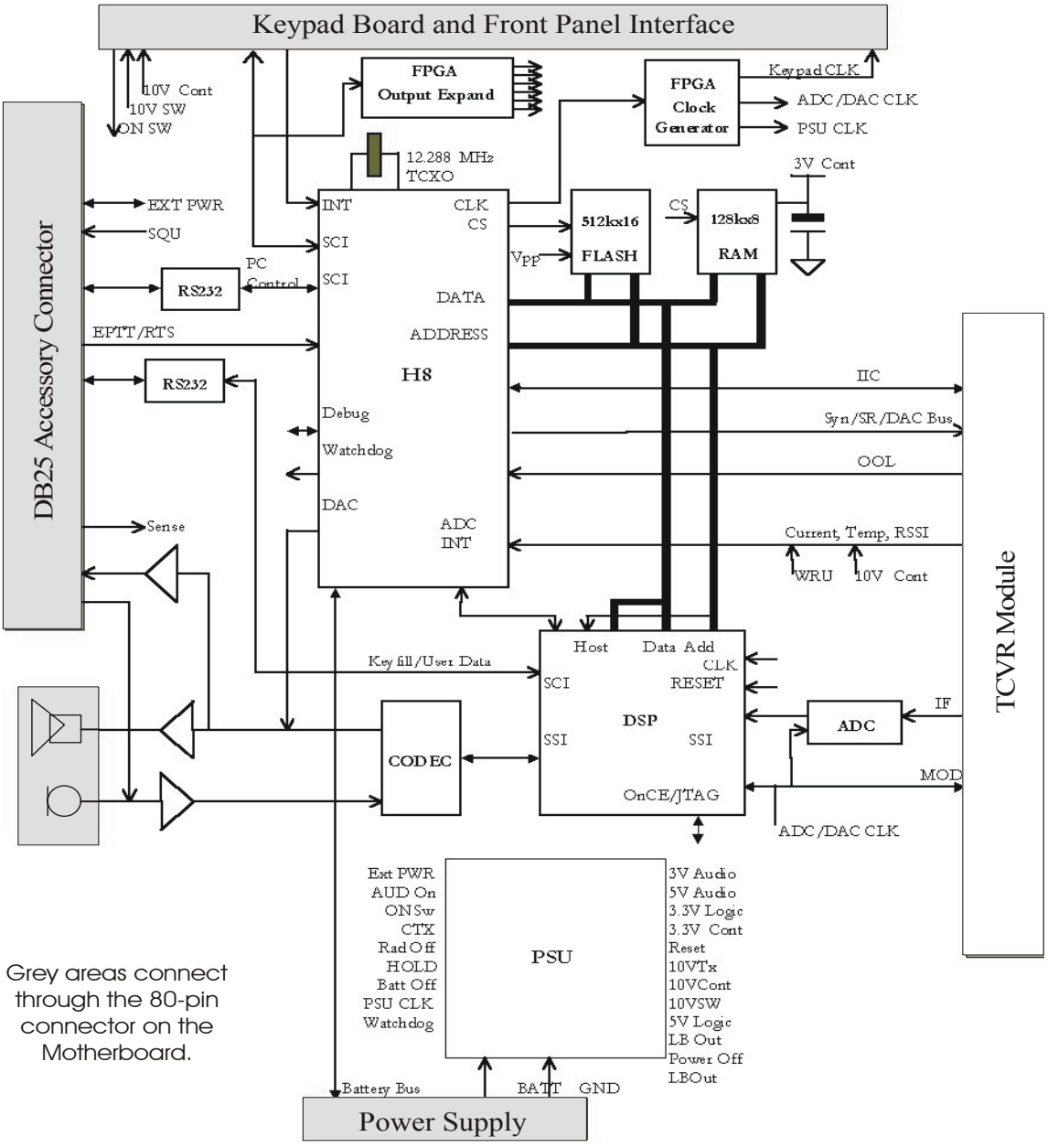

Figure 2-2: Guardian Control Logic

2.4.1.1 Power Supply Unit

This block of circuitry takes the 7.8V regulated voltage together with a number of control signals to generate a number of power supply outputs.

2.4.1.2 On/Off Switching

The main continuous supply 10V control is passed through a front panel on/off switch to generate 10V SW from the main radio supply. In normal operation the on/off switching is controlled by the radio on/off rotary switch by the control /RADON. Once switched on the main controller can hold the radio on by setting PWRHOLD. In addition to the radio rotary on/off switch, the on/off switching can be controlled by the external line /RADOFF via the accessory connector. This line overrides the /RADON line and can be used to force the radio off regardless of the rotary switch setting. However, the H8 controller uses the PWRHOLD and PWROFF lines to implement a clean controlled switch off.

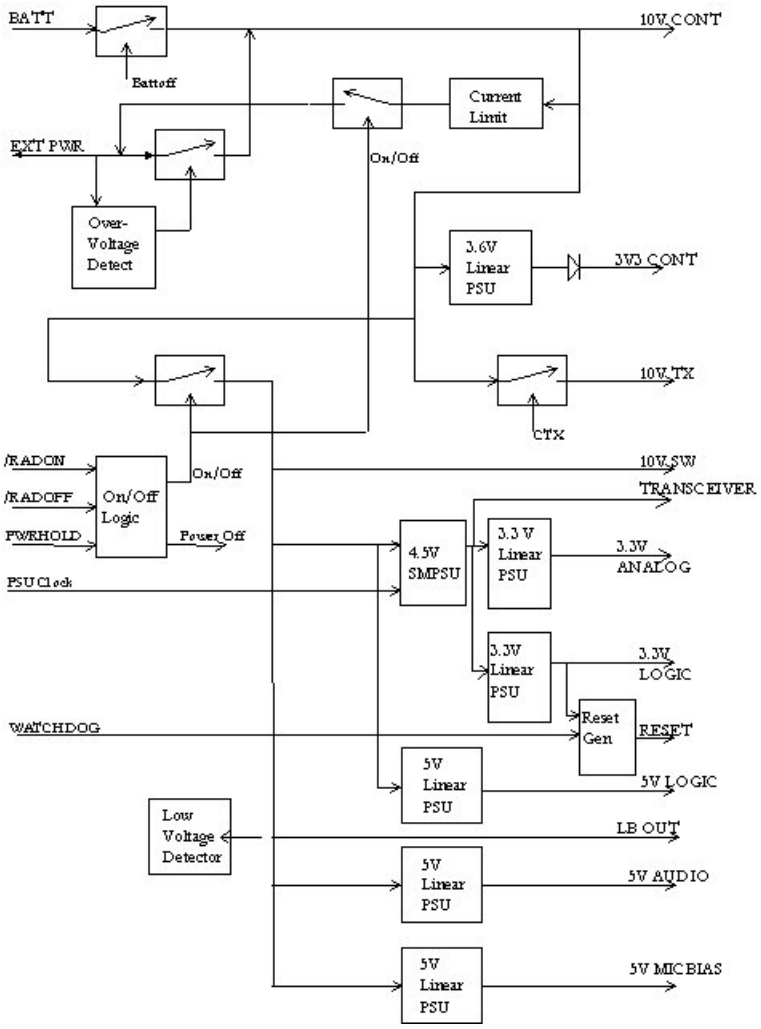

Figure 2-3: RECM Power Supply

2.4.1.3 Transmit Power Switching

A single FET switch controlled by CTX is used to provide a switched 10VTX high-current supply (1.5A) for the transmitter.

2.4.1.4 4.5V Switch Mode Power Supply

This circuit uses a switch mode power supply device to generate a 4.5V supply at 450 mA maximum for the radio logic. The switch mode device is synchronous and uses an externally provided power supply clock at 384 kHz. The power supply circuit includes input and output filters to limit the conduction of the fundamental switching components and their harmonics in the VHF band, both onwards into the logic and back into the power supply.

2.4.1.5 3.3V Linear Logic Supply

The output from the 4.5V switch mode power supply is passed through 3.3V linear power supplies to remove any remaining power supply switching noise on the main logic supply. One 3.3V supply is used for control logic, the other 3.3V, 50 mA supply is used for control logic analog circuitry.

2.4.1.6 Reset Generator

This circuit uses a MPU supervisory device (MAX825) to generate a reset pulse of at least 140 ms whenever the 3.3V logic supply drops below 3.08V. The circuit also generates a reset signal when the watchdog input is asserted by H8 or DSP.

2.4.1.7 5V Linear Logic Supply

This circuit generates a 5V logic supply at 50 mA maximum for use on the control logic.

2.4.1.8 Audio Supplies

Two linear regulators providing clean filtered supplies for the audio at 5V are provided. The audio power amplifiers use the 5V, 800 mA audio supply. The audio supply is used for the low-current microphone amplifier. A linear 5V bias supply to the internal microphone is also provided.

2.4.1.9 H8 Microcontroller

H8 is the main controller for the radio and is a HD6433044 ROM-less microcontroller. H8 is configured with an expanded bus connected to the Flash, RAM, and DSP. The H8 integral bus arbitration logic allows H8 and DSP to both have access to the Flash and RAM. H8 is clocked by the external TCXO.

H8 is powered from the 3.3V logic supply, and reset by the hardware /RES line. A watchdog output to the hardware-reset circuitry is provided. H8 generates chip select outputs to allow the Flash, RAM, FPGA, and DSP host port to be separately addressed.

One serial port of H8 is used to implement a bidirectional synchronous serial interface to the keypad board. This interface is used to communicate with the keypad MPU and directly load the LCD controller. The clock on this interface runs at 100 kHz. An associated interrupt input to H8 is used to initiate transfers from the keypad to H8. This serial interface is also used to load the output expander in the FPGA, and also to configure the FPGA.

One serial port of H8 is used to implement a bidirectional asynchronous serial interface to an external PC used for programming, filling, and controlling the radio. This interface uses programmable standard baud rates (default 9600 baud) and standard data formats. There are no handshaking parallel lines associated with this interface. Two parallel I/O lines on H8 are used to generate an I^2C interface to allow the EEPROM on the transceiver to be accessed. Four parallel output lines on H8 are used to generate a synchronous serial output bus with clock and data and separate strobe lines for the DAC, control shift register, and synthesizer on the transceiver.

One H8 DAC output is used to generate simple audio tones of varying volume for use as audio alerts. The second H8 DAC output is available for VCTCXOP control. The six-channel ADC is used to measure: the raw supply voltage, WRU radio input, reference crystal temperature, PA temperature, PA current, and RSSI. Two I/O lines are used to implement software UART, used for debug outputs in the development environment.

2.4.1.10 H8 Input Requirements

The total requirements for parallel input signals to H8, which need to be polled on a regular basis are:

- OOL: Out-of-lock (OOL) signal from the transceiver synthesizer
- EXT PTT: External PTT
- PWROFF: On/off switch position
- CONFDONE: Configuration status of FPGA

2.4.1.11 H8 Output Requirements

The total requirements for parallel output signals from H8, which need to be controlled are as below. A serial load output latch in the FPGA expands the output capabilities of H8.

- LCDA0: LCD controller A0 command/ data select
- LCDCS: LCD chip select
- SCL: I^2C and synthesizer clock
- DACSDA: Transceiver serial data, synthesizer, DAC, S-R
- SYNTHENA: Synthesizer framing pulse
- DACENA: DAC framing pulse
- SRENA: S-R framing pulse
- /DINT: Interrupt to DSP from H8
- /RESO: Watchdog output from H8

2.4.1.12 H8 Input/Output Requirements

The total requirements for parallel input/output signals on H8, which need to be read and controlled are:

- BATBUS: Not used in the mobile configurations
- SDA: I^2C data

2.4.1.13 H8 Input Interrupt Requirements

The total requirements for parallel input interrupt signals on H8 are:

- LBOUT: Not used in the mobile configuration
- DSPINTDSP: Interrupt

2.4.2 DSP

The DSP56309 (or DSP56302) processor implements all baseband signal-processing functions in the radio. It interfaces with the transceiver through one ESSI port, to the user for voice through the second ESSI port. The DSP function is controlled by H8 through the DSP host port. The DSP has direct access to the main Flash memory through the bus arbitration logic in H8, this allows it to download program images. The initial power-on code download is through the host port. The hardware-reset line resets the DSP. The TCXO clock output line clocks the DSP at 12.288 MHz. The DSP ESSI 1 port is used to provide a synchronous interface to the IF ADC and the transceiver 12-bit DAC. In receive modes that interface is capable of writing to the DAC at 48 ksps while still reading the ADC at 96 ksps. The DSP ESSI "0" port is used to provide a full-duplex synchronous interface to the audio CODEC using 8 kHz sampling rate and 13 bit samples. The data transfer is at 2.048 MHz using a DSP sourced clock and framing pulse.

2.4.3 Flash ROM

A 512k x16 Flash ROM is used as the main program store for the H8 controller and DSP. The Flash ROM uses a protected boot sector that is factory programmed via the DSP JTAG port. Normal reprogramming is implemented by running H8 from the boot sector and using 3V, programming the bulk of the device. The Flash is used to provide a parameter storage area for nonvolatile data storage of frequencies and keys, etc. This storage area is capable of in excess of 100k write cycles.

2.4.4 RAM

A 128k x 8 static RAM is used for temporary storage of data by the H8 controller. This RAM is powered by a continuous supply that maintains its contents as long as a power source is present. Additionally the RAM has a backup capacitor to retain its contents over power interruptions.

2.4.5 TCXO

This oscillator serves as the reference for all logic and power supply clocks within the control logic and keypad. It provides the data rate clocks for radio operation, and is the source of the ADC/DAC/CODEC conversion clocks. The TCXO is at 12.288 MHz, with a temperature tolerance of $\pm$2.5 ppm. Additional calibration is performed to provide a typical temperature tolerance of ± 1.0 ppm, a trimmer to set the initial frequency is provided. A Schmitt trigger buffer squares up the TCXO sine wave output before being output to H8 and DSP.

2.4.6 FPGA

The control logic uses an Altera 8282 FPGA device to provide a flexible serial data routing function, I/O expansion for H8 and DSP, clock generation, data multiplexing, and to absorb discrete logic functions.

The synchronous serial bus routing function involves routing the synchronous serial port of H8 either to the keypad and LCD, or to the I/O expansion in the FPGA. High-order address pins from H8 control this routing and a FPGA dummy write with dedicated FPGA chip select from H8. The FPGA includes a serial load parallel output shift register that is used for parallel output expansion for H8.

The discrete logic functions of the FPGA, includes logic to control an inverter for one of the LCD control outputs. The data multiplexing function involves rerouting serial pins between the accessory connector and the DSP SCI port to allow data transmission and keyfill operations.

2.4.6.1 FPGA Configuration

The FPGA is configured at start-up from the main Flash memory using a serial load from H8. During configuration outputs are tri-stated and pulled to a safe level by committing resistors to prevent audio and RF bursts at power up.

2.4.7 IF ADC

The IF sampling ADC is a 12-bit ADC capable of sub-sampling a 455 kHz, IF signal at 96 kHz sampling rate. It is connected by a serial interface to the DSP ESSI port 1. The serial data interface is clocked at 1536 kHz.

2.4.8 Clock Generation

The clock generation logic is used to generate clocks for the synchronous power supplies, the ADC serial interface, and the keypad microcontroller. The clock generator logic is implemented in the FPGA.

2.4.9 Logic Audio CODEC

The audio CODEC is an integrated ADC/DAC and audio filter device capable of full-duplex operation on voice bandwidth signals at 8 ksps. The samples have a resolution of 13-bits linear. The CODEC is connected to the DSP ESSI port “0” with serial data transfer rate of 2.048 MHz. The CODEC is continuously powered from the 3V logic and 3V audio supplies. DSP parallel control lines are used to mute the input and output sections as required.

2.4.10 Accessory Connector Interface and Filtering

All outputs are filtered to limit their bandwidth to the minimum and current limited to protect them from output short circuits to ground or up to 16V. All inputs are filtered and protected from continuous application of ground or +16V. There is no protection against negative applied voltages. Inputs and outputs are protected from static discharge of at least 10 kV air discharge. All inputs and outputs incorporate RF bypass filter capacitors adjacent to the connector, except for ground.

2.4.11 Transceiver Interface and Filtering

Most of the signals crossing the interface are filtered to limit their bandwidth to the minimum consistent with correct operation. Outputs from the control are filtered with series resistors on the RECM and grounded capacitors on the transceiver adjacent to the connector. Outputs from the transceiver to the control use the reverse configuration.

2.4.12 Keypad Interface

Some filtering is provided on this interface, but all outputs are protected from short circuits by series resistors. Where possible, inputs are also protected from damage by series resistors.

2.4.13 Audio Interface

The audio interface is implemented with four-way wire connectors directly via the 80-pin interface through the Motherboard to the integral speaker and microphone.

2.4.14 Test Interface

The test interface provides the following functions:

- Joint test action group (JTAG) connector access for board test and Flash boot sector programming
- Board reset and control access
- Board power supply and on-off switching access
- H8 serial debug port access

2.4.15 LED

The control logic incorporates a 3-color LED used for status information. It is controlled by the FPGA to show red, green, or off. It is optically coupled to the top face of the radio by a light pipe. The hardware is configured so during hardware reset, before the keypad MPU software is running, the LEDs are off.

2.4.16 RECM Power Consumption

The control logic operates at input voltage 7.7V. The average current consumption of the control logic is:

- Standby mode: 60 mA
- Receive mode @ 500 mW: 330 mA
- Transmit mode @ 2W: 1,000 mA
- Transmit mode @ 5W: 1,500 mA

2.5 RECM Transceiver

RF shields covers the board.

2.5.1 Interface

J2 is the transceiver antenna connector. RF signals are transmitted and received through this surface mount RF connector. Transmitted and received RF signals are routed from this connector through a short RF cable to the RX/TX relay on the Motherboard.

2.5.1.1 Transmit Chain

The pre-driver amplifier (Q7, etc.) amplifies the TXLO signal from the synthesizer section. The Q7 output power is typically 13 dBm measured at C77/R44/R49 node.

R44, R49, and R52 are part of a 3 dB pie attenuator network. The gain control is made up of CR5, CR6, and associated components. This circuit yields more than 50 dB of useful attenuation range. The circuit is part of a DAC controlled closed loop system, in conjunction with the detector/power control circuit (U12, U13, and associated components), which controls the transmitter output power level. The power amplifier (PA) is a Mitsubishi M68776, 7.2V, 6W gained controlled power amplifier**.**

The harmonic filter (C209, L30, C81, C82, L31, C83, and C84) attenuates harmonics created by the power amplifier. The harmonic filter insertion loss is 0.4 dB typically at 174 MHz. The output of the harmonic filter connects to the 20 dB coupler (U12). This coupler is part of a DAC-controlled closed loop system designed to set the transmitter output power level. The insertion loss through the coupler (U12-1 to U12-3) is 0.2 dB typically.

2.5.1.2 Power Amplifier Control

Transmit output power level is controlled by the detector/power control circuit and the gain control amplifier input via VCONTROL. This closed loop system is designed to keep the transmitter output power constant over variations in temperature, transmitter supply voltage (7.5VT), and RF power levels into the transmit chain. The detector/power control circuit is made up of the 20 dB coupler (U12), an RF rectifier circuit (CR11, CR12, etc.), and an integrator (U13). The DAC line labeled PWRSET at the non-inverting input of U13 sets the transmitter to the desired power level. U12-2 samples the transmit signal. The sampled RF signal is rectified by the temperature stable circuitry of CR11, CR12, etc, and is routed to the inverting input of the integrator at U13-4. The output of the integrator at U13-1, labeled VCONTROL, controls the gain of the power amplifier. Any change in transmitter output power level is automatically corrected by the loop.

2.5.1.3 PIN Diode Switch

The antenna PIN diode switch is made up of CR7, CR8, CR9, CR10, and other associated components. This switch is a four-port design. The four ports are antenna 1 (TOP RF), antenna 2 (SIDE RF), receive, and transmit. Receive and transmit ports can be switched to only one of the two antenna ports. Transmit signals are routed from the transmit/receive PIN diode switch (to be discussed in the following paragraph) to the antenna port. The receive signal is routed from the selected antenna port to the transmit/receive PIN diode switch. The antenna PIN diode switch and receiver circuits share current in the receive mode of operation via the signal labeled RXSINK at Q11, pin 3. The insertion loss through the antenna pin switch is 0.2 dB typically.

The transmit/receive PIN diode switch is made up of C6, L60, L38, L40, L39, D9, D7, D10, C97, C98, C104, C105, C106, C107, and other associated components. C127, C114, L42, and C115 are the 1/4 wave simulator circuit. The 1/4 wave simulator is critical to the design of the switch. In the transmit mode of operation CR13 and CR14 are forward biased. C116 resonates with the internal series inductance of CR14 at 155 MHz and the receive port (RX INPUT) is RF shorted to ground. With the receive port RF shorted to ground; the parallel combination of C127, C114, and L42 forms a tank circuit resonating at 155 MHz. Consequently, the receive port appears as an open circuit to the transmit signal and is routed to the antenna PIN diode switch. In the receive mode of operation, CR13 and CR14 are biased off so C114/L42/C115 appears as a low-pass filter (LPF) to signals at the antenna port of the switch. The insertion loss through the transmit/receive PIN diode switch is 0.4 dB in the transmit mode and 0.2 dB in the receive mode typically.

Q10 to Q19 and associated components are switching transistors used to control the antenna and transmit/ receive PIN diode switches. The current flowing through the entire PIN diode circuit is approximately 45 mA in the transmit mode of operation. In the receive mode of operation the transmit/receive PIN diode switch is disabled, and nominal 85 mA flows through the antenna PIN diode switch.

2.5.2 Receiver

The VHF signal enters into the RX INPUT via the PIN diode switch (discussed previously). D1 and D2 are Schottky protection diodes to protect the front-end circuitry from RF overloads that could occur if the PIN diode switch failed to work properly or if a transmitter is very close to a receiver. Typical insertion loss is 0.1 dB for the protection diodes. L25/C61 form a band-stop filter (BSF) at the first IF frequency of 45 MHz. Typical insertion loss for the BSF is 15 dB at 45 MHz but less than 0.1 dB in the VHF band.

L14, L6, CR3, CR4, L7, CR27, CR28, L8, and L15 make up the very high frequency (VHF) preselector band-pass filter (BPF). The BPF is inductively coupled for improved high-side attenuation. This filter provides attenuation to spurious signals such as the first image and the half-IF. The BPF is varactor diode tuned by DAC line RXVTF. Typical insertion loss (138 to 174 MHz) is 1 dB for the VHF BPF.

The RF amplifier (Q1, T1, etc.) utilizes loss-less feedback to deliver reasonable gain, low-noise figure, and a high third order intercept point simultaneously. Typical gain (136 to 174 MHz) is 11.5 dB for the RF amplifier.

C14, L1, C9, C15, L2, C10, C16, L3, C11, C17, and L9 form a VHF LPF. This filter provides additional RX spurious attenuation as well as image noise attenuation. L4, C12, L16, C25, L5, and C13 form a BSF at the first IF frequency of 45 MHz. The insertion loss is 1.0 to 2.0 dB (136 to 174 MHz) typically for the cascade. The IF BSF insertion loss is typically 40 dB at 45 MHz, but less than 0.3 dB in the VHF band.

U1 is a double-balanced mixer (DBM). U1 converts the desired RF signal down to the first IF of 45 MHz. High-side local oscillator (LO) injection is used. Therefore, the LO is 45 MHz higher than the receiver tuned frequency. The LO drive level is +10 dBm nominal at U1, pin 1. The conversion loss of the mixer (RF to IF) is 5.5 dB typically.

The LO signal is generated in the synthesizer section (to be discussed later). The LO signal is designated RXLO on the schematic diagram. The LO signal is routed to a LPF consisting of C31, L21, C87, C30, L20, C75, and C28. L19 and C28 are also used to impedance match the LO port of the mixer. The insertion loss of the VHF LO LPF is 0.3 dB typically at 174 MHz.

R4, L17, C6, L10, R5, and C23 make up the diplexer network. This network properly terminates the DBM both in and out of band. The diplexer also provides some additional half-IF spurious rejection. The diplexer insertion loss is 0.8 dB typically at 45 MHz.

There are two 45 MHz IF amplifier circuits. The first (Q2, T2, etc.) utilizes loss-less feedback to deliver reasonable gain, low-noise figure, and a high third order intercept point simultaneously. Typical gain is 10.5 dB for the first IF amplifier.

There are two crystal BPFs and a second 45 MHz IF amplifier. The BPFs provide attenuation for the adjacent and alternate channels, and also for the second image response. FL1 is a four-pole crystal filter with a 20 kHz bandwidth centered at 45 MHz. FL4 is a two-pole crystal filter with a 30 kHz bandwidth centered at 45 MHz. The second 45 MHz IF amplifier provides high gain to prevent further degradation of receive sensitivity. C57, L12, C18, C19, and L13 are impedance matching elements for the input of FL1. The output of FL1 is impedance matched to the second 45-MHz IF amplifier (Q36, etc.) by C285, L64, and C242.

The output of the second 45-MHz IF amplifier is impedance matched to FL4 by C287, L61, C286, C237, L60, and C235. The entire cascade provides 21 dB of gain and has a 3 dB bandwidth of 20 kHz typically. Typical insertion loss is 1.5 dB for each crystal BPF.

The IF IC (U28) contains the second mixer and an IF amplifier chain. The 45 MHz IF signal enters U28 at pin 6 from the crystal BPF (FL4). FL4 is impedance matched to the IF IC input by C294, L62, and C288. The incoming 45 MHz IF signal is mixed with the second LO (to be discussed later). The second mixer IF output is at U28, pin 8 and the second IF frequency is 455 kHz.

The signal from U28-8 is routed to FL3. FL3 is a ceramic BPF operating at 455 kHz. The insertion loss of the ceramic BPF is 6 dB typically in a 1500-ohm system.

The 455 kHz IF signal enters U28-10, is amplified by a cascade of IF amplifiers, and exits at U28-14. The signal from U28-14 then enters a second ceramic BPF, FL2. FL2 is the final ceramic BPF with a typical insertion loss of 8 dB in a 1000-ohm system. The 455 kHz IF signal enters its final stage of amplification at U29-3. U29 is configured as a non-inverting operational amplifier and is capable of driving a 50-ohm load. The amplifier is set for a voltage gain of 2.5. With the receiver set to full gain the signal level at J4 (455 kHz IF OUT MONITOR) is -20 dBm ±3 dB into 50 ohm with a -119 dBm unmodulated 136 MHz signal injected at J2 (TOP RF) or J3 (SIDE RF). The second LO consists of CR26, R33, Y1, L24, C59, C226, C227, and Q35. The oscillator is a Colpitts type with the crystal operating in the series mode. CR24 is a varactor diode used to set the oscillator on frequency using the DAC output labeled 2nd LO. The second LO operating frequency is 44.545 MHz (low-side injection). L65 and C223 impedance match the output of Q35 to the LPF (C289, C293, L63, and C284). The signal is attenuated by R282, R283, and R284 and sent on to the second mixer. The signal level at U28-4 is -16 dBm nominal.

U4 is a voltage regulator used to power the receiver circuits. The dc voltage appearing at U4, pin 1, labeled RXSINK on the schematic diagram, is routed from the antenna PIN diode switch. As previously discussed, the PIN diode switch and the receiver circuits share current to reduce receive power consumption. The control line +3.3V RXEN is used to enable the regulator while the transceiver is in the receive mode of operation. The regulator is disabled during the transmit mode of operation.

2.5.2.1 Synthesizer and Reference Oscillator

U19 is a fractional-N synthesizer IC programmed for a specific frequency by loading appropriate serial data into the IC. It controls the receive VCO when the transceiver is in the receive mode of operation, and the transmit VCO when in the transmit mode. The programming lines are labeled 3VSCL, 3VSDA and 3VSYNTHENA on the schematic diagram. These are all CMOS logic level inputs. R118 (RF) and R123 (RN) are the fractional compensation and phase detector current setting resistors, respectively. These resistors are critical to the operation of the synthesizer system and must be checked when troubleshooting around U19. The phase detector output pins (U19-13 and U19-14) are fed to the passive loop filter (R140, C177, C172, R134, and C173) and on to the VCO control varactor diodes (CR17/CR19) for frequency control. The buffered, filtered output from the VCO is fed into U19-5 (RF IN) to close the phase-locked-loop. The level is typically -10 dBm into U19-5. The reference oscillator is made up of CR22, Y2, Q28, C197, and C198 and associated components. The reference oscillator operates at 12.8 MHz. The reference oscillator operating frequency is adjusted by varying the dc voltage at the DAC controlled line that is labeled REFOSCMOD. This line is also used to modulate the reference oscillator during the transceiver's transmit mode of operation. The 12.8 MHz signal is fed into the synthesizer chip at U19-8 (REF IN) using a coupling capacitor, C194. The AC signal level at U19-8 is 1V p-p typically.

U22 is the reference oscillator temperature sensor used to monitor the temperature near Y2. Its output is labeled XTALTEMP on the schematic diagram. This line is normally monitored by the microprocessor so the reference oscillator can be adjusted for drift due to changes in temperature.

2.5.2.2 Receive/Transmit VCOs and Buffer Amplifiers

The receive VCO operates from 181 to 219 MHz since high side LO injection is used and the first IF is 45 MHz. The transmit VCO operates from 136 to 174 MHz. Each VCO is a Colpitts type design utilizing a low noise, bipolar transistor as the active device. The receive VCO uses Q24 and the transmit VCO uses Q21, each in the common collector configuration. The Colpitts capacitors are C169/C180 (receive VCO), and C137/C142 (transmit VCO). These capacitors enable Q24 to oscillate in the 181 to 219 MHz frequency range and Q21 to oscillate in the 136 to 174 MHz frequency range. L53 is the resonating inductor for the receive VCO and L45/L46 are the resonating inductors for the transmit VCO. CR20/CR21, and CR16/CR18 are the coarse tuning varactor diodes for the receive and transmit VCO respectively. These diodes are used to coarse tune the VCO such that the LPF, phase detector output voltage (from U19) at TP10 equals 1.65 Vdc. The receive and transmit VCOs share the coarse tuning DAC controlled line labeled CTUNE. Coarse tune dc voltage swings from nominal 1.8 to 22 Vdc. CR19 (receive VCO) and CR17 (transmit VCO) are the fine-tuning varactor diodes controlled by U19 as was explained previously. CR15 is the modulation varactor diode for the transmit VCO. The output from the receive VCO is coupled off Q24-E using C174. The output from the transmit VCO is coupled off Q21-E using C139. The signal is measured at the C174/R146 node (receive) and the C139/R107 node (transmit), and measures -15 dBm typically.

Q26 and Q22, and associated components, form the first VCO receive and transmit buffer amplifiers respectively. These amplifiers buffer the VCO output from changing-output voltage standing wave ratios (VSWR) that could pull the VCO off frequency. The output from each measures -5 dBm typically. The buffer is measured at the C170/R141 node (receive) and the C138/R131 node (transmit). Q25 is the second buffer amplifier. This amplifier is common to both the receive and the transmit VCOs. R131, R141, and R142 are the combining elements used to make this possible. This buffer outputs a signal large enough, after subsequent attenuation and filtering, to properly drive the RF IN pin of the synthesizer (U19-5). The output from this buffer is measured at the C167/C53/L52/C175 node and measures 0 dBm typically.

The output from the Q25 buffer is filtered by C175, C53, L52, and C176. This LPF prevents the synthesizer IC (U19) from locking on to harmonics of the desired frequency. The insertion loss of the LPF is 0.4 dB typically.

The signal is then split by R138, R139, and R144, and sent on to the appropriate receive or transmit final buffer amplifier. The signal measured at R139/C150/ C186 node is -6 dBm, and the signal measured at R144/R143/C168 node is -6 dBm.

Q23 (receive) and Q27 (transmit) is the final buffer amplifier. Q23 amplifies the signal up to the level needed to properly drive the LO port of the DBM (discussed previously). Q27 amplifies the signal up to the level needed to properly drive the PA pre-driver (previously discussed). The signal measured at RXLO is +7 dBm typically. The signal measured at TXLO is +7 dBm typically.

U17, Q20, etc. form the voltage regulator for the receive and transmit VCO/buffer amplifiers. R67, C124, and Q20 form a super filter, which attenuates voltage regulator noise that may otherwise degrade the synthesizer phase noise performance.

U20, U21, Q29, Q30, CR23, CR24, CR35, C199, C202, C203, etc. create a voltage multiplier. The circuit is configured as a voltage quadrupler. Circuit losses and output loading lowers the voltage down from 24 Vdc to about 22 Vdc. The driver circuit (U21) switches at about 192 kHz. This frequency was selected so harmonics would not land at or near the second IF frequency of 455 kHz. The 22 Vdc supply is used to power the DAC supporting quad op-amp U18.

The shift register (U24) is used to control transceiver modes of operation and functions. The line labeled STD/SIDE selects the desired antenna port of the transceiver. The line labeled TX/RX selects either the transmit or receive mode of operation. +3.3V RXEN turns the receiver on and off (previously discussed). Q34/Q32 and Q33/Q31 enable and disable the receive and transmit VCOs and buffers respectively (discussed previously). U16 is the voltage regulator that supplies all 5V digital circuitry on the transceiver.

2.5.3 Digital/Analog Control

Digital/analog control is shown on page 1 of the RECM schematic. The transceiver is fitted with an EEPROM (U15). The IC is used to store calibration and curve fit data, which is needed when the transceiver is configured with the Guardian radio. Each transceiver has its calibration and curve fit data stored within the EEPROM. The calibration and curve fit data is written to the EEPROM at the successful conclusion of level 2 testing. Two quad 8-bit serial DACs, a quad 12-bit serial DAC, and supporting operational-amplifiers (U2, U6, U13, U18, and U30) control much of the transceiver, as has been discussed previously. U32 is a 2.5 Vdc reference used by the Quad 12-bit DAC and the variable IF attenuator (discussed previously).

U18D and associated components amplifies the dc signal supplied by U31-3.

As was discussed previously, REFOSCMOD is the dc signal, which varies the operating frequency of the reference oscillator. Normally under DSP and microprocessor control, this line is used to FM modulate the reference oscillator, which in turn FM modulates the RF carrier in transmit mode. This line is used to temperature compensate the reference oscillator as well.

The DAC controlled line TXVCOMOD at U31-4 is transmit data normally controlled by DSP and a microprocessor. This signal is routed to U18C and associated components. U18C and associated components form an active LPF/attenuator to shape the transmit data before modulating the RF carrier in the transmit mode. The cutoff frequency of the LPF occurs at 20 kHz. The 1 kHz peak-to-peak signal level at the active LPF output (U18-8) is one-fourth TXVCOMOD at 2.5 Vdc.

The synthesizer reference oscillator and the transmit VCO are simultaneously modulated to balance the FM modulation. We refer to this technique as two-point modulation. The DAC values required to balance the modulation are dependent on RF frequency.

The dc signal at U31-17 is routed to U30 and associated components. This op-amp is configured for a voltage gain of 2. The dc signal VATT controls the variable IF attenuator (discussed previously) in the receiver chain. Under DSP and microprocessor control, the attenuator is normally set for a desired amount of attenuation by this DAC controlled signal.

Q37, Q38, Q39, Q40, Q41, and associated components are used to enable and disable the 14 dB step attenuator in the receiver chain (discussed previously). Normally under DSP and microprocessor control, the attenuator is set to the desired state of operation via U31-13. A logic level “1” at this pin enables the attenuator. Conversely, a logic level “0” at this pin disables the attenuator (bypass mode).

U18B and associated components amplifies the dc signal supplied by U33-2. As discussed previously, CTUNE is the dc signal which coarse tunes the receive and transmit VCOs. Under microprocessor control, the appropriate VCO is normally coarse tuned to a desired frequency based on curve fit data stored in the EEPROM (U15). Curve fit data is obtained and stored in the EEPROM during coarse tune calibration procedures performed at level 2 testing.

The DAC controlled DC signal 2nd LO sets the 2nd LO (discussed previously) on frequency at 44.545 MHz. Normally under microprocessor control, the 2nd LO is set on frequency based on a DAC value stored in the EEPROM (U15). The correct DAC value is obtained and stored in the EEPROM during the 2nd LO calibration procedure at level “2” testing.

The DAC controlled dc signal RXVTF appropriately sets the varactor tuned BPF (discussed previously) based on the receiver tuned frequency. Normally under microprocessor control, the varactor tuned BPF is set based on curve fit data stored in the EEPROM (U15). The curve fit is based on statistical data obtained during the testing of hundreds of units.

The DAC controlled dc signal PWRSET sets the power amplifier (discussed previously) to a desired power level. Normally under microprocessor control, the power amplifier is set to the desired level based on curve fit data stored in the EEPROM (U15). The curve fit data is obtained and stored in the EEPROM during transmit power calibration procedures at level 2 testing. The power calibration procedure obtains curve fit data for five power level settings (0.1W, 0.5W, 1.0W, 2.0W, and 5.W) over the entire transmitter operating frequency range (136 to 174 MHz).

The DAC controlled dc signals PA1 and PA2 set the gate bias for each power transistor (Q6 and Q9 respectively) in the power amplifier circuit (discussed previously). These two signals are routed to op-amps U2 and U6, which are

configured for a voltage gain of 2. The outputs at U2-1 and U6-1, labeled PABIAS1 and PABIAS2 respectively, are then routed to the gates of the power transistors. The correct DAC values for the bias current are stored in the EEPROM (U15). The correct DAC value is obtained and stored in the EEPROM during the power amplifier bias calibration procedure at level 2 testing. Each gate is biased such that 100 mA of current flows through each power transistor with PWRSET set to a DAC value of zero in the transmit mode. Level 2 software monitors the U10 output line labeled IMONITOR when calibrating PA bias.

2.5.4 Keypad Microcontroller

The keypad board is controlled by an Atmel AVR4414 microcontroller. This is a Flash programmable device. The microcontroller implements these functions:

- Keypad scanning
- PTT switch input
- Auxiliary keys input
- Volume switch input
- Channel switch input
- Emergency switch input
- Synchronous bidirectional serial interface to main controller at 100 kHz
- Keypad and LCD backlight control

A clock derived from the main reference clock, clocks the keypad microcontroller at 1.5 MHz. The keypad microcontroller is powered by the 3.3V supply as the LCD driver device.

2.6 Audio Amplifier Board

2.6.1 Description

The Audio amplifier board contains the internal and external audio and control circuitry. It also houses the DB25 accessory connector, the DB9 power connector, and the RF control connector that protrudes through the rear panel. The board is located in the Control Module. The board contains the following functions:

- RFI and transient protection and system on/off switch
- Voltage regulator and 7.8V on/off switch
- Communication with transceiver
- Audio power amplifiers
- Power levels detector and converter and the RF and DC combiner
- PA on off control
- RFI and transient protection

2.6.2 Power Conditioning

Power for the Guardian 110W control head enters this board on J5 the DB9 connector. Dual low $R_{DS(on)}$ P-channel FET Q10 serves as reverse polarity protection and on-off switching. Transistor Q7 pulls down the gates of Q10 when the ON/OFF signal is high, allowing Q10 to conduct. With ON/OFF control low, Q10 is cut off, and will not pass forward or reverse polarity. An over-voltage condition is detected by D2 and Q6, which cause Q7 to cut off and turn off power.

Back-to-back transorbers D1 and D4 are used to eliminate voltage spikes before the on/off switch. The input power is routed to the clamp circuit via an LC filter. The filter eliminates unwanted signals from being conducted to the vehicle power line.

2.6.2.1 Voltage Regulator and 7.8V On/Off Switch

Linear regulator U5 provides +7.8V to the RF power control circuitry and to the other two PC assemblies in the control head. The regulator is powered via Q10 body diode at all time. When the unit is turned off all the circuits are disconnected from power except the transceiver in the control head. The transceiver in this case is in the off state. The power consumption in this case is less than 2 mA powering the boat backup memory circuits.

2.6.3 Communication with Transceiver

Twenty pin IDC headers J2 and J3 carry control and status signals from the transceiver and front panel via the Control PCA.

2.6.4 Audio Amplifiers

The board contains two identical audio amplifiers. Each audio amplifier has 20 dB gain and is capable of delivering more than 10W to a 4-ohm load in a bridge-tied-load configuration. They are fed from the transceiver audio output. A front panel switch selects either or both amplifiers; an unselected amplifier is placed in a mute condition by the appropriate disable signal. When there is no received signal, both amplifiers are placed in a low-current standby mode by squelch comparator.

2.6.5 Power Levels Detector, Converter, and RF/DC Combiner

ON /OFF, PTT and RF output power control signals to the 110W power amplifier are generated on this board. These are present as DC signals on the center conductor of the coaxial cable connecting the control head to the remote RF PA. A low-pass filter prevents RF from reaching the control circuitry. The voltage levels are as follows:

DC Control Voltage Range	PA State
0 to 0.4V	DC on/off switch – OFF
>0.7V	DC on/off switch – ON
0.7 to 1.2V	PA is in bypass – RECEIVE mode
2.1V	Power output set 25W
3.6V	Power output set 50W
6.5V	Power output set to 110W

The transceiver power levels are detected via the connection to TP21. The voltages are as follows:

TP 21 Control Voltage	Boat Power Output
2.85	5W
1.87	2W
1.28	1W

The control circuits converts an input above 2.2V (5W setting) to a control signal to 6.5V, which results in 110W generated in the remote RF power module. Accordingly it converts the 2W and 1W control levels to the indicated PA control. Input control of less than 1V is converted to 2.6V. The PA puts out 25W also for the 0.5W input power setting but will fail to do so at the 0.1W setting. In this case power output is not specified, and the red LED will not light.

2.6.6 PA ON/OFF Control (Bypass Mode)

It is possible to operate the system not utilizing the PA (PA in by pass mode.) This is done by turning on control head on with the PTT depressed. An orange TX light indicates to the user that he is operating in by pass mode. In this mode, output power is about 1dB lower that the nominal levels delivered from the transceiver, as indicated in the table above. In normal mode, Q16 conducts at start-up, causing Q14 to conduct, which keeps Q15 off. When using this mode, Q16 conducts in the reverse direction, Q14 remains off and Q15 conducts, which prevents bias voltage from being sent to the RF power amplifier.

2.6.7 RF Power Indication

Operational amplifier U3A forces the output control voltage at Q8-E to be equal to that at U3-3. After high power transmit is detected at the PA output. The RF PA test circuit forces additional current back into this line. The op-amp loop holds the voltage at the input level, so the additional current is forced out Q8-C and through R44. This forces Q9 to conduct and sink additional current from the LED_TX. The LED_TX turns off the green light. When the unit is in bypass (low power) mode the Tx lamplights orange because the red and the green LED's are on.

2.6.8 Audio Board Block Diagram

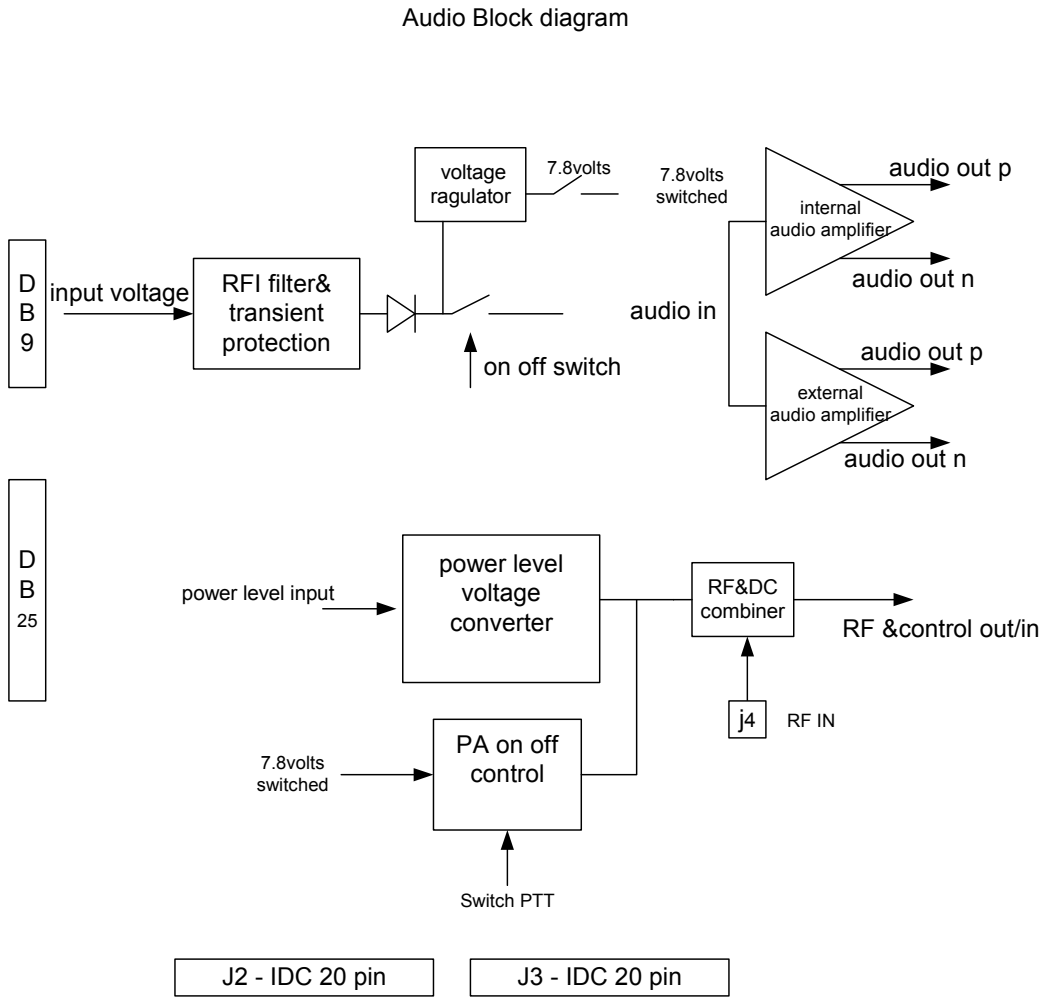

Figure 2-4: Audio Board Block Diagram

2.7 Display Board

The Display board consists of a seven-switch keypad and an LCD module with integrated LED blue backlight. The board is heatstaked onto the plastic front panel, forming a permanent assembly. Electrical connections are made to the Interface board via a 20-pin connector (J13).

The radio display module is a full graphics 80x32 pixels LCD, requiring a temperature compensated differential driving voltage of about 12V and a 1/6 bias, 1/32 duty cycle driving scheme. The LCD driver device (Seiko Epson SED 1530) drives the display. This LCD driver has an internal display RAM that copes with all the display refreshing autonomously. Display data transfers from the main controller are only required when the display is changed, selective display RAM updates are also available to minimize serial traffic. The LCD driver display RAM is accessed through a one way synchronous serial interface and connected in parallel with the AVR serial port. The LCD CS input is used to differentiate between serial data for the LCD driver and the keypad board hardware reset line resets the display drive. The hardware is configured such that during hardware reset, before serial LCD data is presented, the LCD is blank. The radio keypad consists of 16 keys, which contact onto switch contacts on the rear of the keypad board.

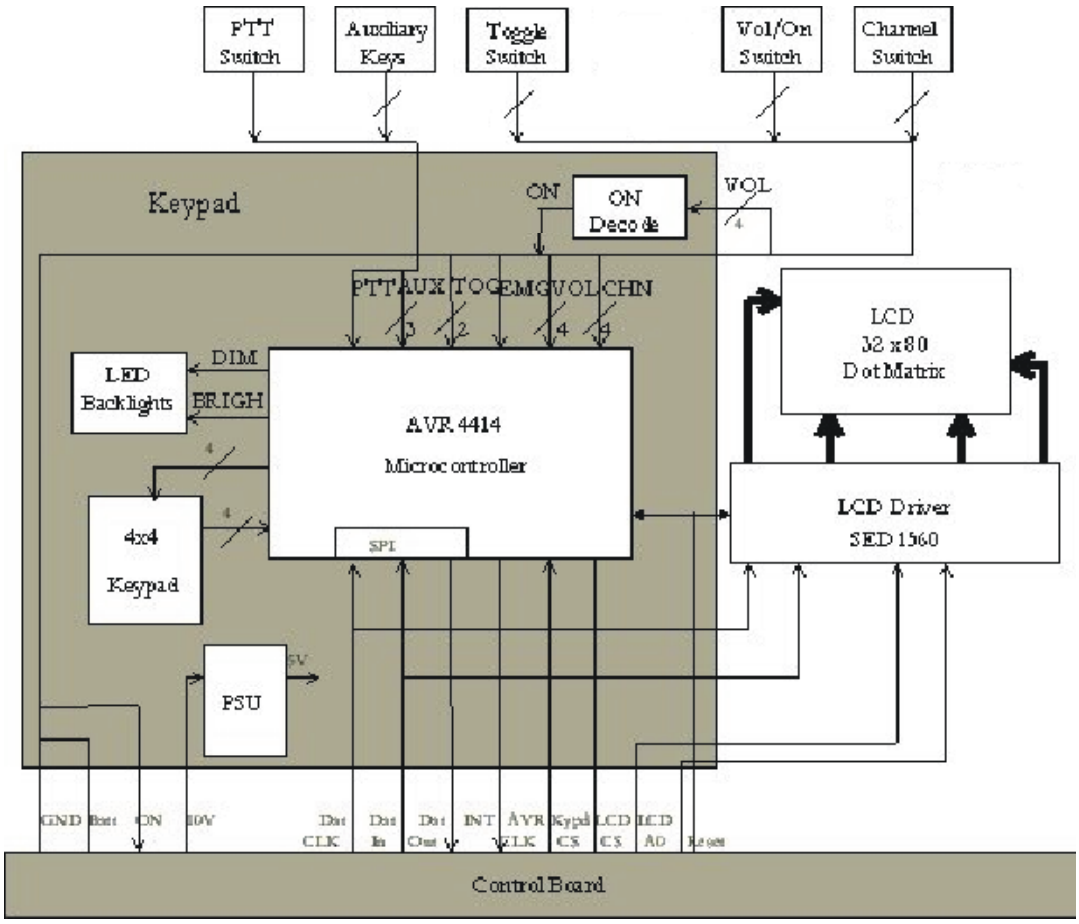

Figure 2-5: Keypad Board

2.7.1 Control Logic Interface

The signals on this interface need not be filtered, but are protected from short circuits to ground. All logic signals are at 0 to 3V Complimentary Metal-Oxide Semiconductor (CMOS) levels at the interface. The interface carries the following functions:

- 10V Control
- Ground
- /RADON
- Switched 10V Supply
- Reset
- AVR Clock
- Serial Data Clock
- Serial Data Input
- Serial Data Output
- Key Interrupt
- LCD Chip Select
- LCD A0 (data\command select)
- Keypad Chip Select

2.7.2 Keypad

2.7.3 Switch Interface

Interface to switches is provided to the RECM via 80-pin connector to the Interface board.

2.8 Interface Board

This board is located in the Control Head Assembly in the vehicle cab. The transceiver (RECM) is mounted to this board and interfaces through 80-pin connector J1. The front panel display PCA mounts to this assembly and interfaces through 20-pin connector J4. The microphone interface is J5, an 8-pin modular connector. Communication with the audio amplifier board and the remote RF Power Amplifier is through two 20-pin connectors J2 and J3. The DC power for this board, the transceiver and front panel functions enters via J3. The 3.3V powering the display and logic is generated by a linear regulator U1 powered from the 7.8V via an on/off switch q12. All front panel switches and LED lamps are mounted to this board. Connection to the internal 5W speaker is via J6.

ON/OFF control: Transistors Q11-14 are connected to the outputs of the binary volume switch SW3. The transceiver uses these signals to detect the off position of the volume switch. At the off position all lines are open. If any of the lines is switched and ignition power is high Q17 is on providing low (0V) to one of the transistor witch will result in a positive ON/OFF voltage. This signal witch is routed also to the audio board to control power function there and in the remote RF Power Amplifier.

SW4: Used to change channels. The transceiver uses the binary outputs to detect the position of the channel switch.

Toggle Switches: Program switch SW1 for a variety of functions. Switch SW2 is used to select between internal and external audio speakers.

Front panel buttons: Keypad depressions on the front panel are detected by the scanning outputs from the transceiver. Keypad depressions on the optional DTMF microphone are detected by the DTMF decoder on this board and are processed as ordinary scan-in signals by the transceiver.

DTMF keypad processing: The optional DTMF can be used to program the radio. Keypad depressions generate a DTMF tone in the audio output. This signal is routed to DTMF detector U6, and digital outputs are sent to1-of-16 de-multiplexer U2. The outputs from U2 are used to control analog switches U3-5. In this way the transceiver scan-out lines can be connected to the appropriate scan-in lines to simulate a physical switch closure.

PTT processing: In normal operation, a PTT switch closure causes Q2 to conduct, which in turn causes Q7 to conduct. This signal is distributed to the rest of the radio as the PTT signal. When a DTMF button is depressed, the transceiver automatically transmits this tone.

PTT lockout: To prevent transmission of DTMF tone during programming, a latch circuit is provided to lockout PTT. When the ENTER button is pressed the PTT signals is disabled by a latches circuit. When the ESCAPE button is pressed the lockout latch is reset. It is recommended to utilize the PTT condition lockout during programming the PTT (light will stay off). This is done by pressing ENTER key and after that hold the PTT key depressed until programming is done. To re-key the radio release PTT and key the radio once the radio is out of the programming mode use the ESC key quit programming.

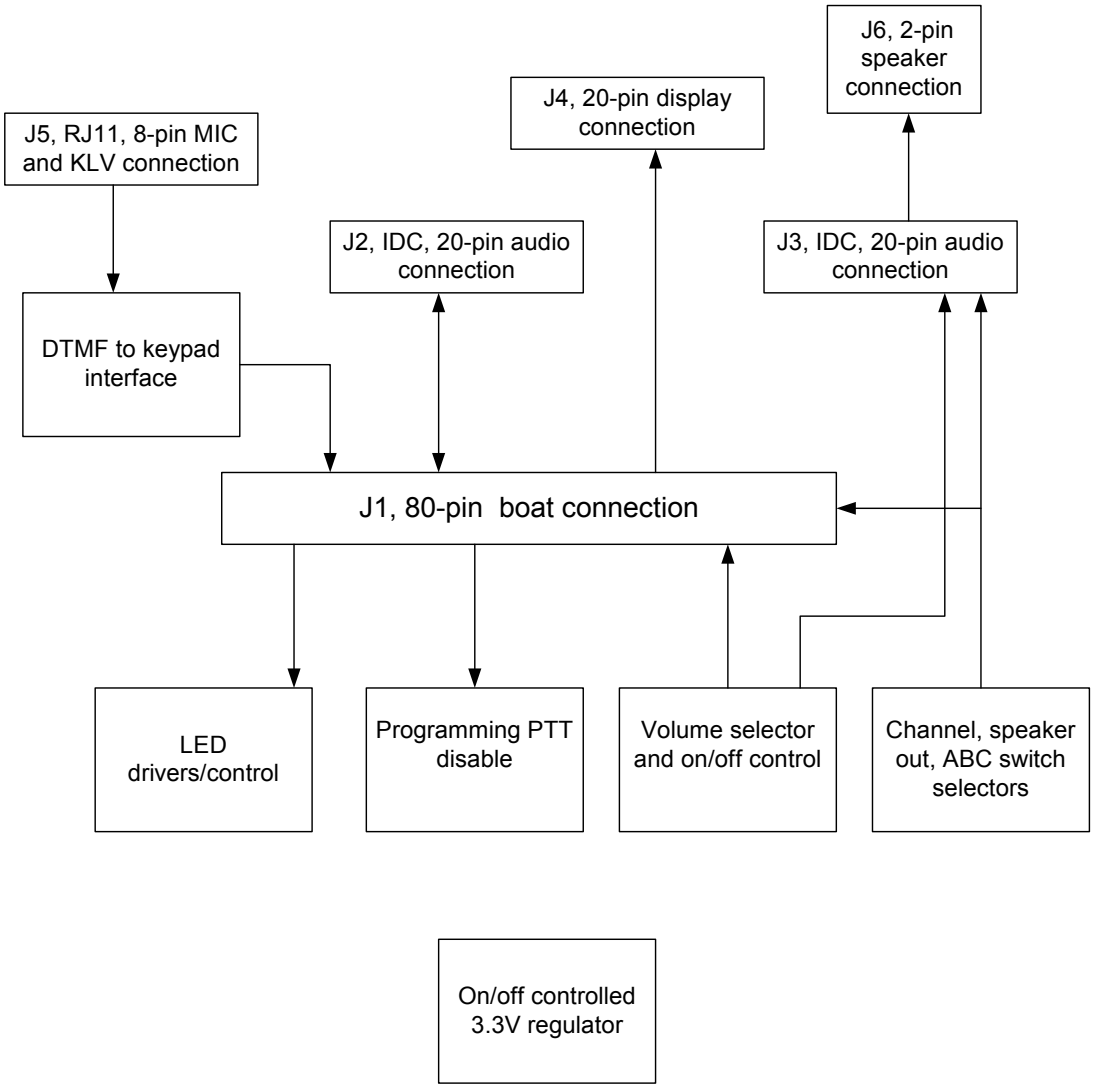

Figure 2-5: Interface Board

CHAPTER 3: SOFTWARE THEORY OF OPERATION

3.1 Functional System Operation

3.1.1 General

All control and channel software is resident in the RECM.

3.1.2 Guardian Block Diagram

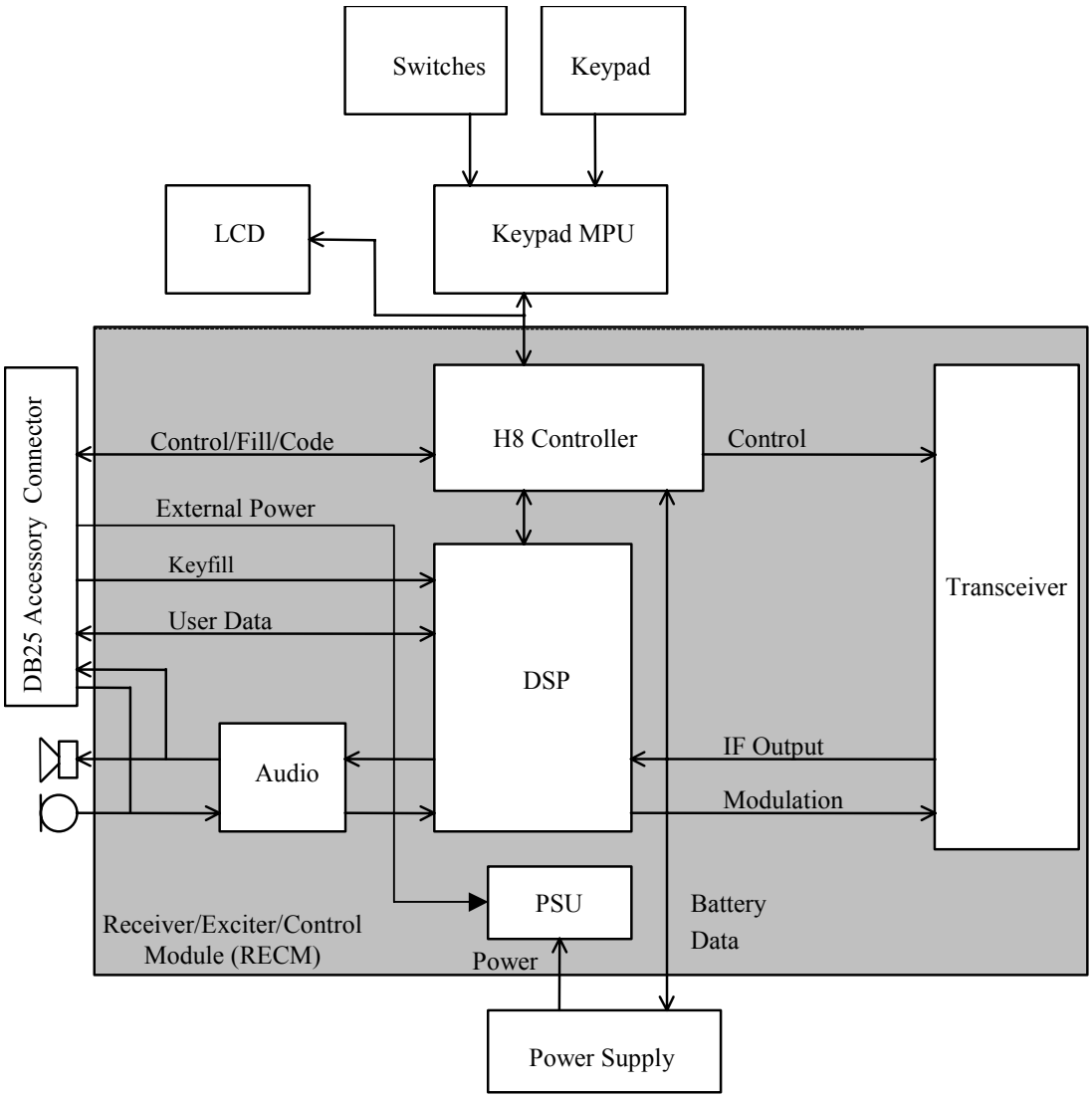

Figure 3-1: Software Theory of Operation Block Diagram

3.1.3 Architecture

A single digital signal processor (DSP) handles all signal-processing functions. An H8 microcontroller is used to control the user interface and implement other radio control functions. All references to signal names relate to the Receiver/Exciter/Control Module (RECM). Functionality partitioning is shown in Figure 1-1.

3.1.4 Board Identification

The control logic stores an electronic serial number and modification status within nonvolatile storage on the board.

3.1.5 Self-Test on Power-Up

The software automatically executes a self-test when the radio is switched on. This test is capable of detecting and identifying faults that prevent the radio from properly operating.

3.1.6 Flash Software Upgrades

The radio software is updated if required using a PC and the Guardian G25AXG004 PC Programming/Cloning cable.

3.1.7 Voice Coder/Decoder (VOCODER)

The VOCODER uses an improved multi-band excitation (IMBE) voice-coding algorithm as specified in the telecommunications industry association and electronic industries alliance (TIA/EIA)-102.BABA. The IMBE VOCODER compresses a high-bit-rate waveform into a low-bit-rate data stream suitable for transmission over the channel. The VOCODER operates at a net bit rate of 4.4 kbps for voice information and a gross bit rate of 7.2 kbps after error control coding.

3.2 Radio Control Software

This software controls the transceiver and baseband signal processing functions.

3.2.1 Audio Control

H8 controls the analog audio signal processing. Audio for transmission comes via an external microphone attached to the front panel. It is wired into the microphone amplifier, which is permanently powered.

Audio output is required when a voice message is received or a tone is generated by the user interface. To allow audio output, H8 sets either SPKRON or EXTSPKRON to the internal speaker or the accessory connector. If an external audio accessory is detected by who are you (WRU) <0.5 Vdc, the audio is routed to the accessory connector. Otherwise audio is routed to the internal speaker. The 16-position volume control knob is decoded and sent to the DSP through the controller software to control the output audio volume.

3.2.2 DSP Control Software

The DSP implements most of the baseband signal processing in the radio. Its function is controlled through its host port by the H8 controller. The DSP operates in a number of basic modes controlled by H8 through the host port. They are as follows:

Mode	Description
Idle	Current shutdown mode released through the host port
Searching	Actively looking for a signal on the IF input signal
Searching paused	Search algorithm paused for an economize cycle or frequency change
Active receive	Actively receiving a message, initiated by detecting a signal or H8 command
Transmit	Actively transmitting voice or data
Keyfill	Keyfill operations and key
Management	Management tasks

The DSP pages-in different program images from the Flash for different modes of operation. Typically one image is used for receive and standby modes, but a new image is needed for transmit and key management operations. The DSP can interrupt the H8 controller, and then pass data over the host port back to H8. Interrupts from the DSP include the following events:

- Signal detected with type data
- Signal lost
- DSP BIT errors
- Paging request

In all active modes the H8 software must be able to write a number of parameters to the DSP and also read back a number of parameters from the DSP. This is implemented through the host port. The parameters used include:

Mode	Description
Search	Reference oscillator temperature used by DSP to correct frequency offsets. AGC reset control is used at start of search period
Analog setting	BW, squelch tones, squelch code, and squelch level
Digital setting	Data rate, key, and algorithm
Project 25 setting	NAC and TGID
CVSD setting	Continuously variable slope delta (CVSD). Data rate
Receive	Reference oscillator temperature used by DSP to correct frequency offsets. Audio volume
Analog setting	Squelch controls, de-emphasis, and companding
Digital setting	Data rate and key algorithm
Project 25 setting	NAC, TGID, BER, and test mode
CVSD setting	Data rate and key
Project 25 setting	Read by H8: SS bits, low-rate data (for future use), and sender ID
Transmit	Reference oscillator temperature used by DSP to correct frequency offsets. Audio volume, sidetone on/off
Analog setting	Squelch controls and de-emphasis
CVSD setting	Data rate and key
Project 25 setting	NAC, TGID, key and low-rate data (for future use)

3.2.3 Transceiver Board

The Transceiver board is controlled through a synchronous serial bus from H8 to the transceiver allowing H8 to control the synthesizer, two 4-channel 8-bit digital to analog converters (DAC), and a control shift register in the transceiver board. Some of the DAC channels are set according to data in the transceiver's electronically erasable read-only memory (EEPROM) calibration tables.

3.2.3.1 Mode Control

The transceiver shift register and the CTX output of the field-programmable gate array (FPGA) control the modes of operation (transmit, receive, or standby). The outputs are controlled as below:

Mode	Description
Spare (SR bit 1)	Spare
3.3VRXSynth (SR bit 2)	Set in active receive mode, RXVCO enable
3.3VTXSynth (SR bit 3)	Set in active transmit mode, TXVCO enable
3.3VRXEnable (SR bit 4)	Set in active receive mode, receiver enable
Spare (SR bit 5)	Spare
Spare (SR bit 6)	Spare

Mode	Description
TX/RX (SR bit 7)	Set in active transmit mode, front end TX/RX control
STD/SIDE (SR bit 8)	Set to use radio antenna, reset to use accessory connector RF port
CTX (FPGA output)	Set in active transmit mode to enable the RF power amplifier

3.2.3.2 Frequency Control

The frequency of operation in both transmit and receive is controlled by the H8 setting in the synthesizer through the serial bus. To set the desired frequency, the appropriate TX or RX synthesizer enable S-R bit must be set, the serial data loaded into the synthesizer chip, and the DAC2 output A synthesizer coarse tune set to the appropriate value for the frequency according to the EEPROM calibration table. Synthesizer lock is monitored by the out-of-lock (OOL) input. Once the synthesizer lock is achieved, the transmitter or receiver is enabled with the appropriate control bits 3.3VRX enable, CTX, and TX/RX. Economizing the synthesizer function is implemented by controlling the 3.3VTXS/RXS bits and by controlling the EM main divider enable bit in the synthesizer control word. If the frequency is unchanged, the synthesizer serial data need not be reloaded when coming out of economize**.**

3.2.3.3 12-Bit DAC

DACLDA, DACADCCLK, and DACDOUT control the 12-bit DAC for IFAGC, TXVCOMOD, REFOSCMOD, and VATT.

3.2.3.4 Reference Oscillator Temperature Compensation

The H8 software constantly monitors the reference oscillator crystal temperature using the XTALMON line. The temperature data is used to lookup the compensation factor in the transceiver's EEPROM calibration table. This compensation factor is written into the DSP, added as a dc offset reference oscillator modulation signal, and used as a dc offset in receive mode.

3.2.3.5 Receiver Control

Setting 3.3VRXE enables the linear receiver chain. The DSP implements software AGC system to control the gain of the linear receiver chain. The H8 controller monitors the actual received signal level by reading RSSI. At all times during receive the RXVTF DAC2 output C must be set to the value in the EEPROM calibration table corresponding to the receive frequency used. This makes the receiver's front-end tunable filter centered on the desired frequency. At all times in receive modes the second LO DAC2 line output B must be controlled using data from the EEPROM calibration table and indexed with oscillator temperature data XTALMON. The temperature compensates the second LO in the receiver chain.

3.2.3.6 Transmitter Control

The radio uses a complex H8 software-based algorithm to dynamically control the transmit power of the radio. The inputs to the power control algorithm are: requested power level (0.1W, 0.5W, 1W, 2W, or 5W), PA calibration data in the EEPROM, supply voltage BATMON (used for monitoring), transmit frequency, PA current, (used for monitoring), and PA temperature (used for monitoring).

The power control algorithm takes these inputs and uses them to control the following outputs to provide a steady RF power output with a clean rise and fall at switch on/off.

Output	Description
PWRSET (DAC1 output A)	Sets the power level in the power amplifier ALC loop
PABIAS1 (DAC1 output B)	Adjusts the bias in the final driver stage
PABIAS2 (DAC1 output C)	Adjusts the bias in the final driver stage

3.2.3.7 TX/RX Switching

The procedure needed to quickly switch the transceiver from receive to transmit and back again is to shut down the current mode, lock the synthesizer in the new mode on the new frequency, and enable the transmitter or receiver, as required.

3.2.3.8 Receiver Scanning

In some scanning modes it is necessary for the radio to scan a number of channels looking for traffic, as controlled by the H8 software. The basic requirement is to change the synthesizer frequency, RXVTF, synthesizer tune DAC, and to resume searching on the new frequency. The DSP may have to be informed of new traffic settings on which to search, for each new frequency. Scanning is interrupted when the DSP detects a signal of interest.

3.2.4 DC Power Control

The H8 controller software controls the power supply switching in the radio. The control software algorithm uses the following inputs:

Input	Description
/PWROFF	Indicates the current position of the radio on/off switch and the accessory connector off line
WRU	Indicates if the radio is fitted into a harness providing external power
/LBOUT	Indicates the supply voltage is at the minimum required for correct operation
BATBUS	Not used in the mobile configuration
BATMON	Indicates the voltage on the main radio supply from external power source

These inputs are used to control the following FPGA outputs:

Output	Description
PWRHOLD	Set during normal operation, the radio stays on regardless of the on/off switch. When PWROFF indicates that a switch off is required, software shut down is executed followed by a release of this output
BATOFF	Not used in the mobile configuration

Additionally the /LBOUT interrupt is used to execute a fast shutdown of the software when the supply voltage drops below that needed for normal operation, or when the power source is removed without switching the radio off.

3.2.4.1 Power Supply Frequency Control

The power supply software controls the switch mode power supply frequency output according to the RF frequency used. The frequency is checked and changed if necessary at every synthesizer frequency change.

3.2.5 Monitoring

The H8 software monitors the following signals:

Signal	Description
Out-of-lock	In all active modes, every 100 ms
EPTT/RTS	In all modes, every 20 ms
RSSI	In receive modes, every 100 ms
WRU	In all modes, every second
DC voltage	In all modes, every 5 seconds
PA temp	In transmit modes, every second
REF temp	In all modes, every 5 seconds
PA current	In transmit modes, every second

3.2.6 Radio Control Drivers

A number of low-level software drivers are used by H8, which interface to the transceiver hardware.

3.2.6.1 Audio and Power Supply Unit (PSU) Driver

A serial interface driver controls the output bits of a serial-to-parallel output shift register in the FPGA. Clock and data source for this shift register is the same serial port used for the user interface serial bus, but data is directed to the shift register using high-order H8 address lines.

3.2.6.2 Transceiver Serial Bus Driver

A serial interface driver controls the transceiver shift register, DAC, and synthesizer. It uses a common clock and data line, and three separate strobe lines for each device.

3.2.6.3 DSP Host Driver

The H8 software includes a DSP host driver for controlling the DSP mode of operation, and initial start-up code download.

3.2.6.4 IIC Bus Driver

The H8 software includes a driver that allows the controller software to read and write to the transceiver EEPROM using IIC protocols. The two lines are general-purpose I/O lines controlled on a bit-by-bit basis by the software.

3.3 Digital Signal Processing

The DSP software implements all baseband signals processing in the radio. It processes signals between the user audio and data interface, and the transceiver modulation and intermediate frequency (IF) interfaces. The signal processing provides compatible analog FM modes, common air interface (CAI) compatible modes, and 12 kbps secure CVSD modes.

3.3.1 DSP Transmit Chain

Signal processing while the radio is transmitting depends on the radio's operational mode. The possible modes are clear analog voice FM, CVSD DES voice, Project 25 clear digital voice, and Project 25 DES digital voice. The Transmit DSP Chain block diagram is shown in Figure 3-2. The major signal processing functions of the DSP transmit chain are described in the following paragraphs.

3.3.1.1 Audio Coder/Decoder (CODEC)

The Guardian uses a Texas Instruments® TLV320-AC36 audio CODEC. Data is transferred to and from the CODEC using the DSP enhanced synchronous serial interface (ESSI) 0 port. The data word is 16 bits long. The first thirteen bits are the two's compliment audio sample, and the last 3 are the volume control word in the receive direction (DIN), and zero padded in the transmit direction (DOUT). The DSP currently sets volume control bits for no attenuation. Scaling the signal prior to sending it to the CODEC controls the volume. The sample rate from the CODEC is 8 ksps.

3.3.1.2 Audio Processing Board

The Audio Processing board receives audio input from the audio CODEC, applies filtering and automatic gain control (AGC), and transmits it to the mode-specific formatting module. The audio filter has a passband from 300 Hz to 3 kHz. This board also transmits DTMF tones to the audio CODEC. DTMF over-dial is supported to allow redirection through the phone network via a base station. Data is transferred to and from the CODEC under interrupt service routine (ISR) control.

3.3.1.3 Project 25 Voice Module

The Project 25 Voice module performs framing and conversion tasks. The framing function uses its own task table to build a CAI time-division multiple access (TDMA) frame. This includes compression of the voice signal using the IMBE VOCODER, forward error correction, and encryption. The physical layer task converts a 4.8 ksps dibit data stream into a 48 ksps real sampled waveform, which is then fed to the Modulation module. The physical layer scales each dibit symbol so that the proper frequency deviation is attained. It applies raised cosine filtering for control of inter-symbol interference.

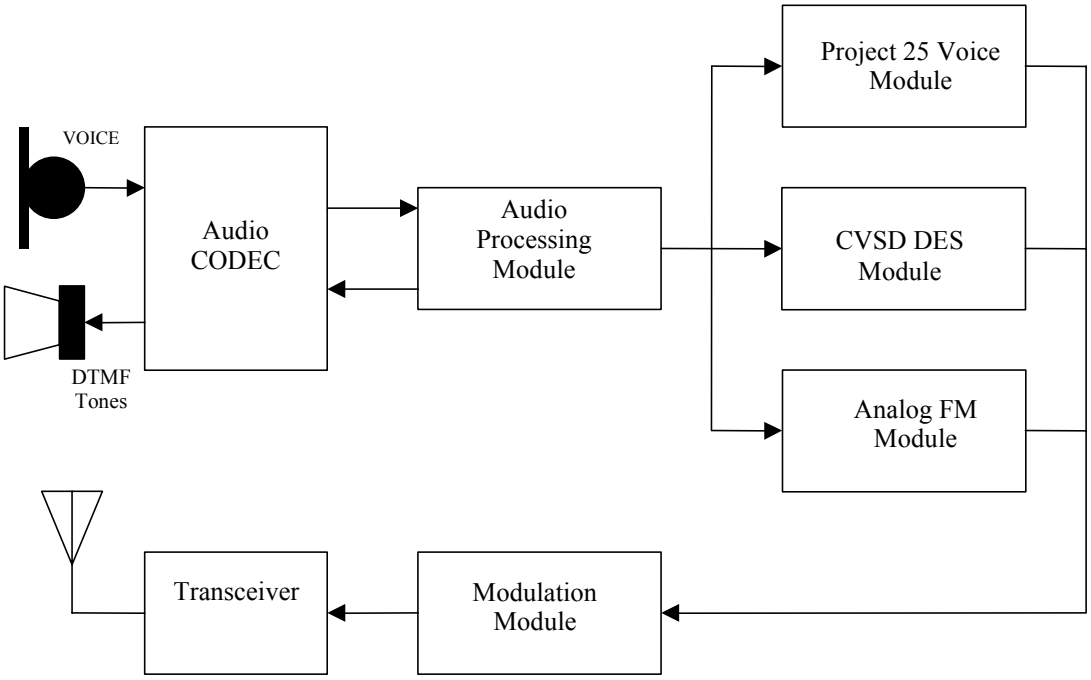

Figure 3-2: Transmit DSP Chain

3.3.1.4 CVSD DES Module

Audio data from the Audio Processing module is sent to the audio circular buffer. The sample rate is increased from 8 ksps to 12 ksps. The CVSD encodes the data and sends it to the transmit CVSD audio circular buffer. The data is DES-encrypted and differentially encoded before sent to the physical interface buffer. The CVSD physical layer converts the CVSD encoded, DES encrypted 12 ksps data stream into a 48 ksps waveform suitable for processing by the Modulation module. The module contains a finite impulse response (FIR) raised cosine filter that acts as an interpolation filter. Transmitting an end of message (EOM) indicator, consisting of 160 ms of alternating ones and zeros, signals the end of a transmission. This allows the receiving radio to squelch the audio output before the radio stops transmitting.

3.3.1.5 Analog FM Module

Audio data entering the Analog FM module is sent through a linear-phase, FIR, audio-shaping filter. Interpolation from 8 ksps to 48 ksps is accomplished using a linear-phase, FIR filter. A single-quadrant sine look-up table (LUT), using fractional addressing and quadrant folding, generates continuous tone controlled squelch system (CTCSS) tones. If the DCS audio turn-off code is transmitted, the tone is fixed at 134.4 Hz and the codes transmitted at a rate of 134.4 bps, derived using the CTCSS tone generator. The DCS data stream passes through a raised cosine filter before added to the speech. The 8 ksps audio stream, with CTCSS/DCS controls, is interpolated to 48 ksps before sent to the Modulation module.

3.3.1.6 Modulation Module

The Modulation module prepares the signal for transmission. The signal is split into a reference oscillator signal and a voltage controlled oscillator (VCO) signal. This allows independent scale and offset values for each signal. A modulation-balance variable scales the reference oscillator voltage, so that the maximum frequency deviation is constant for all RF channels. A transmit modulation variable does the same for the VCO signal.

3.3.1.7 Transceiver Interface

The transceiver DAC has four output ports, two of which modulate the carrier. One of the two channels maintains carrier frequency accuracy. On transmit channel changes, the controller provides the DSP with two fractional values used to scale the two signals output from the DAC. The controller provides the DSP with an additional integer value at one second intervals, and is added to one of the DAC output signals to control carrier frequency accuracy. The modulation interface receives modulation data samples at 48 ksps, independent of the transmit mode. When the radio is operating as a transmitter, the transceiver interface controls the operation of the DAC via ESSI 1 on the DSP. Data is written to the DAC at 96 ksps.

3.3.2 DSP Receive Chain

The radio receive chain hardware consists of an RF transceiver board, analog to digital converter (ADC), a Motorola® DSP 56302 or DSP 56309, and an audio CODEC. The Receive DSP Chain block diagram is shown in Figure 1-3. The major signal receive functions of the DSP receive chain are described in the following paragraphs.

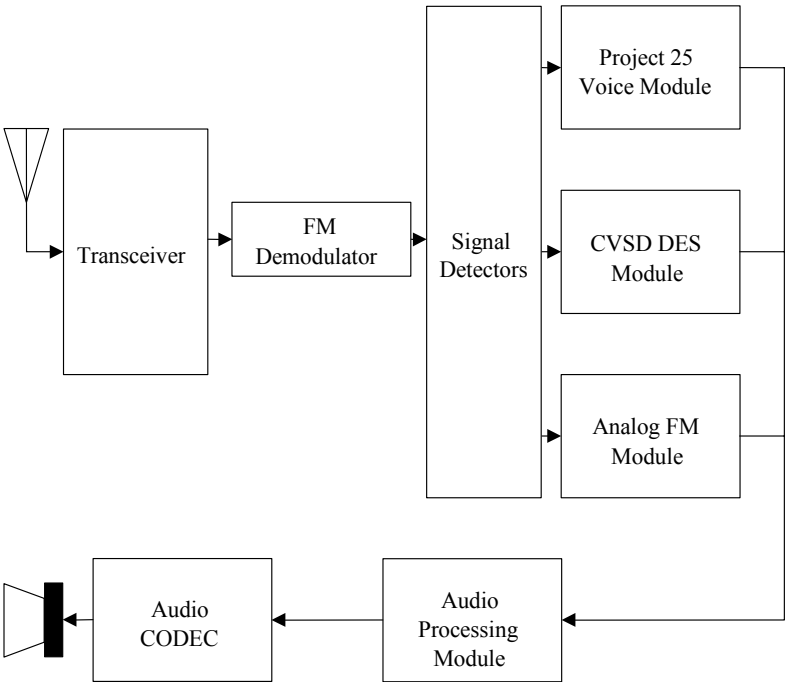

Figure 3-3: Receive DSP Chain

3.3.2.1 Transceiver

The RF transceiver board performs mixing and filtering of the received signal to produce a 455 kHz, 25 kHz bandwidth (BW), IF signal. The output signal from the transceiver is digitized by the ADC and fed to the DSP. The bulk of signal processing is performed by the DSP. An ISR that implements the transceiver/ADC/DAC interface is called at a rate of 96 kHz in receive modes. The ISR reads ADC output data, stores the values in a circular buffer, and controls data transmission to the DAC.

3.3.2.2 FM Demodulator

The FM demodulator converts the FM output of the transceiver to a real-valued, baseband signal. FM demodulation is implemented by a discriminator task. Sub-sampling the 455 kHz IF at 96 kHz folds down the signal to 25 kHz. A mixing function mixes the sampled IF data in the input buffer before filtering. For 12.5 kHz channels, a second

filter is applied to the IQ data stream. Calculating the angular difference between consecutive IQ pairs demodulates the received signal.

3.3.2.2.1 Analog to Digital Converter

Because the signal BW is much less than the 455 kHz carrier frequency, the ADC sub-samples the 455 kHz IF producing a frequency translation as part of the sampling process. The ADC sampling rate is 96 ksps.

3.3.2.2.2 25 kHz Frequency Translation

The 25 kHz frequency translation converts the signal image into a baseband signal, centered at 0 Hz. The DSP implements the digital equivalent of a mixer to perform frequency translation.

3.3.2.2.3 IF Filtering

The complex baseband signal is sent through two linear phase FIR filters. The first IF filter is used as a decimate by two, polyphase, FIR filters and applied to the 96 ksps, complex, baseband output of the 25 kHz mixer. This filter removes some of the out-of-band noise produced by the nonlinear analog components of the transceiver. CVSD DES and analog wide modes have a 25 kHz BW and the first IF filter is the only filtering performed for these modes. Project 25 and analog narrow modes have a 12.5 kHz BW. The second IF filter provides the filtering required for these modes and is applied to the 48 ksps output of the first IF filter.

3.3.2.3 Signal Detectors

The radio uses three signal detectors to detect the presence or absence of a modulated signal in the tuned channel. These signal detectors search for Project 25, analog FM (including noise, CTCSS, and DCS), and CVSD DES signals.

3.3.2.3.1 Project 25 Detector

The Project 25 frame detector detects a Project 25 signal by searching for the frame synchronization (FS) signal and network identifier (NID) embedded in the preamble of every Project 25 data unit. The detector uses this information to perform bit recovery and packet identification. It processes and buffers the binary data for use by the Project 25 Voice Module. Once a target signal is detected, the radio disables squelch using an enable transmit function, so the user can monitor the signal. If the detected signal is lost, squelch is enabled by the shutdown active receive function.

3.3.2.3.2 Analog FM Detector

The analog FM detector uses a function to decimate the incoming data stream by six, to run the noise detector, CTCSS single-tone detector, CTCSS multi-tone detector, and the DCS multi-code detector. A noise squelch detect function detects the appearance of a carrier by searching for a drop in power in a frequency band just above the audio band. In the analog noise detector, the input data is scaled and high-pass filtered, then rectified and scaled again. Then the data is low-pass filtered. The output of the low-pass filter is used to determine whether or not a signal is present.

The detector has two states, searching and locked. If the detector state is searching and the detected power drops below the lower squelch threshold, the detector state transitions to locked. Conversely, if the detector state is locked and the detected power rises above the upper squelch threshold, the detector state transitions to searching. Upper and lower threshold values are BW dependent and can be adjusted at run time.

The multiple-value DCS detector searches for a 134.4 bps bit stream in the sub-audible frequency band used for DCS codes. If found, the code is extracted and appropriate state variables updated. Code extraction is performed in two steps: input data is converted to a binary bit stream, and then data extraction and code comparisons are performed.

The conversion of the input data to a binary bit stream starts with the 8 ksps input data sent through a decimate by six, FIR filter to produce a 1.33 ksps, real valued data stream. This filter removes any signal energy outside of the sub-audible frequency band. The data is then split into two paths. The lower path estimates the dc content of the signal with a narrow low-pass infinite impulse response (IIR) filter. Subtracting the lower path signal from the

upper path signal removes the dc component from the upper path signal. Following this, the resulting signal passes through a single-bit quantizer and the output buffered for use by the code removal step. Data extraction and DCS code comparisons are then accomplished.

3.3.2.3.3 CVSD DES Detection

Detection of CVSD DES waveform is performed by a secure detection function. This function also recovers the 12 kbps bit stream from the 48 ksps input signal. The detector looks for a 12 kbps data stream to determine if a CVSD signal is received.

3.3.2.4 Project 25 Voice Module

The physical layer task extracts FS, NID, SS symbols, and data. All other dibits are passed to the receive framing task. The module performs recovery and symbol extraction based on frame synchronization using a correlation detector. Symbol extraction and error-correction decoding follow carrier frequency offset compensation. VOCODER data and Project 25 framing data is removed and secure mode decryption performed. The VOCODER converts the compressed voice data stream to a 8 ksps audio data stream that is sent to the Modulation module.

3.3.2.5 Analog FM Module

The analog FM module performs two tasks. The detection task uses an FIR filter to down-sample the FM demodulated bit stream from 48 ksps to 8 ksps. It then uses four detectors (noise, single-tone CTCSS, multi-tone CTCSS, and multi-code DCS) to determine signal squelch. The post-detection audio-shaping task applies de-emphasis on/off filtering to a received clear analog signal.

3.3.2.6 CVSD DES Module

The CVSD DES module consists of a 12 kbps clock detection/recovery task, a 12 kbps symbol resolver, a differential decoder, a DES decoder, a 12 kbps CVSD decoder, and a 12 ksps to 8 ksps sample rate converter. The input to the clock detection algorithm is a 48 ksps data stream, representing the sampled FM demodulated carrier. To allow for variation in carrier frequency, the dc component of the demodulated carrier is removed before zero-crossing detection. From a zero-crossing phase profile, a decision can be made whether a 12 ksps data stream is present on the demodulated carrier, or a 12 kHz clock recovered for usage within the 12 kbps symbol resolver. Differential encoding of the binary FSK modulation ensures compatibility between manufacturers, so that either a positive or negative frequency shift can be used to represent a 1 symbol. In the CVSD receive chain, differential decoding precedes one-bit cipher feedback DES decoding. To conserve memory and aid processing efficiency, all symbols (encoded and decoded) are packed in memory. The 12 kbps CVSD decoder is modeled after FED-STD-1023.

The decoder consists of a modulation level analyzer (MLA), a syllabic filter, a pulse modulator, a principal integrator and a comparator. The output of the CVSD decoder is at 12 kbps and must be changed to 8 ksps for output by the CODEC.

3.3.2.7 Audio Processing Module

An audio receive task function and an audio filter is used to output Project 25, clear analog, or secure analog speech samples to the CODEC. When in active receive modes, the ISR is enabled and the task outputs data to the CODEC circular buffer as data is written to it's audio input circular buffer.

3.3.2.8 Audio CODEC

The audio CODEC and the DSP interface uses the DSP ESSI 0 port. The serial clock to the CODEC operates at 2.048 MHz, and is derived from the DSP internal clock. ESSI 0 is configured to operate using a frame rate divider of 16 and a word length of 16 bits, transmitting packets of encoded audio to the CODEC at 8 kHz. The CODEC is used in a linear decode mode, where 13 bits are used to represent the full audio range. The post-processed DSP signal is fed to the audio CODEC, which converts the signal to an analog waveform, applies gain, and routes it to the appropriate output device.

3.3.3 DSP Software

The program data for the DSP is stored in 64K Flash program blocks. The data is stored as unpacked bytes. The blocks used for the DSP software are dedicated so that selective upgrades of this code only are possible.

3.4 Keypad MPU Software

3.4.1 Overview

The keypad microprocessor unit (MPU) provides an indirect interface via the Motherboard to the DTMF keypad and front panel switches. It communicates with the main controller via a synchronous bi-directional serial link.

3.4.2 General

The software is designed so that processor activity and current consumption is minimized. The only continuous operation required is keypad scanning and switch reading. An external clock at 1.5 MHz clocks the keypad. The hardware reset is supplied from the main controller.

3.4.3 Keypad Scanning

The keypad scanning software continuously scans the keypad at a rate of a row every 10 ms. A debounce period of 40 ms is used on key presses and key releases. The software deals with simultaneous key presses and key rollovers, making only single key presses valid. Debounced and validated key presses are passed to the serial data output buffer.

3.4.4 Push-to-Talk (PTT) Input

Inputs from the momentary input switches, and the PTT and auxiliary keys, are read every 10 ms and are debounced for 40 ms. The validation software filters out simultaneous presses of the auxiliary keys and the key rollover between them. Simultaneous presses of the PTT switch and one auxiliary key are allowed. Debounced and validated auxiliary key presses and PTT press and releases are passed to the serial data output buffer.

3.4.5 Switch Input

Inputs from the rotary switches and toggle switch are read at least every 40 ms. Changes in state are debounced for 100 ms. Debounced new switch positions are passed to the serial output buffer.

3.4.6 LED Output

The outputs to the LED are controlled under instruction from the serial port. It is possible to set both outputs off, set the red LED on, set the green LED on, set both LEDs on (orange), and to flash either or both on a 50% duty cycle at a controlled rate of approximately 1 Hz.

3.4.7 Backlight Control

The two LCD backlight controls for setting bright and dim operations are controlled under instruction from the serial port. The keypad uses a fixed level backlight operation. A timeout facility switches off the backlight after 30 seconds if not requested by the main controller.

3.4.8 Serial Interface

The keypad controller implements a synchronous bi-directional serial interface using its serial port allowing it to interface to the main controller. The main controller always sources the serial data clock. To allow autonomous transfers from the keypad controller, a separate keypad interrupt line is provided with the interface. The interrupt line is used to request 8 clocks from the main controller to transfer data from the keypad. The LCD chip select (CS) input line is used to distinguish between serial data for the keypad controller and LCD driver. The serial interface supports the following transfers:

- Keypad to controller including:

Keypad power up okay
Keypad error 1-n
Key press 1-16
Key release 1-16
PTT press
PTT release
Volume switch 1-16
Channel switch 1-16
Toggle switch 1-3
Auxiliary key press 1-3
Emergency key press

- Controller to keypad
- Request current switch status
- Reset and execute BIT test
- Backlight off/bright/dim
- LED off/red/green/yellow/flash/flash rate
- Key press request and interrupt acknowledge

LCD data transfers are in blocks of 80 bytes maximum, allowing a pause on the serial interface at least every 100 ms for the keypad MPU to assert the interrupt and transfer key press or switch change data. During the LCD data transfers, the key data are buffered into the keypad MPU.

3.5 Data Interface

The DSP incorporates a user data interface through its SCI port.

3.5.1 CAI Data Interface

The DSP supports an asynchronous data interface for CAI modes using its SCI port. This interface conforms to the CAI data peripheral interface. It uses standard V24, and RS232 baud rates up to 9600 baud. The software also controls the associated flow control signal data of the terminal ready (DTR) input to the DSP, and the clear to send (CTS) output from the DSP. The request to send (RTS) input to the radio for this interface is processed by H8.

3.5.2 Synchronous Serial Data Interface

The DSP supports a 12 kbps synchronous serial port using its SCI port. The interface is half duplex, uses a DSP generated clock, and includes minimum data buffering within the DSP and RTS/CTS flow control on the transmit function.

3.5.2.1 Receiver Synchronous Serial Data Buffering

In receive synchronous serial data modes the DSP software uses a variable length first-in first-out (FIFO) buffer to cope with differences in clock rates between the transmitter and receiver.

3.5.3 CAI Data Link Layer

This software provides the link between the raw voice and data bit streams, in addition to the data formats required to implement a 9.6 kbps CAI compatible interface.

3.5.3.1 CAI Transmit Voice Mode

The DSP software takes the 144 bit voice code words (encrypted or not) and a number of link control fields set by the host H8 or from the DES system, and formats CAI-compatible logic link data units.

3.5.3.2 CAI Transmit Voice Test Modes

The DSP software is capable of transmitting the CAI voice silence test pattern, the CAI 1 kHz test pattern and a 9 x 144-bit (1296) PRBS test pattern used for error rate tests. The H8 controller controls these test modes.

3.5.3.3 CAI Receive Voice Mode

The DSP takes the 9.6 kbps CAI-compatible data stream and framing, and splits out the voice data for passing to the VOCODER. The DSP decodes the link control words so that the host H8 can read the link control fields, and the encryption synchronization information is available to the encryption process. CAI receive processing is initiated by the frame synchronization correlator trigger. When this is asserted the next 64 bits of network identifier (NID) data are decoded and checked. If the NAC code matches the one selected for the channel, voice or data processing proceeds, otherwise the physical layer is forced into search mode.

3.5.3.4 CAI Receive Voice Test Mode

The DSP software is capable of testing the 9 voice code words received in a CAI frame against a known 9 x 144 PRBS segment. The total number of errors in that frame is then output to the H8 controller. The H8 controller controls this test mode.

3.5.3.5 CAI Transmit Data Mode

The DSP selects the user data (encrypted or clear) and a number of link control fields set by the host H8 or from the DES system, and formats logic link data units compatible with the CAI at 9600 bps.

3.5.3.6 CAI Receive Data Mode

The DSP selects the 9.6 kbps CAI-compatible data stream and framing, and splits out and decodes the data for passing to the user data port. The DSP decodes the link control words so that the host H8 can read the link control fields, and the encryption synchronization information is available to the encryption process.

3.5.4 Transmit Physical Link Layer

This software uses common modulator interface software and a number of mode-dependent, physical link layer software modules.

3.5.4.1 Transmit Modulation Interface

The software provides a common interface to the dual modulation, DAC in the transceiver through its SSI serial port 1 for all transmit modes. In transmit modes, the SSI uses an externally sourced clock at 3072 kHz. This interface takes frequency deviation samples at 48 kHz, and writes each value scaled by a fixed number set by the host to both the reference oscillator DAC and the VCO DAC. Additionally a host-controlled dc offset is added to the reference oscillator DAC value.

3.5.4.2 Transmit CAI Physical Link Layer

This software takes the 9.6 kbps CAI-compatible data stream and converts it to 48k samples of frequency deviation data. To achieve this the software implements the dibit for symbol mapping, Nyquist, and shaping filters as described in the CAI.

3.5.4.3 Transmit Analog FM Physical Link Layer

This software takes the 8 ksps filtered audio and converts it to 48 ksps of frequency deviation data compatible with TIA/EIA-603 in 12.5 kHz and 25 kHz modes. The signal processing uses additional high-pass filtering to reduce the energy in the DCS tone band, audio band pre-emphasis if required, DCS tone addition, and deviation limiting and smoothing. The software is capable of operation in 12.5 kHz, and 25 kHz channel spacing with appropriate deviation scaling. It is capable of appending a phase reversed tone burst of 180 ms as defined in EIA-603, generating DCS and audio turn-off codes, and companding the voice signal in 12.5 kHz mode.

3.5.4.4 Transmit CVSD Physical Link Layer

The transmit CVSD physical link layer converts the 12/16 kbps CVSD data stream and converts it to 48 ksps of frequency deviation data. The software implements a pre-modulation filter with raised cosine time response and 100% eye height.

3.5.5 Receive Physical Link Layer

This software uses common FM demodulation software, and mode-dependent receiver physical layer software modules.

3.5.5.1 Receive ADC and DAC Interface

In receive modes SSI port 1 is used in a duplex manner to allow the ADC to be read continuously at 96 kHz and the DAC written up to 48 ksps for AGC and reference oscillator adjustment. In receive modes, the SSI port is clocked at 1536 kHz from an external clock source, using a 16-bit cycle. At every cycle a value is read out of the ADC. At every other cycle a value may be written to one of the DAC channels to control the AGC and reference oscillator.

3.5.5.2 FM Demodulator

This software provides a common interface to the 96 ksps IF signal at SSI port 1 and produces 48 ksps of frequency deviation data for use in all modes. The SSI port uses an external clock at 1536 kHz. The software implements an FM demodulator function using a quadrature mix with a 24 kHz (Fs/4) local oscillator, dual I and Q channel filters, and a frequency estimator. The channel filtering function is programmable-dependent on the channel spacing used. The channel filtering provides the adjacent channel filtering in addition to that provided by the hardware to achieve the radio adjacent channel rejection performance.

3.5.5.3 Receive CAI Physical Link Layer

This software takes the 48 ksps of frequency deviation data and outputs a 9.6 kbps data stream. The software implements an integrate and dump filter and data slicer as described in the CAI. The integrate and dump filter is controlled by a clock recovery function that selects one of ten possible phases for output to the slicer. The slicer incorporates an averager with a time constant of at least 100 bits, to correct for dc offsets in the received signal.

In parallel with the above, a FIR correlator searching for the CAI fixed framing sequence of 24 symbols operates on the filtered 48 ksps of frequency deviation data. The correlator operates at 10 samples per symbol. The correlator phase with the highest correlation peak selects the clock phase for use in the integrate and dump filter and slicer. This correlator operates continuously when searching for CAI traffic and occasionally when tracking an CAI signal when subsequent frame syncs are expected. The correlator trigger is used to provide a framing signal for the subsequent CAI link layer processing.

3.5.5.4 Receive Analog FM Physical Link Layer

This software takes the 48 ksps frequency deviation data and outputs 8 ksps of audio to the receive audio processing. Software signal processing implements a high-pass filter to remove CTCSS tones and de-emphasis if required. The gain of the signal path is adjusted to cope with the different deviations used on different channel bandwidths. The signal processing signal path is controlled by squelch signals. The software includes audio expanding to reverse the transmit companding.

3.5.5.5 Receive CVSD Physical Link Layer

This software takes the 48 ksps frequency deviation data and outputs 12/16 kbps serial data. The software uses a data filter, a slicer, and a clock recovery function.

3.5.6 DES Encryption

The DSP software implements DES encryption of traffic in the CAI and CVSD modes.

3.5.6.1 DES Kernel

The DSP software implements the DES encryption kernel as described in FIPS 46-2, encrypting 64 data bits using a 56-bit key. It uses output feedback operation or a single bit cipher feedback operation.

3.5.6.2 CAI Encryption

The DSP software uses DES kernel software to implement the CAI encryption of voice traffic as described in TIA/EIA/IS-102.AAAA. The key manager supplies the encryption key. In transmit, the message indicator (MI) vector is passed to data link processing for encoding and transmission. In receive, the data link layer decodes the MI vector, and fly wheeled if decoding fails for up to n frames.

3.5.6.3 DES Data Link Layer

This software encrypts and decrypts the 12 kb of CVSD data using the DES kernel. During transmit, framing synchronization data and the MI vector are inserted into the data stream. In receive, the software searches for and extracts the framing and MI data. Bit definitions and formats are defined in the DES protocol.

3.5.6.4 Key Interface

This software provides an interface for inputting DES encryption keys from the DSP SCI port using synchronous data transfers with an external clock, and for conforming to the Motorola KVL data transfer mechanism and the CAI DES keyfill protocol.

3.5.6.5 Key Bank

The radio maintains a bank of up to 16 encryption keys stored in Flash memory. Associated with each key are a key ID, key data, and an 8-character alphanumeric tag. Each encrypted channel is assigned one of the 16 keys for both secure transmit and secure receive modes. Channel key assignment is accomplished by selecting the corresponding key tag. Upon entering the secure transmit or secure receive mode, H8 transfers the appropriate encryption key to the DSP through the SCI port.

3.5.7 Host Interface

The DSP is controlled through its host interface by H8. It initially boots up through this interface. The host interface is used for DSP mode control, encryption key transfer, link control data transfer, low-rate data transfer, frequency variable data transfer, CTCSS mode control, and initial software download.

3.5.8 Flash Interface

The DSP has direct access to the main radio Flash memory through the H8 bus arbitration logic. This interface is used for software downloads using byte-wide direct memory access (DMA) transfers under host control for mode changes. The DSP software does not write to Flash memory.

3.5.9 Paging

The DSP software is designed so that normal operation does not involve off-chip bus accesses. This means the code size must be limited to 24K words and the data memory to 10K words. A number of program images that correspond to different modes are allowed, with paging of images out of Flash by the DMA at mode changes. The minimum subdivision of images corresponds to the following modes, and a continuously resident core host interface function.

- Initialization/POST
- Receive 12.5 kHz
- Receive 25 kHz
- Transmit 12.5 kHz
- Transmit 25 kHz
- Keyfill

The paging DMA mechanism is controlled by the host H8 and allows the transfer of a program image within 50 ms.

3.5.10 Hardware Control

The DSP software controls the DSP clock rate through the phased locked loop (PLL) output divider. The DSP clock rate is dynamically matched to the mode of operation, in coarse steps for example, between searching and tracking receive modes. The DSP software uses low-current wait modes in pauses between processing to minimize current consumption. The host is also able to request a very low-current idle mode in the DSP. The host releases this mode.

3.6 Controller Software

3.6.1 Overview

The controller software has overall control of the radio; including user interface operations, and the DSP and transceiver. Figure 1-4 is the controller software block diagram.

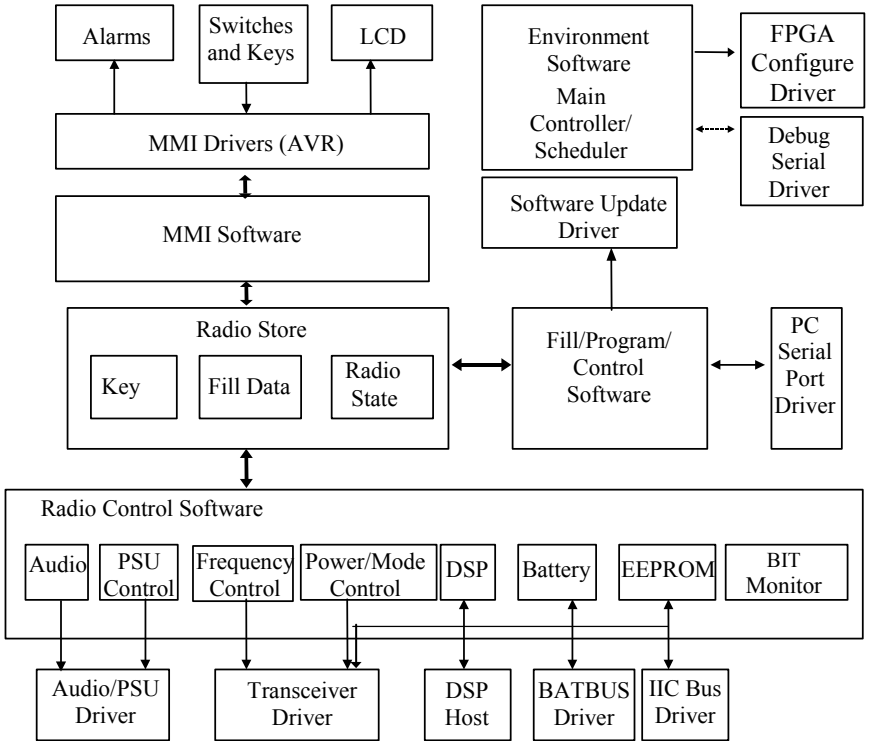

Figure 3-4: Controller Software

3.6.2 Environment

3.6.2.1 General

The H8 controller system is designed for minimum external bus activity and minimum current consumption. These features are provided by the maximum use of low-current standby modes in H8, and an interrupt-driven architecture, with a minimum of input polling. In radio standby and receive modes the only H8 tasks are the control of the transceiver frequency and DSP mode as the radio scans and economizes. The most H8-intensive activities are associated with user interactions, and operations on the fill/program/control port.

3.6.2.2 Scheduler

H8 operates with a simple scheduler that launches tasks after interrupt events. A time base interrupt of 10 ms is used to keep track of time and poll inputs at regular intervals.

3.6.2.2.1 Interrupt Sources

The following interrupt sources are used in H8.

Interrupt Source	Description
User interface	External interrupt from the keypad
DSP	External interrupt from the DSP, signal detected, etc.
Low dc voltage	External NMI from power supply indicates power supply fail
Timer	Internal time base tick interrupt every 10 ms
PC serial port	Internal interrupt from PC interrupt serial port
UI serial port	Internal interrupt from user interface serial port, key press, and LCD data
Debug serial port	Internal interrupt from DMA/timer
Alarm generator	Internal interrupt from DMA/timer

3.6.2.2.2 Polled Inputs

The H8 software polls the following inputs at regular intervals.

Input	Description
EXTPTT/RTS	External PTT and data RTS
OOL	Synthesizer out of lock
PWROFF	On/off switch position
SENSE	External keyfill device detect

The following analog inputs are measured as appropriate to the radio mode of operation.

Input	Description
RSSI	Receiver signal strength
WRU	External device detect
BATT	Main radio 10V supply monitor
PA TEMP	Transmitter temperature
XTAL TEMP	Reference crystal temperature
PA CURRENT	Transmitter current

3.6.2.2.3 Watchdog

A regular watchdog service task is scheduled to prevent the H8 watchdog controller from overrunning, and a hardware reset from occurring. The target watchdog timeout is 100/200 ms.

3.6.2.3 Start-Up Software

3.6.2.3.1 Boot Block Start-Up Software

The minimum simplest start-up software is provided in the boot block of the Flash. This software holds the keypad, DSP, user interface, and FPGA in reset, and then establishes whether a valid H8 program image exists in the program blocks of the Flash. If no valid program exists, a simple alarm sounds. The boot block software includes a minimum basic BIT facility to check the code itself, and the internal and external random access memory (RAM). The boot block code includes the software to allow programming of the program blocks through the PC serial port.

3.6.2.3.2 Full Start-Up Software

If a valid H8 program image exists, the full start-up code executes. This involves initializing RAM, DSP, keypad, user interface, FPGA, transceiver, etc., executing the start-up BIT, and transferring control to the main scheduler.

3.6.2.3.3 FPGA Configure Software

At start-up H8 configures the FPGA using data from the main Flash memory and transferring it via a synchronous serial bus to the FPGA.

3.6.2.4 Shut Down Software

At normal shut down when the front panel on/off switch is off, the H8 software executes a clean shut down to the transceiver, DSP, and user interface (UI), saves any usage data to the Flash, and releases the main power supply. In cases where the power is removed, the low-power interrupt executes a minimum fast shut down, saving RAM data as required, with no Flash update.

3.6.2.5 Debug Driver Software

The H8 controller includes software to implement an asynchronous serial port on two input/output (I/O) pins of H8. Facilities provided include the ability to monitor particular radio variables, and to control specific variables. This port allows PC serial access to the board during board-level factory testing, through the test connector.

3.6.3 Radio Store

All functional areas of the controller software, including the user interface, access the radio data store, fill control, and radio software.

3.6.3.1 Physical Data Storage

The radio data is physically stored in 4 devices, all devices are accessible by the controller software.

3.6.3.1.1 H8 Internal RAM

The H8 controller has 2K x 8 of internal RAM. This data is not retained when the radio is switched off or the power is removed. It is used for short-term storage of frequently accessed variables, stack workspace, etc. to minimize bus activity when the H8 controller is running. The internal RAM is used as program space from which to execute during some Flash update operations.

3.6.3.1.2 External RAM

H8 is provided with an external 128k x 8 bit RAM that is backed up for at least 30 seconds when the radio power is removed, and at all times when a external power is applied with the radio switched off. This device is used as a variable data expansion area, and stores specific user-entered data that must be retained over power interruptions (unlock password, etc.).

3.6.3.1.3 Flash ROM

H8 has a 512k x 16-bit Flash read-only memory (ROM) used primarily for program storage. Data in the Flash is retained permanently. Different areas of the Flash have different characteristics. The boot sector is a 16k block used for the reprogramming software and the radio serial number. The data in this sector is programmed or block-erased only in the factory.

The Flash has 15-64k and 6-8k program blocks that can be block-erased and programmed by the boot block code during normal reprogramming operations, without special equipment and without opening the radio. These blocks are used for H8 and DSP operating software, radio fill data, and FPGA programming data. The Flash has two small 8k parameter blocks used for changing data that must be stored indefinitely, such as user specific settings and usage data.

3.6.3.1.4 Transceiver EEPROM

The radio transceiver has an 8k x 8 serial EEPROM for storing transceiver calibration data. This data is set during production testing for the specific transceiver. The data in this device is essentially constant and is never written to by the main controller. At switch on, contents of the EEPROM are copied into the external RAM; EEPROM is not accessed during normal operation.

3.6.3.2 Data Types

The controller software uses a number of different data types.

3.6.3.2.1 Volatile Variables

Variable data used by the H8 controller that is not retained when the radio is switched off, is stored in the H8 internal RAM and the external RAM.

3.6.3.2.2 Short Term Stored Variables

Variable data retained while the radio is switched off or the power is interrupted, is stored in the external RAM.

3.6.3.2.3 Permanent Stored Variables

Variable data retained indefinitely is stored in the parameter blocks of the Flash. Every time this data changes, a parameter block must be erased, and the new data written into the now blank parameter block.

3.6.3.2.4 Radio Fill Data

The frequencies, modes, and power levels are associated with different channels programmed into the radio. This data is programmed into the radio through the fill port.

3.6.4 Program/Fill/Control Interface

The controller provides a serial port for PC access to allow the following functions:

Function	Description
Programming	To update radio software
Filling	For modifying the radio data store of modes and frequencies, etc.
Control	For controlling the radio operating mode

3.6.4.1 Radio Programming

The controller software allows reprogramming of the Flash memory program blocks, on a block-by-block basis. During these operations, the controller executes from the boot sector of the Flash and no radio or user interface operations are possible. After a programming operation, cycle the power on the radio. Programming operations are initiated on receipt of a specific serial message on the PC serial port.

3.6.4.2 Radio Fill

The controller provides the facilities to modify the system, group, bank, and radio global data through the PC serial port. This interface provides the following facilities:

Facility	Description
Radio erase	Delete all fill data in the radio
Selective erase	Delete (mark as deleted) specific systems, groups, and banks (for future use)
Radio fill	Add specific systems, groups, banks, and global data to the radio store
Radio read	Export the fill data contents of the radio store to the PC

All transfers and operations on the fill port are cyclic redundancy checked (CRC) and acknowledged.

3.6.4.2.1 Cloning

The radio can export channel data to other radios. Data export is initiated by a user interface operation at the exporting radio. The exporting radio emulates a PC programmer during the data transfer. **Cloning of keyfill data is not allowed.**

3.6.4.2.2 Radio Keyfill

The DSP software manages the radio keyfill protocols.

3.6.4.3 Radio Control Port

It is possible for an external PC to control the functioning of the radio. This provides the following facilities:

- Radio status read to export the radio serial number, revision status, history, usage, etc.
- Set external control mode
- Set radio transmit frequency, power level, and mode
- Set radio receive frequency and mode

The transceiver mode control also allows transmission of 1 kHz test tones in analog modes, and BER test patterns in digital modes. The receiver mode control allows the continuous (every 0.5 second) output of the bit error count per frame in digital modes.

3.6.4.4 PC Serial Port Driver

The controller software controls the H8 serial port to implement the asynchronous data formats and baud rates (9,600, 19,200, and 38,400) for the PC serial port. The serial port driver software also controls the 232OFF signal to maintain the RS232 in its low-current standby state, except when data is driven out and while RTS is asserted.

3.7 User Interface

The radio interface is described in the following paragraphs.

3.7.1 Display

The radio has an 80 x 32 dot matrix LCD display. Some of the features of the display are:

Feature	Description
Phone	Indicated by an icon in the top, right of the display (for future use)
Scan	Indicated by SCAN****, SRCH****, or ZONE**** flashing in the top row of the display
Encryption	Indicated by a key icon
Power level	Indicated by HI/LO/2W in the bottom row of the display
Priority scan	Indicated by SCANP1 (P2), SRCHP1 (P2), or ZONEP1 (P2) flashing in the top row of the display
Receive only channel	Indicated by an RX in the bottom, left corner of the display
Talkaround	Indicated by a TA in the bottom, left corner of the display
Repeater mode	Indicated by a receiver icon in the bottom, left corner of the display
Emergency message	EMG displays in the bottom, left corner when the radio is transmitting an emergency message

3.7.2 Optional DTMF Microphone

The radio is programmed using DTMF microphone. For detailed instructions on programming the radio a DTMF microphone, see the Guardian operator manual (G25AMK004).

CHAPTER 4: INSTALLATION, ADJUSTMENT, AND OPERATION

4.1 Radio Configuration

4.1.1 Channels

A channel consists of a receive and transmit frequency pair. The radio has a total of 256 selectable channels. Each channel can be programmed for different receive and transmit frequencies, squelch, modulation, encryption, and power. Each channel can have one of possible 16 keys assigned on a channel-by-channel basis. An 8-character alphanumeric label identifies each channel or by its channel number if no text label. Up to 7 shadow channels can be added to each channel. They enable the radio to be used in several squelch/encryption modes on each physical channel.

4.1.2 Zones

A zone is a group of channels. Each zone can be assigned up to 16 channels. The radio can store up to 16 zones, or groups of channels. The zones can be assigned names of up to 8 alphanumeric characters and assigned to banks during programming. Three zones can be selected by the toggle switch, 16 zones by the front panel keyboard. Channels are mapped to the channel select switch positions using the Guardian PC programmer. When a zone is active (selected), channels within the zone are selected using the 16-position channel select switch on the front panel of the radio.

4.1.3 Banks

A bank is a group of zones. Zones are assigned to banks during programming. The radio can store up to 4 banks of 16 zones each. Banks are assigned names of up to 8 characters.

4.2 Installation and Adjustment

4.2.1 Hardware

Install using the Datron approved bracket.

4.2.2 Software

The manufacturer offers software updates when required. Software updates can be performed via an external port. No radio disassembly is required.

4.3 Operating Procedures

4.3.1 Connect the Power Source

Use only the Datron approved power cable set, negative ground only.

4.3.2 Connect the Antenna

The antenna connects to the radio through a UHF antenna connector. For best VSWR, make sure to match the antenna before operation.

4.3.3 Optional External Speaker

Use the accessory connector on the rear panel of the radio to connect the external speaker.

4.3.4 Radio Programming

Prior to the first time of operation, the radio must be programmed using the Guardian programming kit. For information about programming a radio using the PC programmer, refer to the Guardian programming manual. For PTT lockout during a programming sequence, refer to the Interface board description in Chapter 2.

4.3.5 Radio Power Up

Turn on the radio using the on/off/volume knob. The radio performs a self-test and sounds a short medium-pitched tone to indicate PASS. Use the switch to set the volume to a comfortable level. Select the desired channel using the channel select switch. The process takes 3 to 5 seconds before the radio is ready for operation.

4.3.6 Choose a Channel

The default display shows the current zone and channel. Use the channel select switch to select a different channel in the zone. To change zones, program one of the side keys, program the three-position toggle switch to zone select, or program through the display using the select menu.

4.3.7 Transmit a Voice Message

Press the PTT switch on the palm microphone, hold the radio 2 to 6 inches from your mouth, and speak in a clear voice.

4.3.8 Receive a Voice Message

To receive a voice message, release the PTT. Use the PC programmer or the radio program menu to set or adjust the squelch level, CTCSS tones, DCS variables, NACs, and/or talk-group identifiers (TGIDs) as required.

4.3.9 Programming and Bypass Mode

For description of these features, refer to the Interface board section in Chapter 2.

CHAPTER 5: RADIO SET AND ACCESSORIES

5.1 System Description

The Guardian consists of the following components:

- Receiver/Exciter/Control Module (RECM)
- Front Panel Interface
- Motherboard
- Heatsink Assembly

For available accessories, contact a Datron Guardian representative.

5.1.1 Mobile Radio

The Guardian is a vehicular-mounted transceiver capable of providing secure and non-secure communications over the 136 to 174 MHz RF range. The radio includes an LCD, emergency push button, speaker, microphone, multi-function accessory connector, three programmable function keys, 16-position channel select rotary knob, on/off/volume rotary knob, 3-position programmable toggle switch, antenna connector, dc power connector, and two LED status indicators. The Guardian features adjustable power output ranging from 25W to 110W. Operational modes include:

- Clear analog voice FM, 12.5 and 25 kHz
- DES CVSD modulation voice, 25 kHz, 12 kbps
- Project 25 clear digital voice, 12.5 kHz
- DTMF overdial

5.1.2 Antenna

The antenna is a SO239 (UHF) jack mounted to the rear panel.

5.1.3 Guardian PC Programmer

Note: For some programming features, refer to the Interface board section in Chapter 2.

The Guardian programming kit is compatible with Windows™ 95/98/NT, capable of loading or modifying programming information into the radio from a PC. It includes software, a detailed operator manual, and an RS232 compatible programming/cloning cable. The cable connects the PC serial port to the accessory connector on the rear panel of the radio. See the Guardian programming manual for a complete description of PC programming. The PC programmer is capable of programming the following settings:

BANK	Bank tag
	Special channels: Priority channels 1 and 2, emergency channel, and home channel
	Zones/available zones
ZONE	Zone tag
	Scan list
	Channels/available channels
CHANNEL	Channel tag
	Channel type
	Bandwidth
	Receive only option
	Options: Scan list, talkaround, and locked
	Encryption: Enable, and key
	Transmit Power: High and low RF power levels

	Receive and Transmit Parameters: Operating frequencies, P25 NAC (digital), talkgroup (digital), squelch mode/value (analog), and shadow channels
GLOBAL	User (configuration name)
	User ID P25
	Keys and Switches: Auxiliary switch (1-3) function, toggle switch function, and emergency button function
	Programming Access: Programming enable, and programming password
	Scan: Revert mode, scan delay, scan reply, and monitor time
	Transmit: Transmit inhibit/override, and transmit time-out
	Emergency: Alert mode, duration timer, and repeat timer
KEY	Key tag
	Key ID
	Key data

5.1.4 Cloning Cable

The Guardian G25AXG004 programming/cloning cable is used to transfer programming information (excluding crypto keys and global parameters) from one radio to another radio. The cable connects to the radio accessory connector on both the sending (source) and receiving (target) radios. Each cable end is labeled accordingly (source and target) for ease of use.

5.2 Controls, Indicators, and Connectors

Consult the Guardian operator manual for detailed operating instructions.

5.2.1 Controls

The radio controls consist of a 16-position channel rotary knob, an on/off/volume rotary knob, a 3-position toggle switch, 3 programmable function keys, an emergency push button, a PTT switch, and a 16-button keypad.

5.2.1.1 On/Off/Volume Rotary Knob

The on/off/volume knob located on the front panel of the radio is a 16-position rotary switch. The first position is off, the second position is on with the speaker off (mute), and the remaining positions are used for increasing volume levels.

5.2.1.2 16-Channel Rotary Knob

The channel select knob, located on the front panel of the radio, is used to rapidly switch between the programmable 16 channels.

5.2.1.3 3-Position Toggle Switch

The 3-position toggle switch located on the front panel of the radio is programmed using the PC programmer for zone select, transmit encryption enabled/disabled, scan on/priority/off, high/low power, talkaround on/off, monitor (squelch adjust) on/off, and disabled.

5.2.1.4 External Speaker Switch

The external speaker provides 10W of clear communications audio from the radio. Comes with data and speaker cable. Set the speaker switch to **I** for internal speaker operation, **E** for external, or **B** for both speakers simultaneously.

5.2.1.5 PTT Switch

The PTT switch is located on the microphone.

5.2.1.6 Programmable Keys

Three programmable keys are located on the front panel of the radio. These keys are programmed using the PC programmer for the following functions:

- Backlight dim/bright/off (for future use)
- Encryption on/off
- Scan list add/delete
- Keypad disable (for future use)
- Monitor on/off
- Scan on/priority/off
- Signal strength meter on/off
- Talkaround
- On/off
- Home channel
- Audible tones on/off (for future use)
- Next zone (future use)
- Open microphone (for future use)
- Previous channel (for future use)
- Disabled

5.2.1.7 Optional Emergency Button

Program the emergency button for emergency operation or for zeroize operation. If programmed for emergency operation, pressing the button activates the emergency calling. The emergency condition remains active until cleared by turning off the radio. When the emergency mode is activated, an emergency message is broadcast over the emergency channel. There are two programmable modes: audio (full alert and silent), and display (alert and silent). In full-alert mode, EMERGENCY flashes on the display and an audio tone is sounded. In silent mode, there is no audio tone and no LED indication. If the emergency button is programmed for zeroize operation, all encryption keys contained in the radio are erased.

5.2.1.8 Optional DTMF Microphone

The optional DTMF microphone includes a 12-button keypad with positive feedback on the front panel. The keypad provides adjustable backlighting for nighttime viewing.

5.2.2 Indicators

5.2.2.1 LCD

The radio contains a full graphics 80 x 32 pixel LCD that uses characters and graphics to provide the operator with radio operating information. The display provides backlighting for nighttime operation.

5.2.2.2 LED

The 3-color LED provides the operating status of the radio. The LED is viewable from front panel of the radio and provides radio status as follows:

LED	Indication
Red	Transmitting
Green	Receiving/busy channel indicator
Flashing green	Receiving encrypted transmission
Orange	Emergency/low dc power voltage

5.2.2.3 Audible Tones

The radio has several audible tones that are activated by states of operation or by radio faults. These tones are described in Chapter 9.

5.2.3 Connectors

5.2.3.1 Accessory Connector

The accessory connector is a DB25 connector located on the rear panel of the radio. This connector is used for multiple functions, including PC programming, keyfill, cloning, external speaker, and audio accessory attachment. The pin names and functions are defined in Chapter 10.

5.2.3.2 Antenna Connector

The antenna connector is a SO239 jack.

5.2.3.3 DC Power Connector

The dc power connector is a 9-pin D connector in the rear panel of the radio.

5.3 Transceiver Characteristics

The radio frequency range is 136 to 174 MHz with channel spacing of 12.5 or 25 kHz, tunable in 5 kHz steps.

5.3.1 Transmitter Characteristics

5.3.1.1 Transmitter Output

The transmitter output consists of a single channel FM carrier using either conventional 12.5 or 25 kHz FM modulation, or 12.5 kHz compatible 4-level FM (C4FM). The signal source is analog or digitized voice signals.

5.3.1.2 Transmit Squelch

Transmit squelch parameters are required to enable selective squelch communications options. These parameters are described below.

5.3.1.2.1 Analog Transmit Squelch

There are 3 types of analog transmit squelch:

Type	Description
None	No squelch is included with the analog transmit signal
CTCSS	Sub-audible CTCSS squelch tones are included with the analog transmit signal
DCS	DCS variables are superimposed on the analog transmit signal

5.3.1.2.2 Digital Transmit Squelch

There are 4 types of digital transmit squelch:

Type	Description
None	No squelch is included with the digital transmit signal
Network Access Code (NAC)	A digital NAC is transmitted with the Project 25 digital transmit signal. The primary purpose of this code is to allow the user access to a repeater network
TGID	A digital TGID is transmitted with the Project 25 digital transmit signal. The primary purpose of this selective digital calling identification is to group users into functional teams

Type	Description
Individual Call	TGID is automatically set to 0000 (hex) and the user ID of the targeted radio is activated within the Project 25 digital transmit signal

5.3.2 Receiver Characteristics

5.3.2.1 Receiver Performance

The receiver is capable of demodulating a single-channel FM carrier using either conventional 12.5 kHz FM, 25 kHz FM, C4FM, or compatible quadrature phase shift keying (CQPSK) modulation. The receiver demodulates analog or digital voice and data signals. The radio circuitry receives clear messages while operating in secure mode, and secure messages while in the clear mode, if encryption is enabled.

5.3.2.2 Receive Squelch

5.3.2.2.1 Analog Receive Squelch

There are 3 types of analog receive squelch:

Type	Description
Carrier (noise)	Squelch is opened on any intelligible analog signal
CTCSS	Squelch is opened on any analog signal having the correct CTCSS tone
DCS	Squelch is opened on any analog signal having the correct DCS variable

5.3.2.2.2 Digital Receive Squelch

There are 4 types of digital receive squelch:

Type	Description
Monitor	Squelch is opened on any intelligible digital signal. The NAC and talkgroup ID do not have to match
Normal	Squelch is opened on any digital signal having the correct NAC
Selective	Squelch is opened on any digital signal having the correct NAC and TGID
Individual call	Squelch is opened on a digital signal having a TGID of 0000 (hex) and a user ID matching that of the receiving radio

5.4 Communication Security

The radio is capable of secure communication by means of type-3, software-based encryption, and is fully compatible with any radio using Project 25 DES encryption. When the radio is operating in the secure mode, the transmission of all tone squelch signals is disabled.

5.4.1 Algorithms

The radio is capable of single-bit cipher feedback (SBCF) DES (compatible with other manufacturers) 25 kHz channels.

5.4.2 Keyfill

Keyfill is accomplished through the radio accessory connector using the PC programmer. The PC programming cable is used to load the keys. The radio can store up to 16 encryption keys. The radio retains encryption keys until they are rewritten or zeroized.

5.4.3 Zeroize

The radio can be programmed using an optional, external emergency key to zeroize all encryption keys. Using the programming menu, the radio can also zeroize all encryption keys, or selectively zeroize individual encryption keys. The emergency key is programmed using the PC programmer.

CHAPTER 6: SERVICING THE RADIO

6.1 General

There are no user serviceable parts in the Guardian radio. Return it for servicing to the manufacturer after requesting an RMA number. Attempts to service the Guardian radio by non-authorized personnel voids the warranty.

6.2 Self-Test at Power Up

At radio switch-on, the H8 controller executes a number of tests to confirm correct operation. Any errors are reported to the user through displayed error messages and logged in the Flash. The tests implemented include:

- Flash checksum CRC
- RAM read and write
- FPGA configuration
- DSP host interface
- Keypad interface to AVR
- DC bus interface
- Transceiver EEPROM interface
- Synthesizer lock tests top and bottom frequencies, lock time, etc.

6.3 Caution

Repair of some parts of this unit require special tools and soldering techniques not normally available in a field service environment. DWC highly recommends the module subassemblies be returned to the factory for service. Damage can easily occur from repair attempts by non-trained personnel.

CHAPTER 7: TROUBLESHOOTING

7.1 Introduction

This chapter is included to help qualified service personnel troubleshoot and repair the Guardian radio. If questions or problems arise, contact Datron Technical Support Services Group, Datron World Communications Inc., 3030 Enterprise Court, Vista, CA 92083, or phone (760) 597-3755, or email to: guardianservice@dtwc.com. For additional troubleshooting information, refer to the following sections of this manual:

- Chapter 2: Hardware Theory of Operation
- Chapter 3: Software Theory of Operation
- Chapter 4: Installation, Adjustment and Operation
- Chapter 11: Schematics

This chapter contains basic functional tests. Once the problem is corrected, restart the tests.

7.2 Radio Functional Tests

The tests in this chapter require the radio to be tested as programmed. It is best to program all 3 auxiliary buttons to Hi/Lo power, the emergency button to emergency, and the toggle switch to zone select. Program the radio with eighteen channels, 3 zones, and 1 bank. Put 16 channels in zone 1, 1 channel in zone 2, and 1 channel in zone 3. For all of the channels, use assigned transmit and receive frequencies, turn transmit squelch off, and set receive squelch to carrier, level 8. When more than one remove and receive tasks are shown in a block, they are listed in order from most to least probable for fixing the problem. It is recommended that the remove and repair tasks are tried one at a time, and the radio re-tested until the problem is fixed.

The tests outlined below provide an overall check of the radio to ensure it is working properly.

7.2.1 Power-On Test

This test ensures that the radio turns on, the latest software version number briefly appears, a beep is heard, and an operational screen appears on the LCD.

7.2.2 Buttons and Switches Test

This test ensures that the PTT, auxiliary buttons, toggle switch, emergency key, keypad, on/off/volume switch, and channel switch work.

7.2.3 Transmit Test

This test ensures the radio has the required transmit power, frequency accuracy, and deviation.

7.2.4 Receive Test

This test ensures the radio LED works, a 1 kHz tone is heard, and that SINAD is within specified limits.

7.2.5 Audio Test

This test ensures that the radio's internal speaker and microphone are working. If the radio fails this test, please contact Datron for radio servicing.

CHAPTER 8: DEFINITIONS

Alert Mode: Display and audio properties are used when the emergency key is pressed. In normal mode, the display flashes EMERGENCY and an audio tone is heard. In silent mode, the display is blank and no audio tone is heard.

Analog-to-Digital Converter (ADC): An electronic device for converting data from analog to digital form for use in electronic equipment.

Backlight: The light behind the keypad and LCD enables the keys and LCD to be visible in dark conditions.

Backlight Delay: The time the backlight remains on after the last keypad activity.

Bandwidth (BW): A small range of frequencies around a transmit or receive frequency in which a message can be received or transmitted.

Bank: A group of zones. There are up to 4 banks per radio. Up to 16 zones can be distributed through these 4 banks.

Channel: A memory location with defined receive, transmit, squelch, modulation, and power settings. There are 256 channels per radio.

Channel Locked: An indicator informing that channel settings cannot be programmed using the LCD and keypad. The settings can only be changed using the PC programmer.

Channel Scan: Scans all channels on the scan list in a given 16-channel zone. The scan starts on the home channel, checks each channel in the scan plan, returns to the home channel, and then scans each channel in the scan plan.

Common Air Interface (CAI): The CAI standard allows interoperability within any Project 25 system provided they are all in the same frequency band.

Continuous Tone-Controlled Squelch System (CTCSS) Tone: A sub-audible tone superimposed on an analog signal to reduce interference from traffic and background noise.

Digital Coded Squelch (DCS): A digital variable superimposed on a digital signal to reduce interference from traffic and background noise.

Digital Signal Processor (DSP): Handles all signal-processing functions.

Digital to Analog Converter (DAC): A device that takes a digital value and outputs a voltage that is proportional to the input value.

Dual-Tone Multiple-Frequency (DTMF): A signaling scheme used by the telephone system in which two-voice band tones are generated for each keypad key press.

Global Search: Scans all frequencies programmed into the radio, regardless of scan list designation.

Initial Synchronization: The length of time required for the radio to perform encryption synchronization.

Microprocessor Unit (MPU): A computer's entire CPU is contained on one (or a small number of) integrated circuit.

Monitor Receive Squelch: The radio receives any intelligible analog transmission.

Monitor Timer: The amount of time the radio stays on a channel picked up during the scan and before the radio reverts back to scan mode.

Network Access Code (NAC): Selective squelch for digital mode. The primary purpose is to allow the user access to a repeater network. In radio-to-radio communications, these codes are used to eliminate interference from other traffic and background noise.

Normal Receive Squelch: The radio receives any transmission having the correct NAC.

Priority 1 Scan: Priority 1 channel is sampled during scanning, receive of an active channel, or standby. Activity on the priority1 channel overrides all other modes except emergency.

Priority 2 Scan: Priority-2 channel is sampled in a similar fashion to the priority-1 channel. Activity on the priority-2 channel overrides all other modes except emergency and priority 1.

Receive Only Channel: A feature that does not allow outgoing transmissions on the channel. It is used for channels in which transmission is prohibited (i.e., weather channels). If PTT is pressed on a receive-only channel, RX ONLY appears on the display.

Receiver/Exciter/Control Module (RECM): Transceiver module containing all radio functions except RF/audio amplifiers and display/keypad circuitry.

Repeater Delay: A delay timer used to prevent a radio from receiving its own transmission from a tactical repeater.

Scan Delay: The amount of time the scanner dwells on an active receive channel after the carrier is dropped. This prevents another message from being received before a response can be made.

Scan Reply: If a PTT press interrupts the scan delay timer, this is the amount of time allowed to ensure a reply to a received message.

Scan List: A group of channels in a zone that are designated as active scan list channels. Channels are added or deleted from the scan list using the PC programmer or the radio keypad.

Scan Revert Channel: The transmit channel that the radio reverts to when PTT is pressed during or following a scanned message.

Search Mode: The radio scans for and opens on carrier only regardless of CTCSS, DCS, or the digital ID.

Selective Receive Squelch: The radio receives any transmission having the correct NAC and TGID.

Shadow Channel: The radio of primary channels, each of which can have up to 7 shadow channels. A shadow channel has the same transmit and receive frequencies, options, and transmit power levels as its primary channel. Individual shadow channels can be configured for different channel types (analog or digital), BW (12.5 or 25 kHz for analog channels), squelch modes, P25 NACs (digital channel only), and encryption key (only one primary or shadow channel can have CVSD DES enabled). When properly configured, shadow channels can be created to allow a user to hear all transmissions on a receive/transmit frequency regardless of channel type, BW, squelch mode, or encryption. Shadow channels are created and their settings edited using the PC programmer.

Talk Group Identifier (TGID): Selective squelch for the digital mode, used to group users into functional teams.

Transmit Inhibit and Override: A feature that stops users from talking over other radio conversations. There are three options: CARRIER prevents transmission if any activity is detected on the channel, TONE prevents transmission on an active channel with a squelch code other than your own, and NAC prevents transmission on an active channel with the same NAC. There is a quick-key override feature available that allows a user to override the transmit inhibit state by quick-keying the radio (i.e., 2 PTT presses within a short time frame).

Transmit Timeout: Prevents inadvertent or prolonged transmit operations.

User Interface: The same as a man-machine interface.

Zone: A group of channels. There is a maximum of 16 zones per radio and each zone can contain up to 16 channels. Three zones can be selected using the toggle switch or 16 zones selected by the radio keypad.

Zone Scan List: A group of zones in a bank designated as active scan list zones. Zones are added or deleted from the scan list using the PC programmer or the radio's keypad.

CHAPTER 9: SIGNAL TONES

Tone	Signal	Cause
Brief low-pitched	Key press error	Invalid key pressed
	Failed power on self-test (POST)	Radio fails POST
	Transmit time-out warning	Time-out about to interrupt PTT
	Empty channel warning	No RX/TX frequencies programmed for the channel
Steady low-pitched	Transmit time-out timed out	Transmit time is exceeded and PTT still pressed
	Transmit inhibit	PTT switch is pressed and there is activity on the transmit channel
	Invalid mode	No programmed data on the selected channel
	Radio locked	Radio locks after 3 consecutive wrong password attempts
Brief medium-pitched	Key press	Valid key press is accepted by the radio
	Radio passed POST	Radio passed POST
	Clear voice received	Radio is receiving a clear signal
Repeated medium-pitched	Emergency call state	Emergency button is pressed
	Key error	Encryption is selected but no key is present
Brief high-pitched	Low dc supply voltage	DC supply voltage falls below a preset value
Repeated high-pitched	Individual call	An individual call is received

CHAPTER 10: CONNECTOR PINOUTS

10.1 Accessory Connector Pins and Functions

Pin	Signal Name	Description
1	RS232_RXD	Receive data line output (DCE), RS232 level (>+3V=ZERO, <-3V=ONE)
2	RS232_RTS	Data port control input (DCE), RS232 level (>+3V=ON, <-3V=OFF)
3	SERIAL_CLOCK	Synchronous clock output to PC terminal (DCE), RS232 level (>+3V=ZERO, <-3V=ONE)
4	RS232_CTS	Data port control output (DCE), RS232 level (>+3V=ON, <-3V=OFF)
5	PC_232RXD	Programming receive data line output (DCE), RS232 level (>+3V=ZERO, <-3V=ONE)
6	SQUELCH_INF	Squelch, low on valid receive signal, 7.8V squelched
7	GND	Ground
8	EXTERNAL_SPEAKER_N	Balanced audio output from RECM, 500 mW into 8 ohms
9	EXTERNAL_PTT/KID	PTT input asserted by voltage closure to ground or pseudo-random key insert data, LVTTL level input
10	7.7V	Test point for internal regulated voltage supply
11	EXTERNAL_MIC/WE	Microphone input or key transfer indicator input, asserted by voltage 0.8 Vdc
12	GND	Ground
13	INTERNAL_SPEAKER_P	Balanced audio input from external device; can override RECM audio output signal
14	PTT_SWITCH	PTT input asserted by voltage closure to ground
15	RS232_DTR	Data port control input (DCE), RS232 level (>+3V=ON, <-3V=OFF)
16	PC_232TXD	Programming transmit data line input (DCE), RS232 level (>+3V=ZERO, <-3V=ONE)
17	RS232_TXD	Transmit data line input (DCE), RS232 level (>+3V=ZERO, <-3V=ONE)
18	WRU_MONITOR	Voltage input identifies external device
19	EXT_10W_SPEAKER_N	Balanced audio output for external 10W 4-ohm speaker
20	EXT_10W_SPEAKER_P	Balanced audio output for external 10W 4-ohm speaker
21	EXTERNAL_MIC_BIAS/KEY	Microphone bias or bi-directional key data, LVTTL levels
22	EXTERNAL_SPEAKER_P/KLD	Balanced audio output from RECM, 500 mW into 8 ohms or LVTTL low-output level when keyloader is connected
23	EMERGENCY_SWITCH	Active low control to transmit emergency signal
24	IGN_SW	Power switch override input. Ground forces off, open enables switch
25	INTERNAL_SPEAKER_N	Balanced audio input from external device; can override RECM audio output signal

10.2 Power Connector Pins and Functions

Pin	Signal Name	Description
1	BATTERY	Battery power
2	GROUND	Ground
3	IGN_SW	Ignition switch
4	EXTERNAL_10W_SPEAKER_N	External speaker
5	EXTERNAL+10W_SPEAKER_P	External speaker
6	BATTERY	Battery power
7	GROUND	Ground
8	GROUND	Ground
9	EMERGENCY_SWITCH	Emergency switch

10.3 Microphone Jack Connector Pins and Functions

Pin	Signal Name	Description
1	EXTERNAL_MIC_BIAS/KEY	Keyload line
2	GROUND	Ground
3	INTERNAL_MIC	Microphone audio
4	EXTERNAL_MIC/WE	Keyload line
5	PTT_SWITCH	Push-to-talk line
6	BIAS(+)	Microphone power
7	EXTERNAL_SPEAKER_P/KLD	Keyload line
8	EXTERNAL_PTT/K1D	Keyload line

CHAPTER 11: SCHEMATICS

REV	ECN	DESCRIPTION	DATE	APPR
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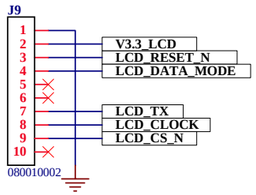

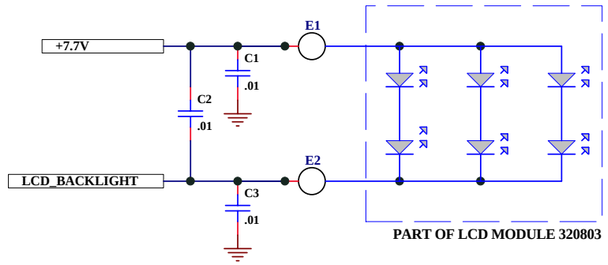

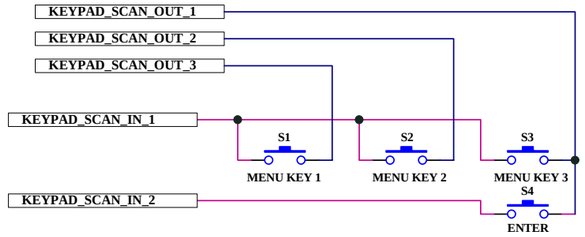

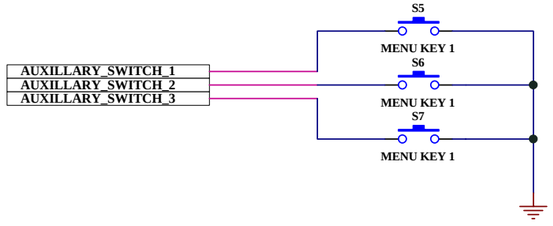

DATRON WORLD COMMUNICATIONS INC.
3030 Enterprise Ct.
Vista, CA 92083
(760)597-3777

Title: *Schematic*

SCHEMATIC, KEYPAD/DISPLAY

Size:	Drawn: ABE SABET	Date: 04-12-01	Drawing Number:	Rev:
B	Appr:	Date:	994466	A

File: 994466A.Sch | Date: 14-May-2002 Time: 11:06:32 | Sheet 1 of 1

REV	ECN	DESCRIPTION	DATE	APPR

EXTERNAL AUDIO AMPLIFIER

INTERNAL AUDIO AMPLIFIER

J1 — 613507
RS232_RXD
PC_232RXD
RS232_RTS
SERIAL_CLOCK
RS232_CTS
RS232_DTR
IGN_SW
EMERGENCY_SWITCH
PC_232TXD
RS232_TXD
WRL_MONITOR
EXTERNAL_MIC_BIAS/KEY
EXTERNAL_SPEAKER_P/KID
EXTERNAL_PTT/KID
EXTERNAL_SPEAKER_N
VBAT_TP
3.3V

J2 — 613507
PTT_SWITCH
SQUELCH_INDICATOR
INTERNAL_SPEAKER_N
INTERNAL_SPEAKER_P
AUDIO_EXT_DISABLE
AUDIO_INTERNAL_DISABLE
INT_5W_SPEAKER_P
INT_5W_SPEAKER_N
LED_TX
PA_PTT
TP21
BIAS
7.8V
ON/OFF

R1 200k 7.8Vsw
U6A LM2903 (1,2,3)
U6B LM2903 (5,6,7)
R20 100k

AUDIO_EXT_DISABLE
INTERNAL_SPEAKER_P
INTERNAL_SPEAKER_N
SWBAT
R10 10K, R11 10k, R12 10k, C14 0.1uF, C19 47uF,20V, C20 47uF,20V
C7 1nF
R7 10k, R9 10k, C2 1uF/25V, C3 1uF/25V, R6 10k, R8 10k, R21 10k, C1 1uF/25V
U1 TDA1516BQ (-IN1, +IN1, MODE, Vp, BS1, OUT1, RR, +IN2, OUT2, Vref, GND1, GND2, BS2)
R2 0ohm → EXTERNAL_10W_SPEAKER_P
R3 0ohm → EXTERNAL_10W_SPEAKER_N

AUDIO_INTERNAL_DISABLE
SWBAT
R17 10K, C8 1nF, R19 10k, R18 10k, C15 0.1uF, C21 47uF,20V, C22 47uF,20V
R14 10k, R16 10k, C4 1uF/25V, R13 10k, R15 10k, R33 10k, C6 1uF/25V, C5 1uF/25V
U2 TDA1516BQ (-IN1, +IN1, MODE, Vp, BS1, OUT1, RR, +IN2, OUT2, Vref, GND1, GND2, BS2)
R4 0ohm → INT_5W_SPEAKER_P
R5 0ohm → INT_5W_SPEAKER_N

R40 10k, R29 100, Q1 2N7002

R31 0OHM
R66 DNP, R28 10k, C38 DNP, R22 10k, R67 0OHM, R41 51.1K-1%, U3A LM2904 (1,2,3), R42 0OHM
R48 10k, Q8 10K/10K
R46 100k, FB1, C9 1nF, FB2, L1 2.7uH
E1 PAD, J3 PANEL MNT, E2 PAD
C12 1nF, J4 OSMT
R45 0OHM → LED_TX
Q9 MMBT2222, R44 100k
R63 100k, R64 100k, Q15 2N7002
Q13 2N7002, Q14 2N7002, Q16 MMBT2222, R65 100k, PTT_SWITCH
C24 1uF/25V
R23 1k, R24 1k, R25 6.2K, R37 0ohm, R26 10k, R27 300, R43 0ohm
Q5 2N7002, R57 0OHM, PA_PTT
R32 10k
R30 10k, R38 2.67K-1%, R39 1.27k-1%, C54 1nF → TP21
U4A LM2903 (1,2,3)
U4B LM2903 (5,6,7)
R53 10k, R54 1.82K-1%, R55 560
U3B LM2904 (6,5,7)
R60 10k, C58 1nF
R52 10k, R56 1.05K,1%

3.3V, VBAT, SWBAT, 7.8V

J6 — 610458
C26 C27 C28 C29 C30 C31 C32 C35 C36 C38 C39 C40 100pF
C41 C42 C41 C44 C45 C46 C47 C48 C49 C50 C51 100pF
FB4 RS232_RXD
D3 4148, FB24 PTT_SWITCH
FB5 RS232_RTS
FB6 RS232_DTR
FB7 SERIAL_CLOCK
FB8 PC_232TXD
FB9 RS232_CTS
FB10 RS232_TXD
FB11 WRL_MONITOR
FB12 SQ_INF
FB13
FB14 EXTERNAL_SPEAKER_N
FB15 EXTERNAL_MIC_BIAS/KEY
FB16 EXTERNAL_PTT/KID
FB17 EXTERNAL_SPEAKER_P/KID
FB18
FB19 EMERGENCY_SWITCH
FB20 EXTERNAL_MIC_WE
FB21 IGN_SW
FB22 INTERNAL_SPEAKER_N
FB23 INTERNAL_SPEAKER_P
C52 100pF → EXTERNAL_10W_SPEAKER_N / EXTERNAL_10W_SPEAKER_P
7.8Vsw

J5 — 610457
PF1 550044, C25 .01uF
L2 10uH
FB25 IGN_SW
FB3 EMERGENCY_SWITCH
C34 100pF
EXTERNAL_10W_SPEAKER_N
EXTERNAL_10W_SPEAKER_P
C33 100pF, C37 100pF
D1 IN6278, D4 IN6278
Q10 IRF7328
R35 10k, R36 10k
ON/OFF → R34 10k → Q7 2N7002
BIAS → R68 270 → SWBAT
C13 1nF

VBAT → R69 10k → VBAT_TP
C53 10uF, C55 1nF/25V, C16 0.1uF
U5 LM350T (+Vin, Vout, ADJ)
C11 10uF, C57 DNP
Q3 MMBT2907, Q2 MMBT2222
R47 100k, R50 2.67K, R51 12.7K, R49 1.05K,1%
C82 1uF/25V, C56 1uF/25V
R62 10K → Q12 IRLML6302 → 7.8V / 7.8Vsw
ON/OFF → Q11 2N7002

SWBAT
C17 0.1uF, U3C LM2904 (VCC, GND)
C18 0.1uF, U4C LM2903 (8, 4)
C23 0.1uF, U6C LM2903 (8, 4)

FD3 FD2 FD1

PCB:738534
BOM:125-50220

3030 Enterprise Ct.
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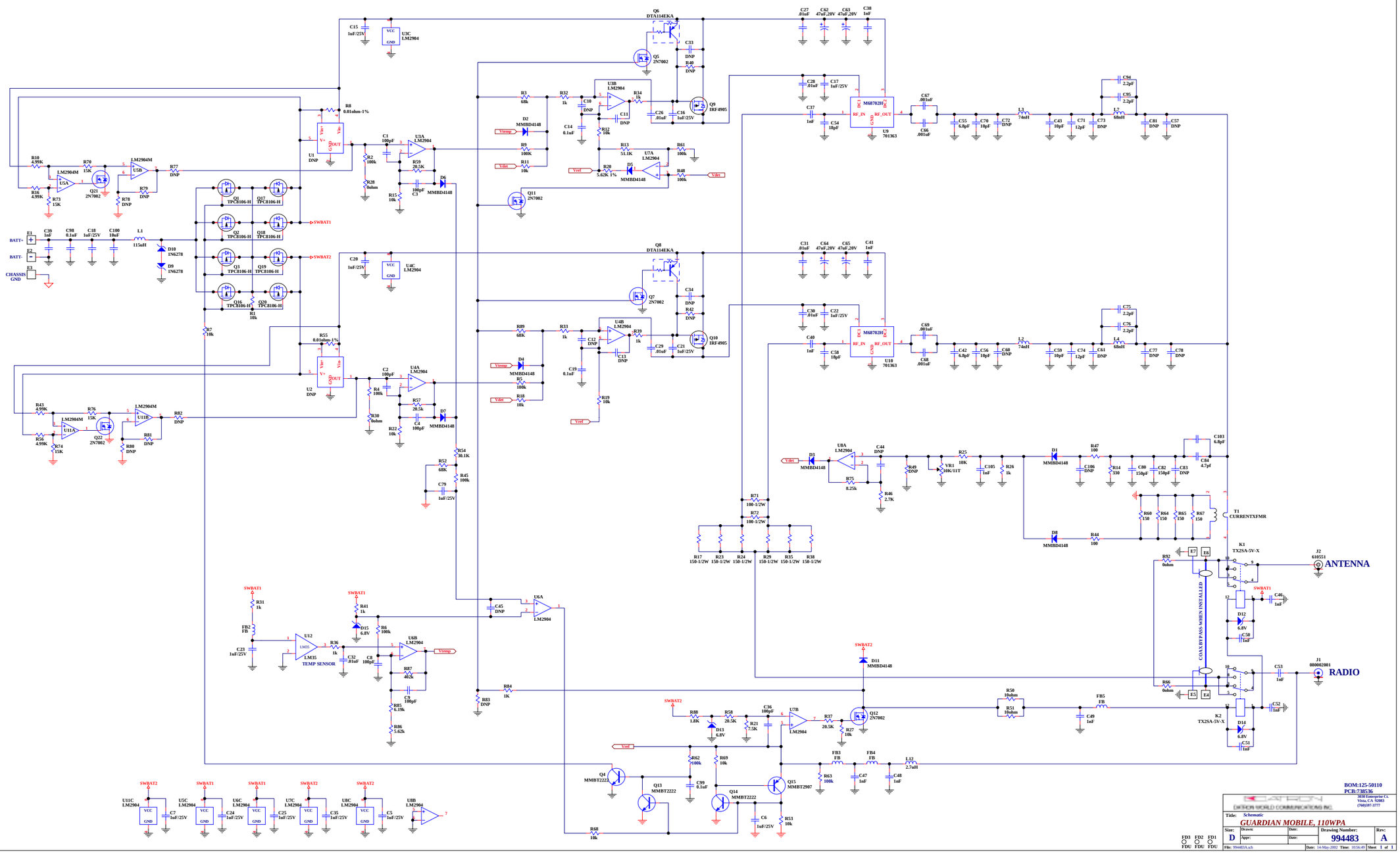
(760)597-3777

Title: Schematic
AUDIO AMP BD, GUARDIAN 100W MOBILE

Size:	Drawn:	Date:	Drawing Number:	Rev:
D	Appr:	Date:	994478	A

File: 994478A.Sch — Date: 14-May-2002 Time: 10:55:16 — Sheet 1 of 1

REV	ECN	DESCRIPTION	DATE	APPR



REV	ECN	DESCRIPTION	DATE	APPR

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RS232_RXD
PC_232RXD
RS232_RTS
SERIAL_CLOCK
RS232_CTS
RS232_DTR
EMERGENCY_SWITCH
PC_232TXD
RS232_TXD
WBU_MONITOR
EXTERNAL_MIC_BIASKEY
EXTERNAL_SPEAKER_PKLD
EXTERNAL_MIC/WE
EXTERNAL_PTT/KID
EXTERNAL_SPEAKER_N
VBAT
3.3V

J3 — 613507
PTT_SWITCH
SQUELCH_INDICATOR
INTERNAL_SPEAKER_N
INTERNAL_SPEAKER_P
AUDIO_EXT_DISABLE
AUDIO_INTERNAL_DISABLE
INT_SW_SPEAKER_P
INT_SW_SPEAKER_N
LED_TX
PA_PTT
TPDT
BIAS
ON/OFF
7.8V

R61 10k

J1 — 610354
ON/OFF
KEYPAD_BACKLIGHT_N
KEYPAD_SCAN_OUT_1
KEYPAD_SCAN_OUT_2
KEYPAD_SCAN_OUT_3
KEYPAD_SCAN_IN_1
KEYPAD_SCAN_IN_2
KEYPAD_SCAN_IN_3
KEYPAD_SCAN_IN_4
KEYPAD_SCAN_IN_5
KEYPAD_SCAN_IN_6
LCD_BACKLIGHT_N
LCD_CLOCK
LCD_TX
LCD_CS_N
LCD_RESET_N
LCD_DATA_MODE
INTERNAL_SPEAKER_P
INTERNAL_SPEAKER_N
INTERNAL_MIC
INTERNAL_PTT
AUXILIARY_SWITCH_1
AUXILIARY_SWITCH_2
AUXILIARY_SWITCH_3
VOLUME_SWITCH_1
VOLUME_SWITCH_2
VOLUME_SWITCH_3
VOLUME_SWITCH_4
TOGGLE_SWITCH_1
TOGGLE_SWITCH_2
CHANNEL_SWITCH_1
CHANNEL_SWITCH_2
CHANNEL_SWITCH_3
CHANNEL_SWITCH_4
EMERGENCY_SWITCH
3V3_LOGIC
LED_RED_N_SYS
LED_GREEN_N
EXTERNAL_MIC_BIASKEY
EXTERNAL_MIC/WE
WBU_MONITOR
EXTERNAL_PTT/KID
EXTERNAL_SPEAKER_PKLD
EXTERNAL_SPEAKER_N
SQUELCH_INDICATOR
RADIO_OFF_SC_N
SERIAL_CLOCK
RS232_RXD
RS232_TXD
RS232_DTR
RS232_CTS
RS232_RTS
PC_232RXD
PC_232TXD
7.8Vsw

C1–C13 DNP; C14–C19 100p
R9 10K
R1 1k, R2 1k
INTERNAL_PTT
E1 PAD, E2 PAD, E5 PAD, E6 PAD, E7 PAD
FB8 FB; D2 4148
R24 DNP, R25 0ohm
R21 10k

J4 — 621112
3.3V_LCD
LCD_RESET_N
LCD_DATA_MODE
LCD_TX
LCD_CLOCK
LCD_CS_N
AUXILIARY_SWITCH_1
AUXILIARY_SWITCH_2
AUXILIARY_SWITCH_3
7.8Vsw
KEYPAD_SCAN_OUT_1
KEYPAD_SCAN_OUT_2
KEYPAD_SCAN_OUT_3
KEYPAD_SCAN_IN_1
KEYPAD_SCAN_IN_2

R49 0ohm, R7 0ohm, R6 DNP
L10 DNP, L1 FB, L2 FB, L3 FB, L4 FB, L5 FB, L6 FB, L7 FB, L8 FB, L11 DNP
PC_232RXD
EXTERNAL_MIC_BIASKEY
INTERNAL_MIC
EXTERNAL_MIC/WE
PTT_SWITCH
BIAS(+)
EXTERNAL_SPEAKER_PKLD
EXTERNAL_PTT/KID
PC_232TXD
R43 560, D4 12V, BIAS

J5 — 610669
C46–C52 100p

ON/OFF → R3 1k → 7.8V
VOLUME_SWITCH_1 → Q11 DTA144EKA
VOLUME_SWITCH_2 → Q12 DTA144EKA
VOLUME_SWITCH_3 → Q13 DTA144EKA
VOLUME_SWITCH_4 → Q14 DTA144EKA
.10K
R20 10k

KEYPAD_SCAN_IN_1 (ESCAPE) → Q1 DTA144EK .47K
KEYPAD_SCAN_IN_2 (ENTER) → Q3 DTA144EK .47K
PTT_SWITCH → Q2 DTA144EK .47K
R8 1M, C20 1uF/16V, Q15 2N7002
R16 10k, R19 10k, R17 10k, R18 10k, Q8 2N7002, Q6 2N7002
E3 PAD
R12 100k, Q7 2N7002, Q5 2N7002, Q16 2N7002
FB7 FB; E4 PAD; INTERNAL_PTT; PA_PTT
Q10 DTA144EK .47K, C31 1uF/16V, R22 1M

INT_SW_SPEAKER_P, INT_SW_SPEAKER_N
C38 DNP, R30 DNP, R31 DNP, R32 DNP, J6 610217 — SPEAKER
Q19 DTA144EK .47K, Q18 2N7002, R10 100K, R11 100K
D3 RED/IGRN 035500004
R33 100
LED_GREEN_N, LED_TX, LED_RED_N_SYS
R58 0OHM, R59 DNP, R60 0OHM

E9 PAD → FB13 FB → AUDIO
R45 DNP, C54 .01uF, C53 .01uF, R13 100k, R14 100k, R48 220K, R49 220K
C26 0.1uF, C28 0.1uF, C29 0.1uF
U6 CM8817O
ESI
R46 270k, D6 DNP, D7 DNP, R47 DNP, C27 0.1uF, R50 DNP
Y1 3.579545 MHZ, C39 DNP

E8 PAD → ESI
R51 47.5k, Q4 DTA144EK .47K, C32 1uF/16V, C33 1uF/16V
R29 0ohm, R15 100k
U2 74HC4514

Q21 IRLML6302, Q20 2N7002, R62 10K, ON/OFF
R36 100, R38 100, R35 100, R37 100
U1 LM317 (IN, NC, OUT2/OUT3, OUT1/OUT4, ADJ, NC)
C21 0.1uF, C22 0.1uF, C40 47uF/20V
R52 240, R53 270, R54 150
FB9 FB → 3.3V_LCD; FB10 FB → 3.3DTMF; FB11 FB → 3.3V

U3 74HC4016, U4 74HC4016, U5 74HC4016
C25 0.1uF, C24 0.1uF, C30 0.1uF
KEYPAD_SCAN_IN_1, KEYPAD_SCAN_IN_4, KEYPAD_SCAN_OUT_1, KEYPAD_SCAN_OUT_2, KEYPAD_SCAN_OUT_3, KEYPAD_SCAN_IN_5, KEYPAD_SCAN_IN_6
C42 DNP, C43 DNP, C41 DNP, C44 DNP
R28 0ohm, R27 0ohm, R26 0ohm

VOLUME_SWITCH_1, VOLUME_SWITCH_2, VOLUME_SWITCH_3, VOLUME_SWITCH_4 → SW3 510038 VOLUME; FB12 FB
IGN_SW → R44 100k, R23 1M, R55 1M, Q17 2N7002

CHANNEL_SWITCH_1, CHANNEL_SWITCH_2, CHANNEL_SWITCH_3, CHANNEL_SWITCH_4 → SW4 510038 CHANNEL; R35 100

TOGGLE_SWITCH_2, TOGGLE_SWITCH_1 → SW1 TOGGLE; R4 1K
AUDIO_EXT_DISABLE, AUDIO_INTERNAL_DISABLE → SW2 TOGGLE; R5 1K

7.8Vsw → R57 330, R56 330, R34 330, D5 RED → AUDIO_EXT_DISABLE → Q9 2N7002

BOM: 125-50210
PCB: 738535

3030 Enterprise Ct.
Vista, CA 92083
(760)597-3777

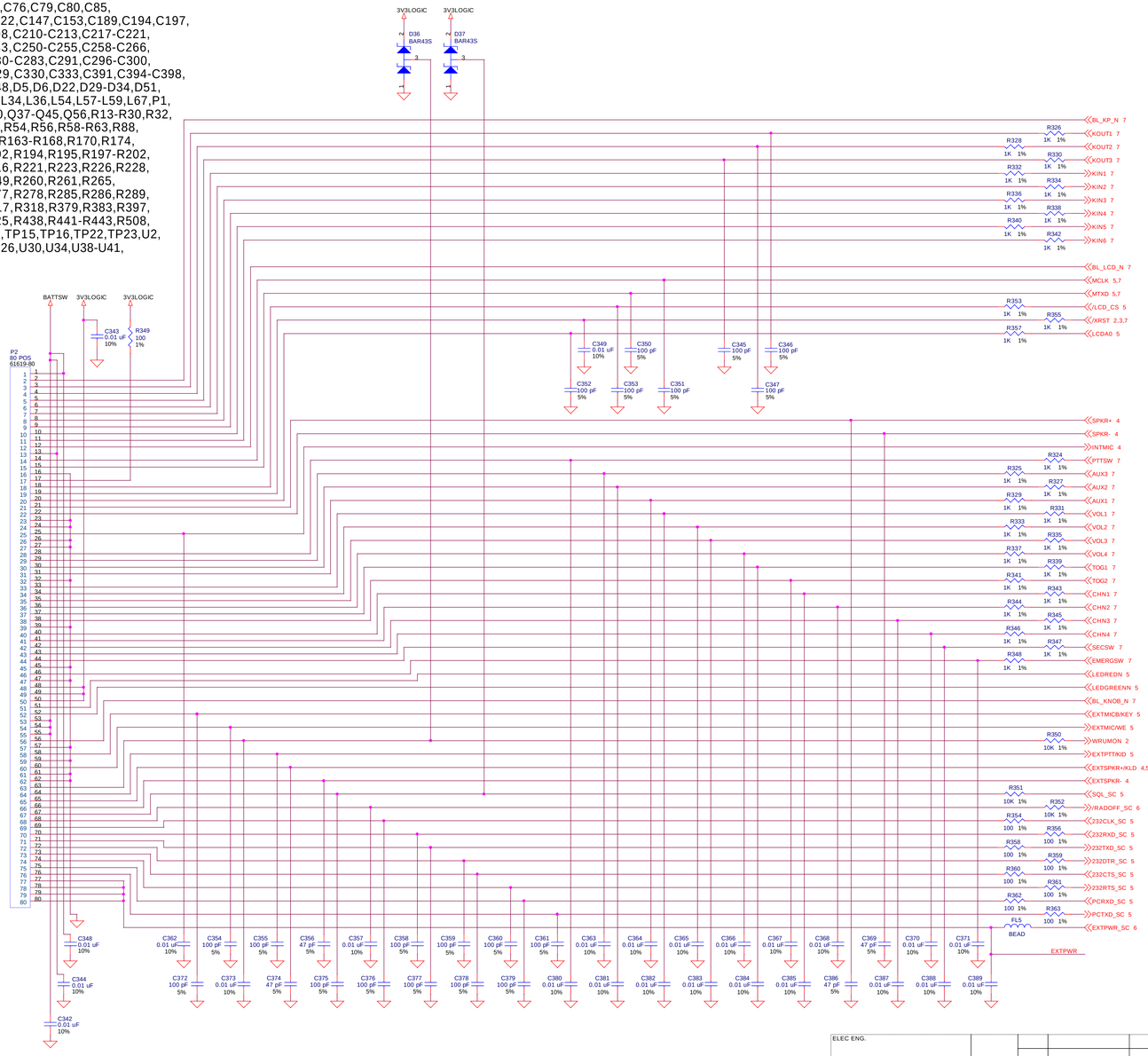
Title: Schematic
GUARDIAN 100W MOBILE, CONTROL BD
Size: D | Drawn: | Date: | Drawing Number: 994484 | Rev: A
Appr: | Date:
File: 994484A.sch | Date: 14-May-2002 | Time: 10:57:49 | Sheet 1 of 1

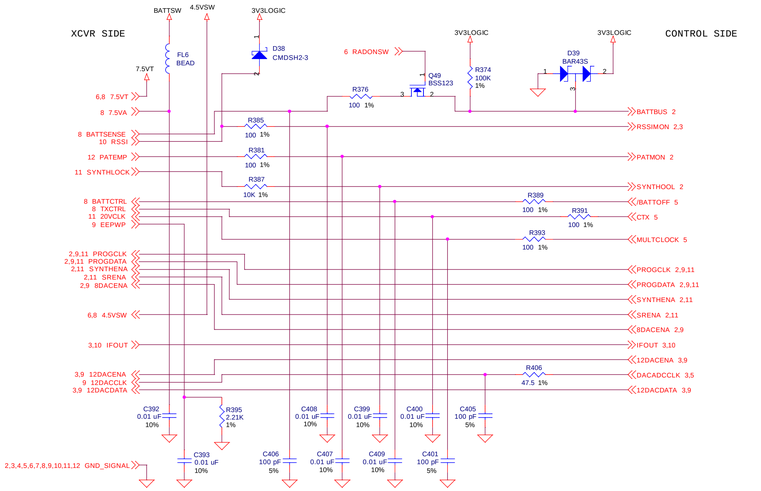
FD3 FD2 FD1

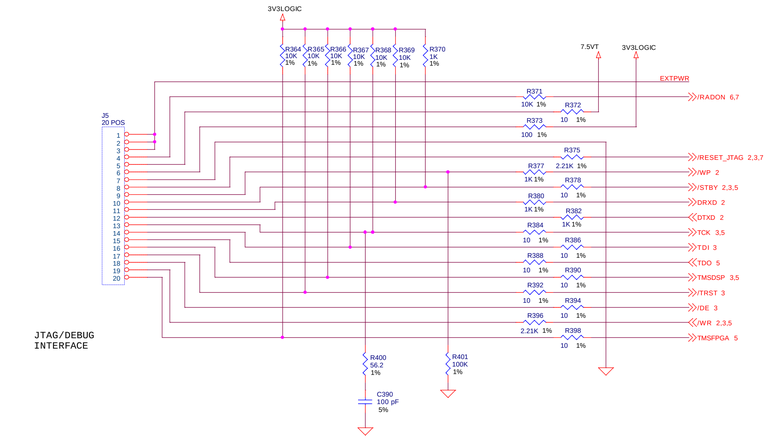
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	01	PREPRODUCTION RELEASE	-	-
	02	BOARD SPIN 2 UPDATED	10/10/01	BMAAT

NOTES: UNLESS OTHERWISE SPECIFIED.

1. INTERPRET DRAWING PER MIL-STD-100.
2. ALL RESISTANCE VALUES ARE IN OHMS,
3. CAPACITANCE VALUES ARE IN MICROFARADS,
4. LAST REF DES USED:
   B1,C550,D69,FL6,J5,L80,P2,Q71,R580,RT1,
   T2,TP24,U77,Y1
5. REF DES NOT USED:
   C20,C24,C32,C33,C35-C37,C39-C42,C44-C52,
   C54,C55,C58,C60,C62-C73,C76,C79,C80,C85,
   C89-C91,C93,C99,C119,C122,C147,C153,C189,C194,C197,
   C198,C204,C205,C207,C208,C210-C213,C217-C221,
   C232,C234,C238,C239,C243,C250-C255,C258-C266,
   C272-C274,C277,C278,C280-C283,C291,C296-C300,
   C313-C317,C320-C327,C329,C330,C333,C391,C394-C398,
   C402-C404,C530,C533,C548,D5,D6,D22,D29-D34,D51,
   J1,J4,L23,L26,L27,L29,L32-L34,L36,L54,L57-L59,L67,P1,
   Q3-Q6,Q8,Q9,Q20,Q28-Q30,Q37-Q45,Q56,R13-R30,R32,
   R34-R43,R45,R46,R50,R53,R54,R56,R58-R63,R88,
   R90,R93,R108,R158,R161,R163-R168,R170,R174,
   R176,R184,R188-R190,R192,R194,R195,R197-R202,
   R205,R207,R209-R211,R216,R221,R223,R226,R228,
   R231-R235,R239,R242-R249,R260,R261,R265,
   R267-R271,R274,R275,R277,R278,R285,R286,R289,
   R301-R305,R307-R314,R317,R318,R379,R383,R397,
   R399,R402-R405,R407,R425,R438,R441-R443,R508,
   R509,R519,R520,R532,TP4,TP15,TP16,TP22,TP23,U2,
   U5-U10,U18,U22,U23,U25,U26,U30,U34,U38-U41,
   U61,U66,U67,U72







JTAG/DEBUG INTERFACE

						-	REVISION	REV STATUS OF SHEETS
6	5	4	3	2	1		SHEETS	

SOFTWARE VERSION: Orcad Capture 7.00
FILENAME: 07160101.DSN

ELEC ENG.			
MECH ENG.			
QA			
MFG/TEST ENG			
TECH DIR			
DSGNR			
ADDITIONAL APPROVALS	DATE		

	4101421	DATRON
PART DASH NO.	NEXT ASSY	USED ON
	APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS +/- DECIMALS .XX +/- .XXX +/- ANGLES +/-
DO NOT SCALE DRAWING
TREATMENT
FINISH
SIMILAR TO

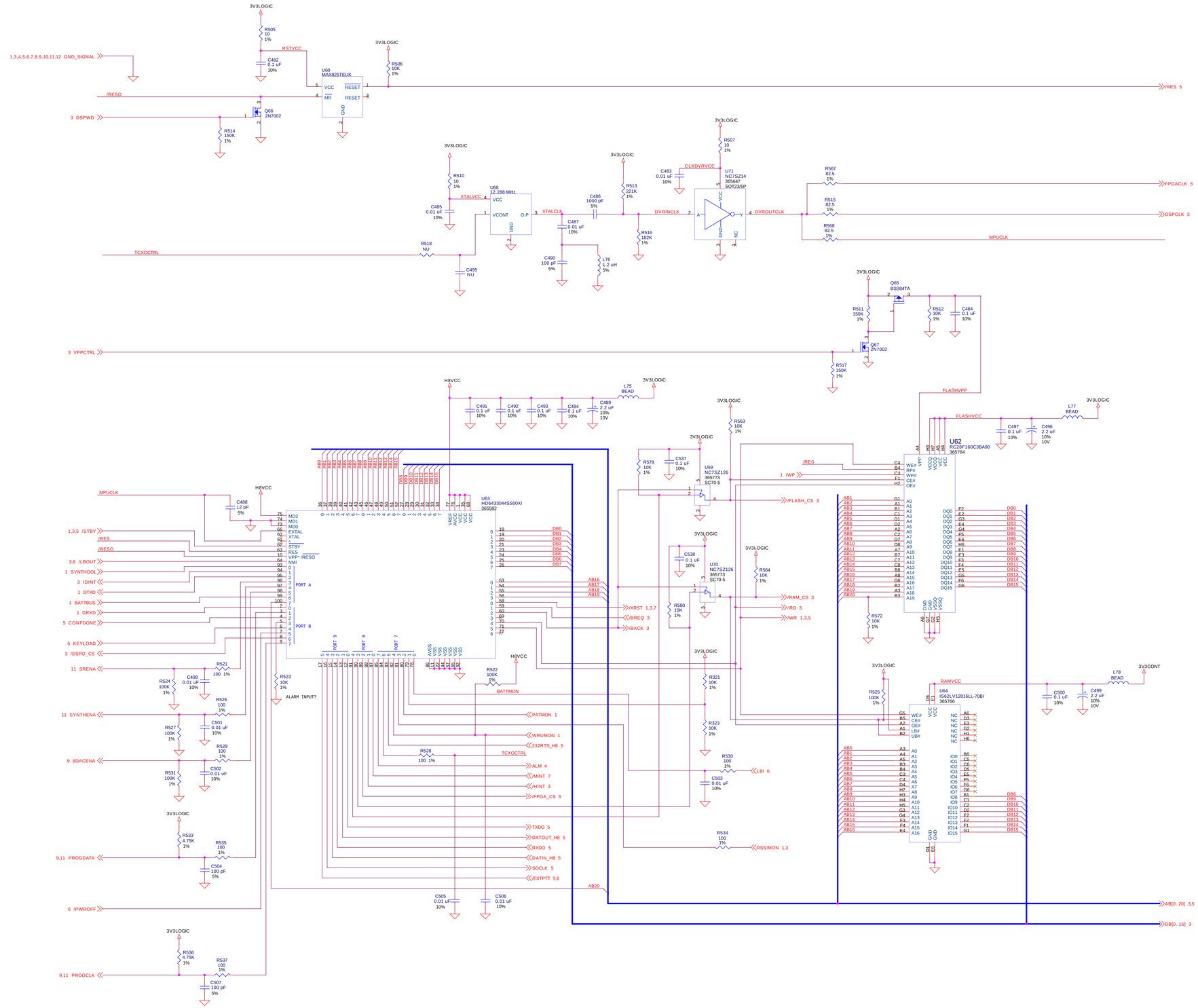
CONTRACT NO.

APPROVALS	DATE
DRAWN E. HOOKER	07/20/00
CHECKED	

THALES COMMUNICATIONS, INC.
ROCKVILLE, MARYLAND

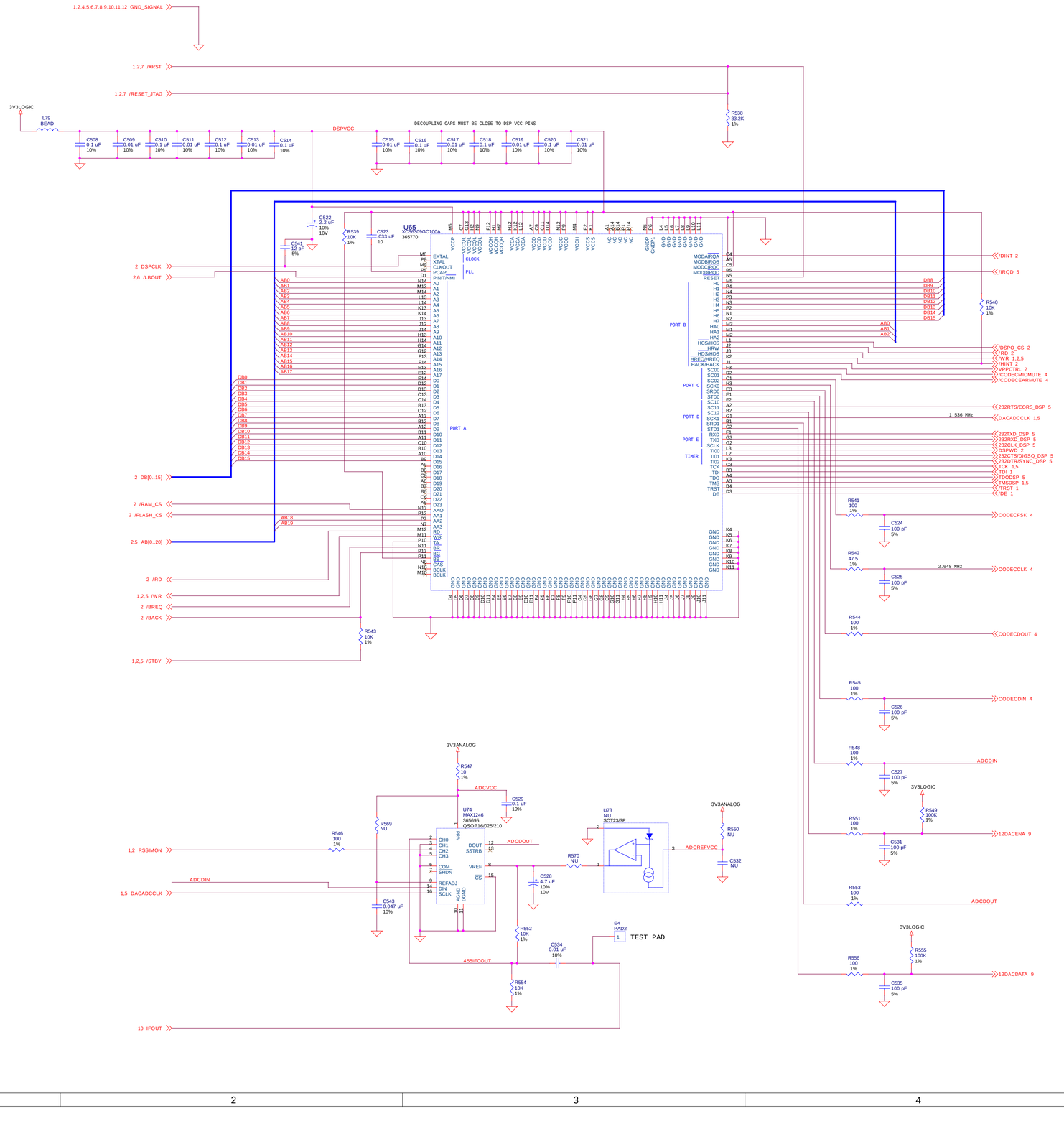
TITLE: SCHEMATIC DIAGRAM, CCA CONTROL/TRANSCEIVER

SIZE	CAGE CODE	DWG NO	REV
D	23386	4200716	02
SCALE: NONE	Thursday, November 15, 2001	SHEET 1 OF 12	



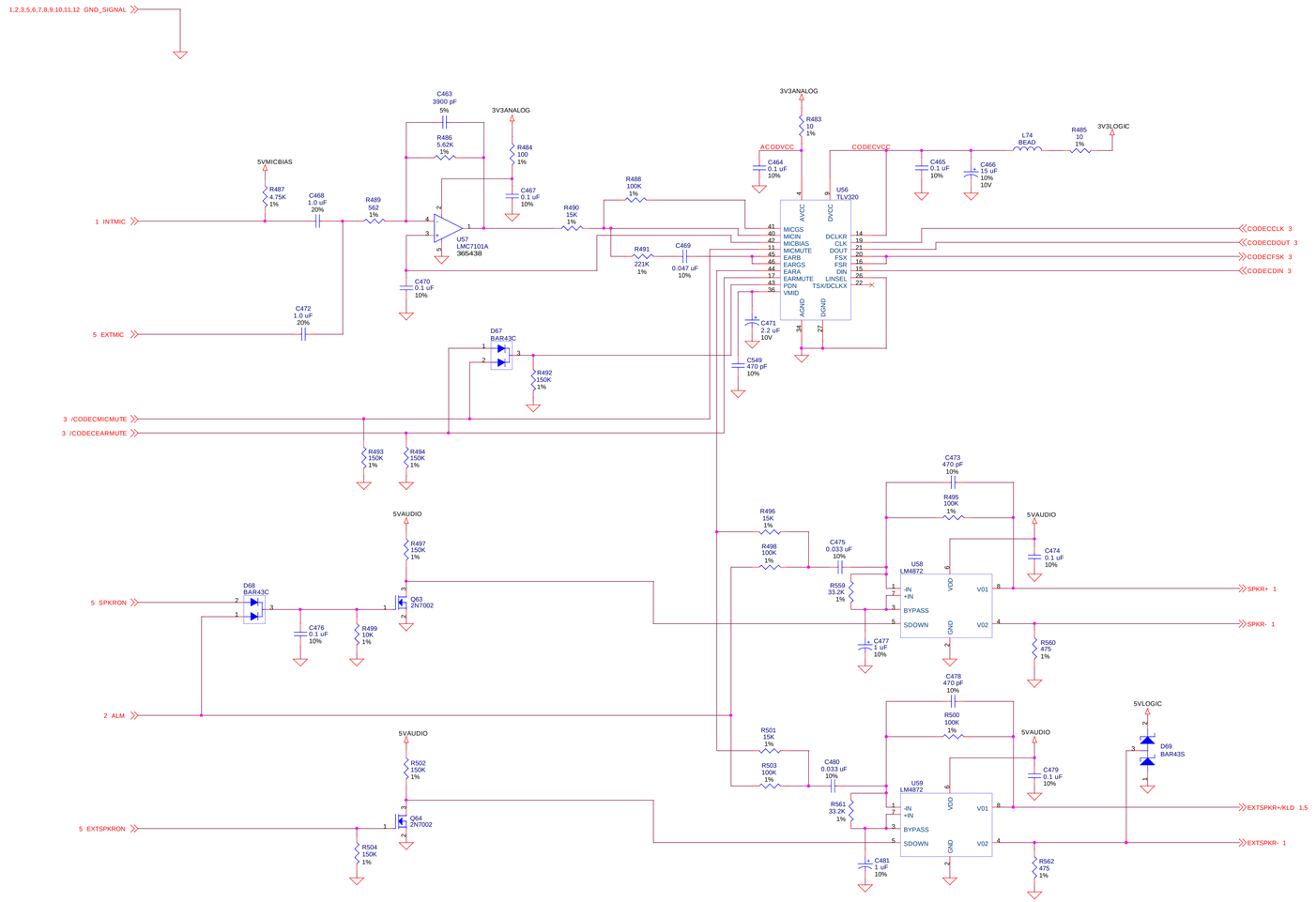
Control MPU

Thales Communications, Inc. Rockville, Maryland		Size	CAGE Code	Dwg No.	Rev
Drawn E. HOOKER		D	23386	4200716	02
		Scale None	Thursday, November 15, 2001	Sheet 2 of 12	



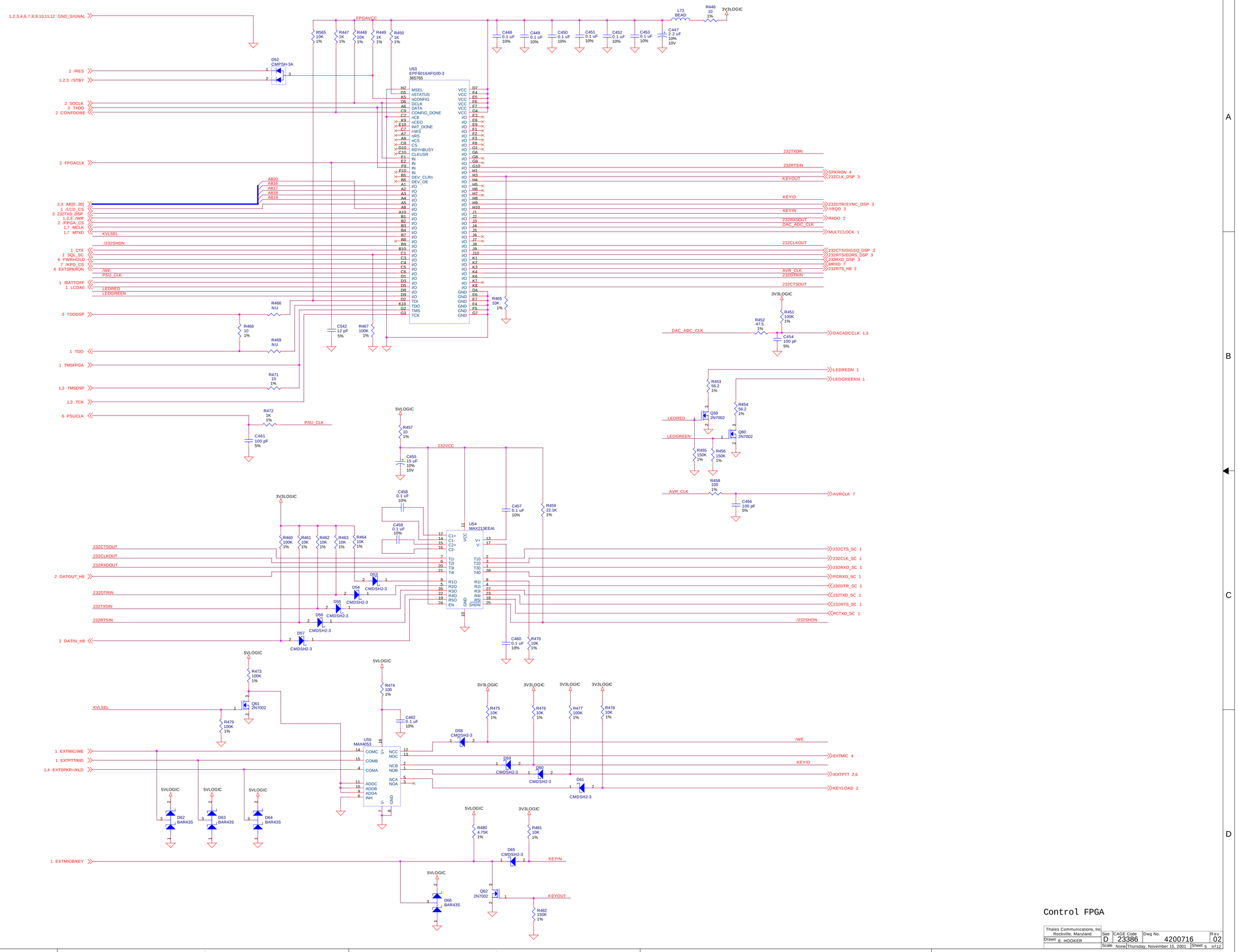
Control DSP

Thales Communications, Inc. Rockville, Maryland	Size	CAGE Code	Dwg No.	Rev
Drawn E. HOOKER	D	23386	4200716	02
	Scale None	Thursday, November 15, 2001	Sheet 3 of 12	



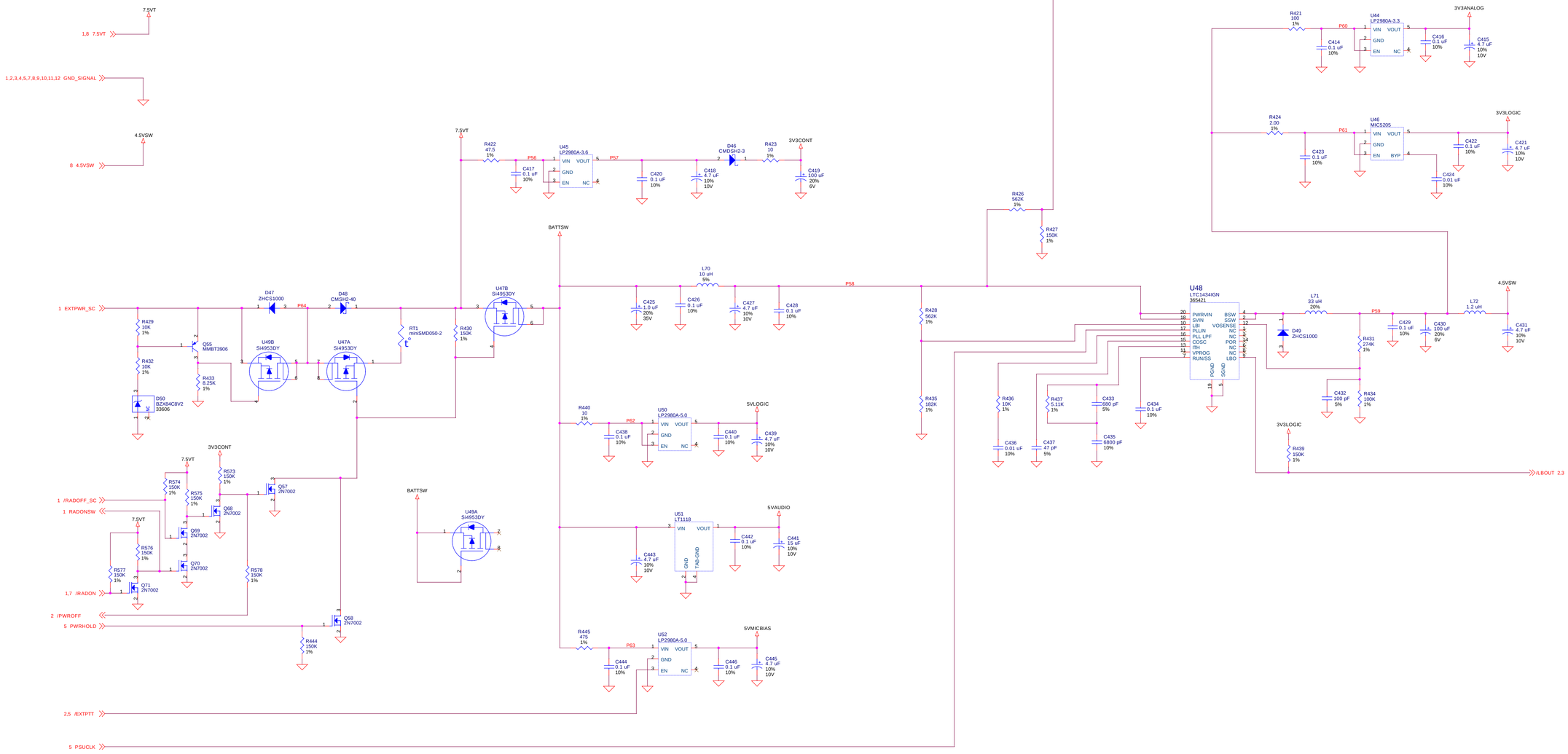
Control Audio

Thales Communications, Inc. Rockville, Maryland		Size	CAGE Code	Dwg No.	Rev
Drawn E. HOOKER		D	23386	4200716	02
		Scale None	Thursday, November 15, 2001	Sheet 4 of 12	



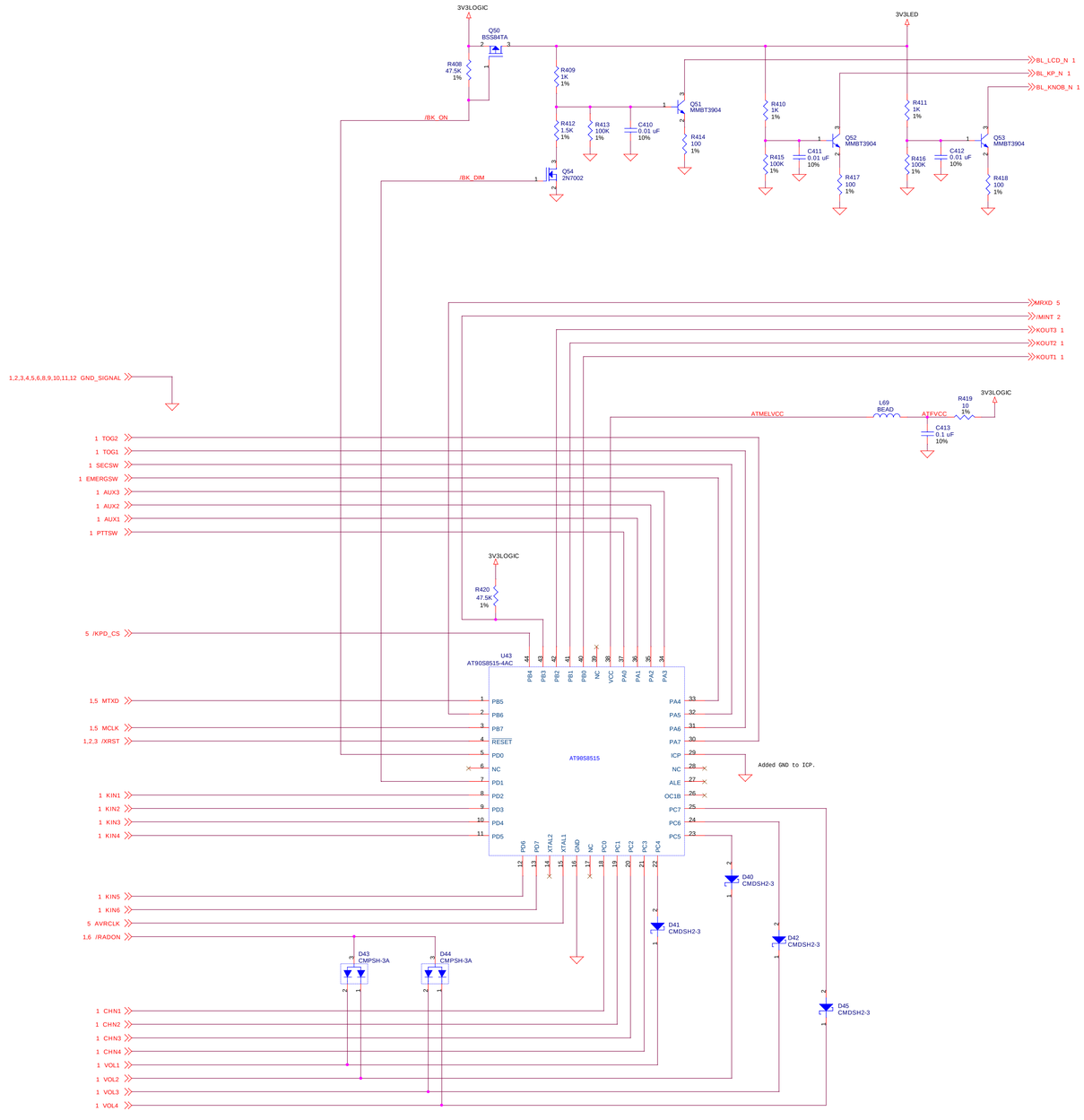
Control FPGA

Thales Communications, Inc. Rockville, Maryland		Size	CAGE Code	Dwg No.	Rev
Drawn E. HOOKER		D	23386	4200716	02
		Scale None	Thursday, November 15, 2001	Sheet 5 of 12	



Control Power

Thales Communications, Inc. Rockville, Maryland		Size	CAGE Code	Dwg No.	Rev
Drawn E. HOOKER		D	23386	4200716	02
		Scale None	Thursday, November 15, 2001	Sheet 6 of 12	

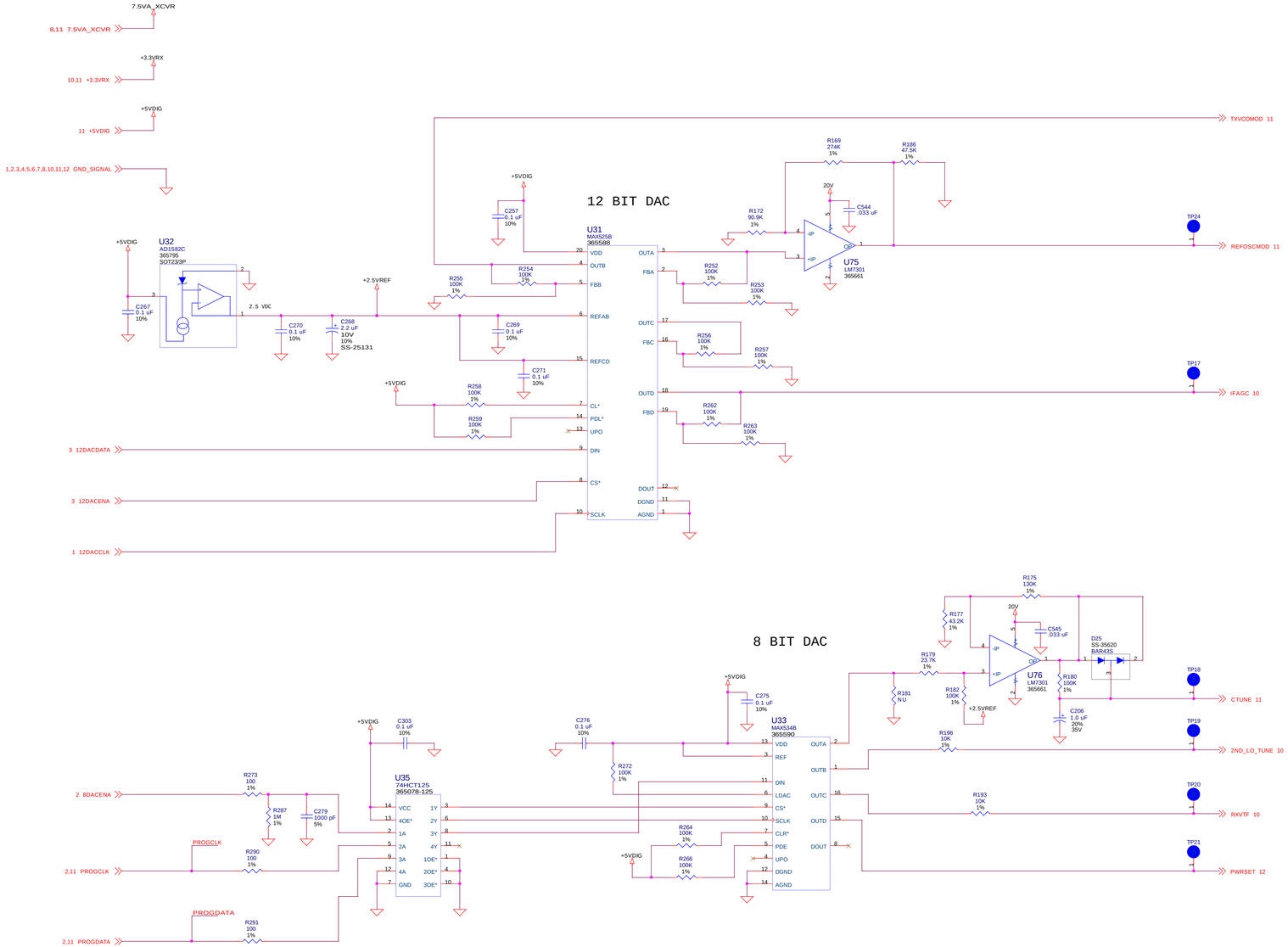


Control Keypad

Thales Communications, Inc. Rockville, Maryland		Size	CAGE Code	Dwg No.	Rev
Drawn E. HOOKER		D	23386	4200716	02
		Scale None	Thursday, November 15, 2001	Sheet 7 of 12	

Transceiver Interface

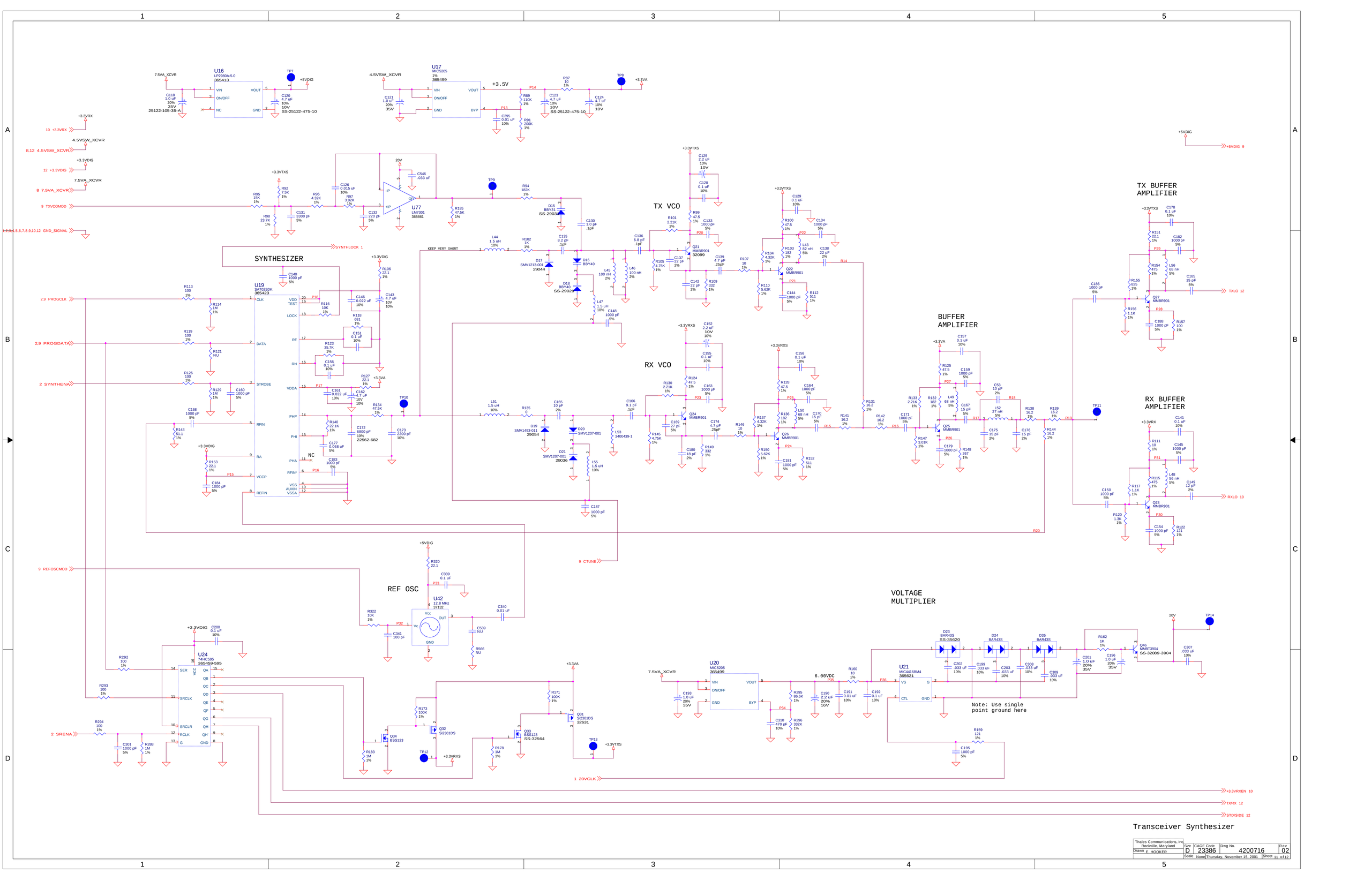
Thales Communications, Inc. Rockville, Maryland	Size D	CAGE Code 23386	Dwg No. 4200716	Rev 02
Drawn E. HOOKER	Scale None	Thursday, November 15, 2001	Sheet 8 of 12	

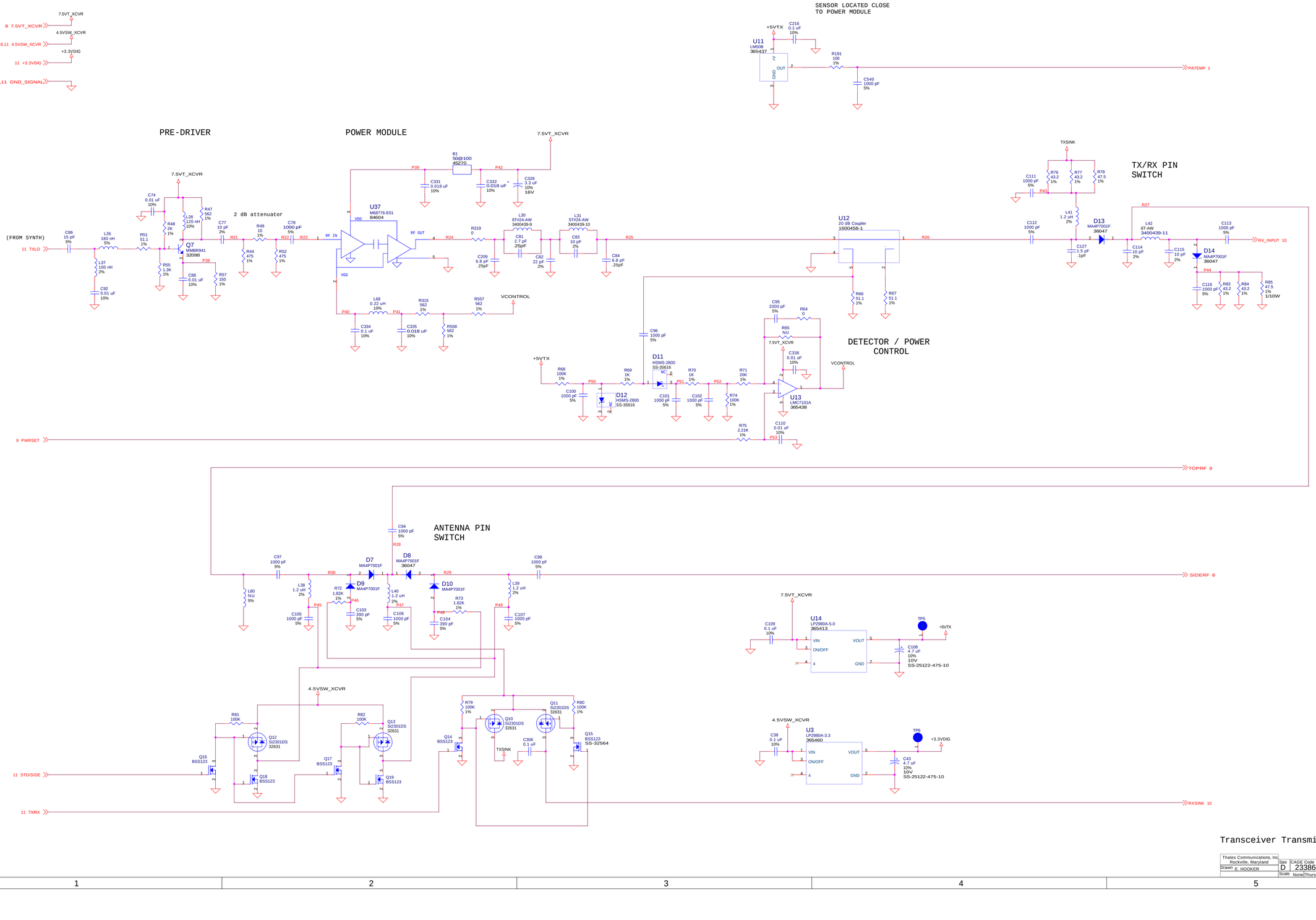


Transceiver DACs

Thales Communications, Inc. Rockville, Maryland		Size	CAGE Code	Dwg No.	Rev
Drawn E. HOOKER		D	23386	4200716	02
		Scale None	Thursday, November 15, 2001	Sheet 9 of 12	


RF AMPLIFIER
2 POLE BANDPASS FILTER
LOWPASS FILTER & IF NOTCH
MIXER
1st IF AMPLIFIER
136-174 MHZ
12 RX_INPUT
9 RXVTF
11 RXLO
181-219MHz
1,2,3,4,5,6,7,8,9,11,12 GND_SIGNAL
2nd LO
IF IC
9 IFAGC
9 2ND_LO_TUNE
2 dB PAD
2nd IF AMPLIFIER
PLACE C230 NEAR PIN 16, C536 NEAR PIN 20
PLACE NEAR U28-9 (VMID)
PLACE NEAR FL3-3
RSSI 1
IFOUT 3
+3.3VRX 11
12 RXSINK
11 +3.3VRXEN
Transceiver Receiver
Thales Communications, Inc
Rockville, Maryland
Drawn E. HOOKER
Size D
CAGE Code 23386
Dwg No. 4200716
Rev 02
Scale None
Thursday, November 15, 2001
Sheet 10 of 12


U16
LP2980A-5.0
365413
U17
MIC5205
1%
365499
+3.5V
SYNTHESIZER
U19
SA7025DK
365423
U77
LM7301
365661
TX VCO
RX VCO
U42
12.8 MHz
37132
REF OSC
U24
74HC595
365459-595
U20
MIC5205
365499
U21
MIC4416BM4
365621
6.00VDC
Note: Use single
point ground here
TX BUFFER
AMPLIFIER
BUFFER
AMPLIFIER
RX BUFFER
AMPLIFIER
VOLTAGE
MULTIPLIER
Transceiver Synthesizer
Thales Communications, Inc
Rockville, Maryland
Drawn E. HOOKER
Size D
CAGE Code 23386
Dwg No. 4200716
Rev 02
Scale None
Thursday, November 15, 2001
Sheet 11 of 12


7.5VT_XCVR
8 7.5VT_XCVR
4.5VSW_XCVR
8,11 4.5VSW_XCVR
+3.3VDIG
11 +3.3VDIG
1,2,3,4,5,6,7,8,9,10,11 GND_SIGNAL
SENSOR LOCATED CLOSE TO POWER MODULE
+5VTX
C216 0.1 uF 10%
U11 LM50B 365437
R191 100 1%
C540 1000 pF 5%
PATEMP 1
PRE-DRIVER
POWER MODULE
7.5VT_XCVR
B1 50@100 45270
C331 0.018 uF 10%
C332 0.018 uF 10%
C328 3.3 uF 10% 16V
U37 M68776-E01 84604
VDD
RF IN
RF OUT
VGG
2 dB attenuator
(FROM SYNTH)
11 TXLO
C86 15 pF 5%
L35 180 nH 5%
L37 100 nH 2%
C92 0.01 uF 10%
C74 0.01 uF 10%
R51 51.1 1%
R48 2K 1%
L28 120 nH 10%
Q7 MMBR941 32098
C88 0.01 uF 10%
R55 1.3K 1%
R47 562 1%
C77 10 pF 2%
R57 150 1%
R21
R49 10 1%
R44 475 1%
C78 1000 pF 5%
R22
R23
R52 475 1%
R24
R319 0
C209 6.8 pF .25pF
L30 6T#24-AW 3400439-9
C81 2.7 pF .25pF
C82 22 pF 2%
L31 5T#24-AW 3400439-10
C83 10 pF 2%
C84 6.8 pF .25pF
R25
L68 0.22 uH 10%
C334 0.1 uF 10%
C335 0.018 uF 10%
R315 562 1%
R558 562 1%
R557 562 1%
VCONTROL
U12 20 dB Coupler 16004588-1
R26
R66 51.1 1%
R67 51.1 1%
TXSINK
C111 1000 pF 5%
R76 43.2 1%
R77 43.2 1%
R78 47.5 1%
C112 1000 pF 5%
L41 1.2 uH 2%
D13 MA4P7001F 36047
C127 1.5 pF 1pF
TX/RX PIN SWITCH
R27
L42 6T-AW 3400439-11
C114 10 pF 2%
C115 10 pF 2%
D14 MA4P7001F 36047
C113 1000 pF 5%
RX_INPUT 10
C116 1000 pF 5%
R83 43.2 1%
R84 43.2 1%
R85 47.5 1% 1/10W
P44
DETECTOR / POWER CONTROL
C95 3300 pF 5%
R64 0
R65 NU
C96 1000 pF 5%
C336 0.01 uF 10%
U13 LMC7101A 365438
D11 HSMS-2800 SS-35616
D12 HSMS-2800 SS-35616
R68 100K 1%
R69 1K 1%
R70 1K 1%
R71 20K 1%
R74 100K 1%
R75 2.21K 1%
C100 1000 pF 5%
C101 1000 pF 5%
C102 1000 pF 5%
C110 0.01 uF 10%
9 PWRSET
TOPRF 8
SIDERF 8
ANTENNA PIN SWITCH
C94 1000 pF 5%
C97 1000 pF 5%
C98 1000 pF 5%
D7 MA4P7001F
D8 MA4P7001F 36047
D9 MA4P7001F
D10 MA4P7001F
L38 1.2 uH 2%
L39 1.2 uH 2%
L40 1.2 uH 2%
L80 NU 5%
R72 1.82K 1%
R73 1.82K 1%
C103 390 pF 5%
C104 390 pF 5%
C105 1000 pF 5%
C106 1000 pF 5%
C107 1000 pF 5%
R28
R29
R30
P45
P46
P47
P48
P49
U14 LP2980A-5.0 365413
C109 0.1 uF 10%
C108 4.7 uF 10% 10V SS-25122-475-10
TP5
+5VTX
U3 LP2980A-3.3 365460
C38 0.1 uF 10%
C43 4.7 uF 10% 10V SS-25122-475-10
TP6
+3.3VDIG
4.5VSW_XCVR
R81 100K
R82 100K
Q12 SI2301DS 32631
Q13 SI2301DS 32631
Q16 BSS123
Q17 BSS123
Q18 BSS123
Q19 BSS123
11 STD/SIDE
11 TX/RX
R79 100K 1%
R80 100K 1%
Q10 SI2301DS 32631
Q11 SI2301DS 32631
Q14 BSS123
Q15 BSS123 SS-32564
C306 0.1 uF
TXSINK
RXSINK 10
Transceiver Transmitter
Thales Communications, Inc. Rockville, Maryland
Drawn E. HOOKER
Size D
CAGE Code 23386
Dwg No. 4200716
Rev 02
Scale None
Thursday, November 15, 2001
Sheet 12 of 12