<SPECIFICATION>

**1. GENERAL**

| | |
|---|---|
| Communication system | One-way communication |
| Frequency range | 429.2500 - 429.7375 MHz |
| Oscillation system | Synthesizer controlled by crystal resonator |
| Transmission system | Digital code transmission |
| Data rate | 2,400bps |
| Identification code | ID code 16 bits (65536 codes)<br>(ID code is set at the factory and cannot be changed by the user.) |
| Service distance | 100 m or greater (However, the range may be shorter depending upon the surrounding, radio wave environment.) |
| Operating temperature range | -10 - DEG. C (Excluding battery) |
| Operating humidity range | 90% RH or less (No condensation) |
| Storage temperature range | -20 - DEG. C (Excluding battery) |
| Storage humidity range | 90% RH or less (No condensation) |

**2. Transmitter**

| | |
|---|---|
| Type of emission | F1D |
| RF output power | 10,797 [micro V/m] or less (3 m distance) |
| Frequency tolerance | 4 ppm |
| Modulation | FM-FSK |
| Supply Voltage | "AA" x 4 (DC 4.0 - 7.0 V) |
| Current Consumption | 50 mA or less (power supply voltage 6 V) |
| Automatic power off | shut down in approximately 4 seconds |
| Antenna | Built-in antenna |

**3. Receiver**

| | |
|---|---|
| Receiving sensitivity | -100 dBm or less (normal temperature) |
| Intermediate frequency | 1ST IF 21.7 MHz<br>2ND IF 450 kHz |
| Supply Voltage | DC 9 - 31 V |
| Current Consumption | 1.2 A or less (Excluding load current) |
| Antenna | 1/4 wave-length whip antenna (flexible, length approx. 160 mm) |

**Description of RF module**

Type of emission F1D
Frequency range 429.2500 - 429.7375 MHz

Transmit frequency synthesizer
The frequency synthesizer is a "pulse-swallowing" type using a TB31213FN integrated circuit. It uses a 21.250 MHz TCXO for its reference source. This IC is programmed to select the individual frequency steps. Programming of this IC is accomplished at power-on time and is controlled by the microprocessor. After receiver selects an unused frequency, it enables the transmitter to begin transmission on that frequency. The operation frequency is selected from predetermined group of ten frequencies listed in the following table:

Programmed Frequency Table

| Step | Group1 | Group2 | Group3 | Group4 |
|---|---|---|---|---|
| 1 | 429.5000 | 429.2500 | 429.5125 | 429.6250 MHz |
| 2 | 429.3750 | 429.2625 | 429.3875 | 429.6375 MHz |
| 3 | 429.2750 | 429.4000 | 429.5250 | 429.6500 MHz |
| 4 | 429.2875 | 429.4125 | 429.5375 | 429.6625 MHz |
| 5 | 429.3000 | 429.4250 | 429.5500 | 429.6750 MHz |
| 6 | 429.3125 | 429.4375 | 429.5625 | 429.6875 MHz |
| 7 | 429.3250 | 429.4500 | 429.5750 | 429.7000 MHz |
| 8 | 429.3375 | 429.4625 | 429.5875 | 429.7125 MHz |
| 9 | 429.3500 | 429.4750 | 429.6000 | 429.7250 MHz |
| 10 | 429.3625 | 429.4875 | 429.6125 | 429.7375 MHz |

**Frequency stabilizing circuitry:**
X101 FTA3001A TCXO (Reference clock of PLL)
I101 TB31213FN PLL synthesizer IC
I401 TK11227M Voltage stabilizer

**Transmitter signal path**
The serial data from microprocessor (logic unit) passes a low-pass filter, and it directly modulates to VCO in PLL. The modulated signal passes a buffer and amplified with RF amplifier. Then, it passes a low path filter to eliminate undesired emissions, and finally transmit from an antenna.

**Modulation restrictions**
Although it is made the composition which gives direct frequency modulation to a voltage controlled oscillator with an modulation signal, a variable resister adjusts an modulation level and it is made to maintain the suitable degree of modulation.

**Power restrictions**
A variable resister adjusts the degree of amplification of a final stage amplifier, and it is made to maintain suitable transmitted electric power.

**Suppressor of spurious radiation**

low-pass filter C101 CH 8pF
C102 CH 12pF
C103 CH 18pF
L101 15nH
L102 15nH

**Receiver signal path**

The signal received with the antenna is amplified with a low noise amplifier. Then, it is changed into the first intermediate frequency with a mixer. The signal of the first intermediate frequency is further amplified with a low noise amplifier, and is inputted into FM detection IC. Inside this IC, FM demodulation signal is carried out, after changing into the second intermediate frequency. And it is inputted into a microprocessor as receiving data.

**Description of modulation**

The modulation signal consists of 16 bits of Identification code, 16 bits operation channel data and 32 bits of error check code. These 64bits are biphase encoded to make 128bits of transmitted data. Eight bits of synchronization code are inserted before the 128 bits data packet.

**Control system**

One microprocessor is controlling generation of the transmitting data by the input of control of a high frequency circuit, switch operation, etc. alone. About control of a high frequency circuit, processing of a frequency setup of a phase lock loop (PLL), a change of transmission and reception, etc. has become main especially.

**Transmitter antenna**

An internal "printed-circuit-board" type antenna is used. There are no provision to attach an external antenna.

**Receiver antenna**

1/4 wave-length whip antenna with RG-58/U cable is used. Receiver antenna terminal is M type connecter.

**Function of each active device**

Q201 2SC5065 RF amplifier (Receiver block)
Q202 2SC5065 1ST IF buffer (Receiver block)
Q301 2SC5065 RF amplifier (Transmitter block)
Q302 2SC5065 RF amplifier (Transmitter block)
Q401 DTA143ZUA Transmitter block power supply control
Q402 DTA143ZUA Receiver block (RF block) power supply control
Q403 DTA143ZUA Receiver block (IF block) power supply control
I101 TB31213FN PLL synthesizer IC
I201 TA31136FN Demodulator
I401 TK11227M Voltage stabilizer