CIRCUIT DESCRIPTION

A general description of the overall circuit is covered in the instruction manual. This section provides the description of circuits required by subpart 2.983 of the Commissions' rules. Circuits not described in the manual are covered in this exhibit.

The following are included:

1.	Means for Carrier Frequency Generation and Stabilization	4A
2.	Means for Modulation Limiting and Low Pass Filter	4B
3.	Means for Harmonic Suppression	4C
4.	Means for Power Limiting	4D

CARRIER FREQUENCY GENERATION AND STABILIZATION

Circuit Description:

The carrier frequency is generated using a fractional-N frequency synthesizer. This consists of a phase-locked loop circuit with a voltage controlled oscillator (VCO) whose output is fed back to a programmable divider chain. The divide ratios are determined from information stored in the memory ICs and bussed to the synthesizer via a microcomputer. The microcomputer extracts the data for the division ratios as determined by the system select switch or by loading data stored in the memory ICs. Using a time averaged algorithm a combination of divide ratios are used so that the reference frequency can be a much higher value than the value of the frequency resolution. Modulation occurs by a combination of directly coupling the modulation signal to the low pass filter in the loop and by processing the digitized analog modulation signal to alter the divider values. A temperature compensated crystal oscillator, operating at 16.8 MHz and stable to 2.0 parts per million over temperature extremes is used for the frequency reference. The 16.8 MHz reference is further divided into one of three reference frequencies which is compared to the divided down VCO output in a phase detector which in turn provides a DC steering voltage back to the VCO.

A Block diagram of the VCO/Synthesizer system is shown below.

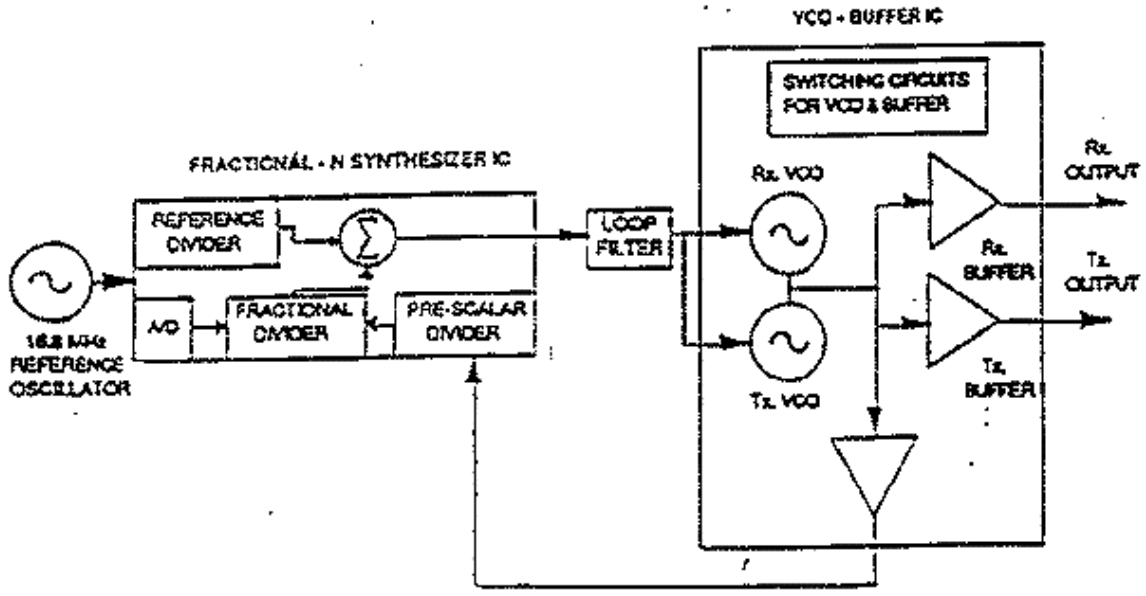


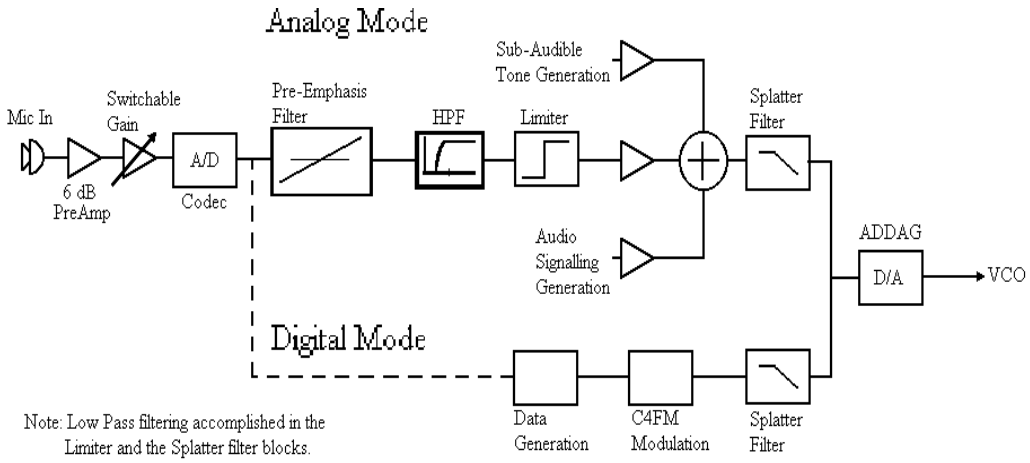
EXHIBIT 4A

MODULATION LIMITING AND LOW PASS FILTERING

Circuit Description:

The pre-emphasis, modulation limiting and low pass filtering of this transmitter are accomplished in the Digital Signal Processor IC (U602) using software implementations of digital filters. Analog audio is digitized in the DSP Support IC (U603) and then transferred to the DSP (U602) where it is pre-emphasized and scaled. Sub-audible tones and audio frequency signaling information is generated in the DSP, scaled, and summed with audio. The combined signal is then filtered using a low pass filter. Signals are then returned to the DSP Support IC (U603) and converted to analog signals. The limited, filtered audio is then fed through digitally programmable attenuators to the modulation ports on the synthesizer module. Digital mode modulation is similar, except no pre-emphasis or summing is required.

A block diagram of the limiting and low pass filtering is shown below.



Modulation Limiting and Low Pass Filtering Scheme

EXHIBIT 4B

HARMONIC SUPPRESSION CIRCUIT

Circuit Description:

Attenuation for harmonics is provided by a low pass filter between the Antenna Switch and the Antenna port. The filter is composed of 7 elements: 5 capacitors and 2 inductors.

Circuit Diagram:

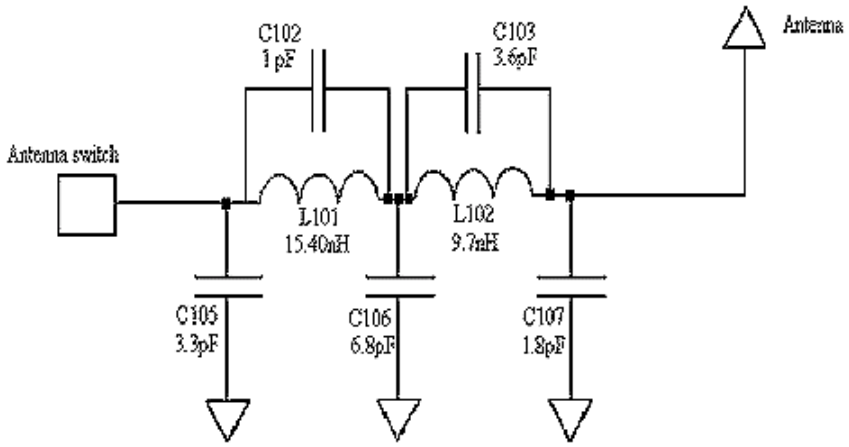


EXHIBIT 4C

POWER LIMITING

The transmitter automatic level control (ALC) circuit consists of the following functional blocks.

AR1 Power Amplifier (PA)
DC1 Directional coupler
D1 RF detector
U1 Power Control IC (PCIC)

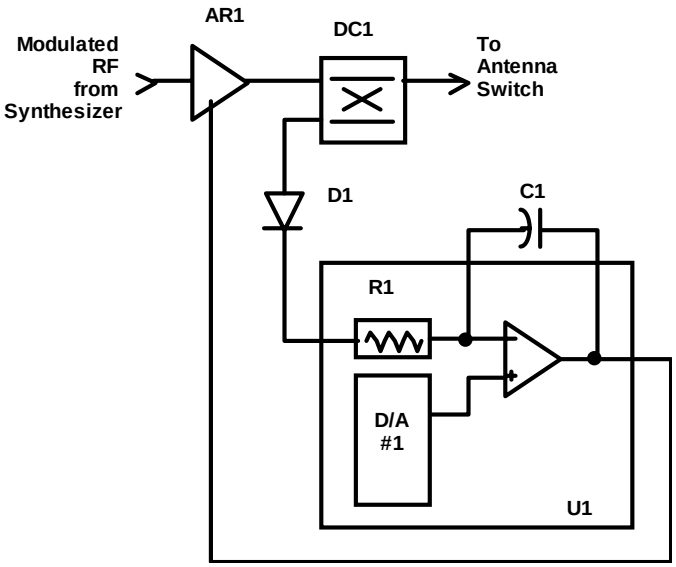


Figure 1 - Transmitter ALC Block Diagram

Power amplifier (PA) AR1 amplifies the modulated radio frequency (RF) signal to the rated output power level of the radio. The PA gain is adjustable by means of a control voltage signal (Vctrl) from the Power Control IC (PCIC). Increasing Vctrl increases the PA gain.

Directional coupler DC1 couples a fixed fraction of the PA forward power into detector D1. The output of detector D1 is a DC voltage (Vdet) with an amplitude proportional to the PA forward power.

At the PCIC (U1) signal Vdet connects to the inverting input of an operational amplifier. Internal D/A converter (D/A#1) is programmed to a reference voltage (Vref) which is proportional to the output power set point. Constants of proportionality are computed by the factory tuning procedure for each radio over the range of powers and frequencies, and stored in the radio's internal non-volatile memory. Vref connects to the non-inverting input of the op-amp. The ALC loop is levelled when Vdet is equal to Vref. PCIC maintains Vctrl at the voltage required to level the loop. Loop transient response is determined by time constants which are set by the PCIC internal programmable resistor R1 and external capacitor C1.

Thus the transmitter ALC maintains a constant power level over all radio operating conditions. Accuracy is determined by the linearity of DC1 and D1, and the settabillity of D/A#1.