1. Receiver System

1-1. Front-end RF amplifier

Incoming RF signal from the antenna is delivered to the Main Unit and passes through low-pass filter, antenna switching diode **D1004** and **D1005** (both **1SS390**), high-pass filter and removed undesired frequencies by varactor tuned band-pass filter **D1007** and **D1009** (both **1SV325**).

The filtered RF signal is amplified by **Q1015** (**BFS505**) and then passes through another varactor tuned band-pass filter **D1013** and **D1014** (both **1SV325**) to remove the undesired frequencies, and then applied to the 1st mixer **Q1020** (**3SK293**).

1-2. First Mixer

The RF signal is mixed with the 1st local signal between 186.85 and 224.85 MHz in the 1st mixer **Q1020** (**3SK293**), to produce 50.85 MHz 1st IF signal.

The 1st local signal is generated by the VCO, which consists of **Q1029** (**CPH3910**), varactor diodes **D1021**, **D1022**, **D1023**, and **D1025** (all **1SV282**). The 1st local signal is supplied to the 1st mixer **Q1020** (**3SK293**) through the buffer amplifier **Q1021** and **Q1026** (both **2SC5010**).

1-3. IF Amplifier & Demodulator

The 1st IF signal passes through monolithic crystal filters **XF1001** (±7.5 kHz BW) to strip away all but the desired signal, and then supplied the buffer amplifier **Q1035** (**2SC5226**).

The amplified 1st IF signal is applied to the FM IF subsystem IC **Q1040** (**AA32416**) which contains the 2nd mixer, 2nd local oscillator, limiter amplifier, noise amplifier, and RSSI amplifier.

The signal from reference oscillator **X1002** (16.8 MHz) becomes three times of frequencies in **Q1040** (**AA32416**), it is mixed with the 1st IF signal and becomes 450 kHz.

The 2nd IF signal passes through the ceramic filter **CF1001** (**LTM450GW**) or **CF1002** (**LTM450EW**) to strip away unwanted mixer products, and is supplied to the limiter amplifier in **Q1040** (**AA32416**), which removes amplitude variations in the 450 kHz IF, before detection of the speech by the ceramic discriminator **CD1001** (**JT-BM450CX24**).

1-4. Audio amplifier

The detected signal from **Q1040** (**AA32416**) is supplied to the AF adder **Q1045-1** (**NJM12902V**) through the TX/RX switch **Q1057-2** (**SN74LV4066A**), high-pass filter **Q1045-2** (**NJM12902V**), and mute switch **Q1057-4** (**SN74LV4066A**).

The audio signal from **Q1045-1** (**NJM12902V**) is supplied to the audio amplifier **Q1008** (**TDA2822L**) through the AF volume potentiometer (VR1001). As a result, the audio signal provides up to 700 mW (@16-ohm BTL) for internal speaker or up to 500 mW (@4-ohm OTL) for external speaker.

1-5. Squelch Circuit

There are 16 levels of squelch setting from “0” to “15”. The level “0” means open the squelch. The level “1” means the threshold setting level and level “14” means tight squelch. From level “2” to level “13” is established in the middle of threshold and tight. The level “15” becomes setting of carrier squelch.

1-5-1. Noise Squelch

The noise squelch circuit is consisted of the band-path filter, noise amplifier **Q1047** (**2SC4617**), and noise detector **D1035** (**DA221**).

When a carrier isn’t received, the noise ingredient which goes out of the demodulator section of **Q1040** (**AA32416**) is amplified by noise amplifier **Q1047** (**2SC4617**) through the band-path filter, and then is detected to DC voltage by **D1035** (**DA221**). The DC voltage is inputted to pin 54 (A/D port) of the CPU **Q1028** (**R5F100LHDFB**). When a carrier is received, the DC voltage becomes low because the noise is compressed.

When the detected voltage to CPU is “High”, the CPU stops the AF output of **Q1013** (**DTC144EE**) by making to “low” of the pin 39 of CPU.

When the detection voltage to CPU is “low”, the CPU allows the AF output of **Q1013** (**DTC144EE**) by making to “High” of the pin 39 of CPU.

1-5-2. Carrier Squelch

The detected RSSI voltage from pin 12 of **Q1040** (**AA32416**) supplied to pin 53 (A/D port) of **Q1028** (**R5F100LHDFB**). It is controls the AF output.

The RSSI output voltage changes according to the signal strength of carrier. The stronger signal makes the RSSI voltage to be higher voltage. The process of the AF signal control is same as Noise Squelch. The shipping data is adjusted 3 dBμ (EMF) higher than squelch tight sensitivity.

2. Transmitter System

2-1. MIC Amplifier

The speech signal from internal microphone **MC1001** or external microphone **J1003** is amplified by **Q1044-2** (**NJM12902V**).

The amplified speech signal from **Q1044-2** (**NJM12902V**) is supplied to pin 14 of Electric Volume IC **Q1018** (**AK2330**) which adjusts the microphone gain through the TX/RX switch **Q1057-2** (**SN74LV4066A**), high-pass filter **Q1045-2** (**NJM12902V**), and other TX/RX switch **Q1057-3** (**SN74LV4066A**).

The adjusted speech signal is output from pin 15 of **Q1018** (**AK2330**), and then passed through the limiter amplifier **Q1044-1** (**NJM12902V**), low-pass filter **Q1044-2/-3** (**NJM12902V**), and AF adder **Q1052-3** (**NJM12902V**).

The processed speech signal from **Q1052-3** (**NJM12902V**) is supplied to pin 22 of Electric Volume IC **Q1018** (**AK2330**) which adjusts the maximum deviation. The adjusted speech signal is amplified by **Q1052-2** (**NJM12904R**), and then is made FM modulation to transmit carrier by the modulator **D1019** (**BB208**) of VCO **Q1037** (**2SC4227**).

2-2. Drive and Final Amplifier Stages

The modulated signal from the VCO **Q1037** (**2SC4227**) is buffered by **Q1026** (**2SC5010**). Then the signal is buffered by **Q1021** (**2SC5010**) and **Q1019** (**2SK3077**) for the driver amplifier **Q1016** (**RQA0004PXDQS**). The low-level transmit signal is then applied to **Q1012** (**RQA0011DNS**) for final amplification up to 5 watts output power.

The transmit signal then passes through the antenna switch **D1003** (**RN1425**) and is low-pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

2-3. Automatic Transmit Power Control

The current detector **Q1053-1** (**NJM12902V**) detects the current of the driver amplifier **Q1016** (**RQA0004PXDQS**) and final amplifier **Q1012** (**RQA0011DNS**), and converts the current difference to the voltage difference.

The output from the current detector **Q1053-1** (**NJM12902V**) is compared with the reference voltage by **Q1053-2** (**NJM12902V**). The output from **Q1053-2** (**NJM12902V**) controls the gate bias of the driver amplifier **Q1016** (**RQA0004PXDQS**) and final amplifiers **Q1012** (**RQA0011DNS**).

The reference voltage changes into two levels (Transmit Power "High" and "Low") controlled by the Electric Volume IC **Q1018** (**AK2330**).

3. PLL Frequency Synthesizer

3-1. VCO (Voltage Controlled Oscillator)

While the radio is receiving, the RX VCO **Q1029** (**CPH3910**) generates a programmed frequency between 186.85 and 224.85 MHz as 1st local signal.

While the radio is transmitting, the TX VCO **Q1037** (**2SC4227**) generates a frequency between 136 and 174 MHz.

The output from VCO is amplified by buffer amplifier **Q1026** and **Q1021** (both **2SC5010**). The buffered VCO is supplied to the 1st mixer **Q1020** (**3SK293**) in case of the reception. In the transmission, the buffered VCO is supplied to other buffer amplifier **Q1019** (**2SK3077**), and then amplified more by **Q1016** (**RQA0004PXDQS**) and it is put into the final amplifier **Q1012** (**RQA0011DNS**).

A portion of the buffered VCO is fed back to the PLL IC **Q1046** (**AK1541**) to control the VCV voltage.

3-2. Varactor Control Voltage

The tuning voltage (VCV) of VCO is established the lock range of VCO by controlling the cathode of varactor diodes **D1021**, **D1022**, **D1023**, and **D1025** (all **1SV282**) for receiving and **D1026**, **D1027**, **D1028**, and **D1029** (all **1SV325**) for transmitting.

3-3. PLL

The PLL IC **Q1046** (**AK1541**) is consists of reference divider, main divider, phase detector, charge pumps, and pulse swallow operation.

The reference frequency from TCXO **X1002** (16.8 MHz) is inputted to pin 10 of PLL IC **Q1046** (**AK1541**) and is divided by reference divider. On the other hand, the feedback signal of the VCO inputted to 17 pin of PLL IC **Q1046** (**AK1541**), and is divided with the dividing ratio which becomes same frequency as the output of reference divider.

These two signals are compared by phase detector, and then phase difference pulse is generated. The phase difference pulse is becomes a DC voltage through the charge pumps and LPF, and it controls the VCO.

The PLL serial data from CPU **Q1028** (**R5F100LHDFB**) is sent with three lines of SDO (pin 5), SCK (pin 6) and PSTB (pin 4).

The lock condition of PLL is output from the UL (pin 7) terminal of the PLL IC **Q1046** (**AK1541**). The UL terminal becomes "High" at the lock condition, and becomes "Low" at the unlock condition.

The CPU **Q1028** (**R5F100LHDFB**) is always watching over the UL condition, and when it becomes "Low" unlocked condition, the CPU prohibits transmitting and receiving.