VX-350 Series Circuit Description

1. Circuit Configuration by Frequency

The receiver is a Double-conversion Super-heterodyne with a first intermediate frequency (IF) of 50.85 MHz and a second IF of 450 kHz. Incoming signal from the antenna is mixed with the local signal from the VCO/PLL to produce the first IF of 50.85 MHz.
This is then mixed with the 50.4 MHz second local oscillator output to produce the 450kHz second IF. This is detected to give the demodulated signal.
The transmit signal frequency is generated by the PLL VCO, and modulated by the signal from the microphone. It is then amplified and sent to the antenna.

2. Receiver System

2-1. Front-end RF amplifier

Incoming RF signal from the antenna is delivered to the RF Unit and passes through Low-pass filer, antenna switching diode **D5003** (**JDP2S12CR**), high pass filter and removed undesired frequencies by varactor diodes **D5007** and 5**009** (both **1SV331**)(tuned band-pass filer). The passed signal is amplified in **Q5021** (**MSG33001**) and moreover cuts an image frequency with the tuned band pass filter **D5016** and 5**018** (both **1SV331**) and comes into the 1st mixer.

2-2. First Mixer

The 1st mixer consists of the **Q5036** (**3SK293**). Buffered output from the VCO is amplified by **Q5031** (**2SC5005**) to provide a pure first local signal between 352.15 and 419.15 MHz for injection to the first mixer.
The IF signal then passes through monolithic crystal filters XF5001 (±5.5 kHz BW) to strip away all but the desired signal.

2-3. IF Amplifier

The first IF signal is amplified by **Q5048** (**2SC5226**).
The amplified first IF signal is applied to FM IF subsystem IC **Q5053** (**NJM2591**) which contains the second mixer, second local oscillator, limiter amplifier, noise amplifier, and S-meter amplifier.
The signal from reference oscillator X5002 becomes 3 times of frequencies in **Q1053**, it is mixed with the IF signal and becomes 450 kHz.
The second IF then passes through the ceramic filter CF5001 (LTM450EW: wide channels), CF5002 (LTM450GW: narrow channels) to strip away unwanted mixer products, and is applied to the limiter amplifier in **Q5053**, which removes amplitude variations in the 450kHz IF, before detection of the speech by the ceramic discriminator CD5001 (JTBM450CX24).

2-4. Audio amplifier

Detected signal from **Q1053** is inputted to mute switch **Q5001- 3** (**SN74LV4066APWR**) and option switch **Q5001-2**. The signal which appeared from **Q5001-2** is in band pass filter **Q5066** (**NJM12902V**).
In the case an optional unit is installed, the **Q5001-2** is made “OFF” and the AF signal from **Q5001-3** goes the optional unit. In the case an optional unit is not installed, **Q5001-2** is made “ON” and the signal goes through **Q5001-2**.
The signal which passed **Q5066** goes to AF volume (VR5001). And then the signal goes to audio amplifier **Q5007**(**NJM2070M**).
The output signal from **Q5007** is in audio speaker.

2-5. Squelch Circuit

There are 16 levels of squelch setting from “0” to “15”. The level “0” means open the squelch. The level 1 means the threshold setting level and level “14” means tight squelch. From “2” to “13” is established in the middle of threshold and tight.
The bigger figure is nearer the tight setting.
The level “15” becomes setting of carrier squelch.

2-5-1. Noise Squelch

Noise squelch circuit is composed of the band path filter of **Q5053**, noise amplifier **Q5058** (**2SC4617**), and noise detector **D5042** and **D5043** (both **DA221**).

When a carrier isn't received, the noise ingredient which goes out of the demodulator **Q5053** is amplified in **Q5058** through the band path filter **Q5053**, is detected to DC voltage with **D5042** and **D5043** and is inputted to 48 pin (the A/D port) of the **Q5044** (CPU: **LC87F5864B**).

When a carrier is received, the DC voltage becomes low because the noise is compressed.

When the detected voltage to CPU is high, the CPU stops AF output with **Q5001-1** "OFF" by making the 39 pin (CPU) "L" level.

When the detection voltage is low, the CPU makes **Q5001-1** "ON" with making 39 pin "H" and the AF signal is output.

2-5-2. Carrier Squelch

The CPU (47 pin: A/D port) detect RSSI voltage output from **Q5053** 12 pin, and controls AF output.

The RSSI output voltage changes according to the signal strength of carrier.

The stronger signal makes the RSSI voltage to be higher voltage.

The process of the AF signal control is same as Noise Squelch.

The shipping data is adjusted 3dB higher than squelch tight sensitivity.

3. Transmitter System

3-1. Mic Amplifier

The AF signal from internal microphone MC5001 or external microphone J5002 is amplified with microphone amplifier **Q5069-2** (**NJM12904**), after passes microphone gain volume **Q5017-CH1** (**M62364FP**).

AF signal is passes a pre-emphasis circuit.

Q5001-1 (**SN74LV4066APW**) becomes "OFF" when an option unit is attached and the AF signal from **Q5068** goes via the option unit. When an option unit isn't attached, **Q5001-1** becomes "ON", the signal passes **Q5001-1** and is input to the limiter amplifier **Q5068-2** (**NJM12902V**).

The signal passed splatter filter of **Q5068** and adder amplifier **Q5065** is adjusted by maximum deviation adjustment volume **Q5017- CH4** (**M62364FP**).

The AF signal ingredient is amplified **Q5065** (**NJM12902V**). After that, it is made FM modulation to transmit carrier by the modulator **D5023** (**HVC383**) of VCO.

3-2. Drive and Final amplifier

The modulated signal from the VCO **Q5049** (**2SC4227**) is buffered by **Q5042** (**2SC5005**) and amplified by **Q5031** (**2SC5005**).

Then the signal is buffered by **Q5026** (**2SC5998**) for the final amplifier driver **Q5020** (**RD01MUS1**). The lowlevel transmit signal is then applied to **Q5013** (**RD09MUP2**) for final amplification up to 5watts output power.

The transmit signal then passes through the antenna switch **D5002** (**HVU131**) and is low pass filtered to suppress away harmonic spurious radiation before delivery to the antenna.

3-3. Automatic Transmit Power Control

The current detector **Q5064-1** (**NJM12902V**) detects the current of **Q5013** and **Q5020**, and converts the current difference to the voltage difference.

The output from the current detector **Q5064-1** is compared with the reference voltage and amplified by the power control amplifier **Q5064-2**.

The output from **Q5064-2** controls the gate bias of the final amplifiers **Q5013** and the final amplifier driver **Q5020**.

The reference voltage changes into four values (Transmit Power High and Low) controlled by **Q5017-CH8** (**M62364FP**).

4. PLL Frequency Synthesizer

The frequency synthesizer consists of PLL IC, **Q5059** (**AK1542**), VCO, TCXO (X5002) and buffer amplifier.
The output frequency from TCXO is 16.8MHz and the tolerance is ±2.5 ppm (in the temperature range –30 to +60 degrees).

4-1. VCO

While the radio is receiving, the RX oscillator **Q5046** in VCO generates a programmed frequency between 352.15 and 419.15MHz as 1st local signal.
While the radio is transmitting, the TX oscillator **Q5049** in VCO generates a frequency between 403 and 470MHz.
The output from oscillator is amplified by buffer amplifier **Q5042** and becomes output of VCO.
The output from VCO is divided, one is amplified by **Q5052** and feed back to the PLL IC 16pin.
The other is amplified in **Q5031** and in case of the reception, it is put into the mixer as the 1st local signal through D5019, in transmission, it is buffered **Q5026**, and more amplified in **Q5020** through **D5019** and it is put into the final amplifier **Q5013**.

4-2. VCO Tuning Voltage

Tuning voltage of VCO is expanding the lock range of VCO by controlling the cathode of varactor diode at the voltage and the control voltage from PLL IC. The control voltage is added to the anode of varactor diode after converted to by **Q5069-1**(**NJM12904**) which is output voltage of D/A converter Q5017-CH1.

4-3. PLL

The PLL IC consists of reference divider, main divider, phase detector, charge pumps and pulse swallow operation. The reference frequency from TCXO is inputted to 10pin of PLL IC and is divided by reference divider.
The other hand, inputted feed back signal to 16pin of PLL IC from VCO is divided with the dividing ratio which becomes same frequency as the output of reference divider.
These two signals are compared by phase detector, the phase difference pulse is generated.
The phase difference pulse and the pulse from through the charge pumps and LPF.
It becomes the DC voltage to control the VCO.
The oscillation frequency of VCO is locked by the control of this DC voltage.
The PLL serial data from CPU is sent with three lines of SDO (64pin), SCK (1pin) and PSTB (32pin).
The lock condition of PLL is output from the UL (7Pin) terminal and UL becomes “H” at the time of the lock condition and becomes “L” at the time of the unlocked condition.
The CPU always watches over the UL condition, and when it becomes “L” unlocked condition, the CPU prohibits transmitting and receiving.