

GMRS-1000

« CIRCUIT DESCRIPTION »

RECEIVER SECTION

Reset = MENU + Δ + ∇]
PWR ON. ←

1. RF AMPLIFIER Circuit.

- * The input signal received through Ant. Terminal goes through L.P.F.(L1,L2,L3,C2~7) and is Applied to RF AMP(Q7).
- * The signal amplified by RF AMP goes through B.P.F.(F1: SAW FILTER) and is applied to 2nd RF AMP(Q8) and is applied to 1st MIX(er) (Q19).

2. MIXER CIRCUIT.

- * The signal amplified at 2nd RF AMP goes to Base of 1st MIX(Q9). Local signal(RX Freq - 21.7MHz) from the PLL is applied to Base of 1st MIX and is Mixed and converted to 21.7MHz.

3. IF AMPLIFIER CIRCUIT.

- * The signal converted to 21.7MHz. at 1st MIX have adjacent signal removed by B.P.F. (F2: Crystal Filter) and is sent to IF AMP. (Q10).
- * The signal amplified by IF AMP. goes to IF-IC (Q11) pin 16. Signal is mixed in MIX circuit in Q11 with 2nd local signal(21.25MHz) and converted to 450KHz and come out as output from pin 3 of Q11.
- * The output signal from pin 3 is supplied to B.P.F.(F3) where adjoining signal are removed and is applied to pin 5. Signal received at pin 5 goes through 2nd IF AMP., limiter, quadrature, detector and comes out through pin 9 as detector output.

4. AUDIO AMPLIFIER SECTION.

- * The detector output from Q11 goes through audio amplifier (Q226). Signals amplified by preamplifier goes through H.P.F. circuit (Q226) and mute circuit (Q222) and L.P.F (Q221) to audio volume control (Q217 - Q220). Signal volume adjusted at Q217 - Q220 goes through AF Power Amplifier (Q231) where the output goes through external speaker jack (J201) to operate internal speaker (E201).

5. SQUELCH CIRCUIT.

- * 30Hz - 30KHz noise part of detector output from Q11 is amplified using the squelch amplifier in Q11.

6. MUTE CIRCUIT.

- * With BUSY SIGNAL going to CPU mute output goes "ON" and "OFF". Pin 66 is mute output for AF power amplifier(Q231) and Pin 65 of Q253 goes to the terminal for AF signal mute.
- * When BUSY output is "HI" Pin 66 is "LO" while Pin 65 will be "HI". When in this condition, mute circuit switch(Q244) for AF Power amplifier goes "ON" and power supply for Q231 is turned "OFF". Also AF signal mute circuit(Q222) will become "OFF" condition and AF signal will go into muted condition.
- * When BUSY output is "LO" the reverse operation will be done.
- * When Buzz sound is to be sounded, only pin 66 of Q253 will go "ON", "OFF".

TRANSMITTER SECTION

1. PRE-AMP.

* Signal from PLL output amplifier goes through TX/RX switch(Q6) and to Pre-AMP (Q18, Q19, Q20) where it is amplified and supplied to Power Amplifier(Q17) as input.

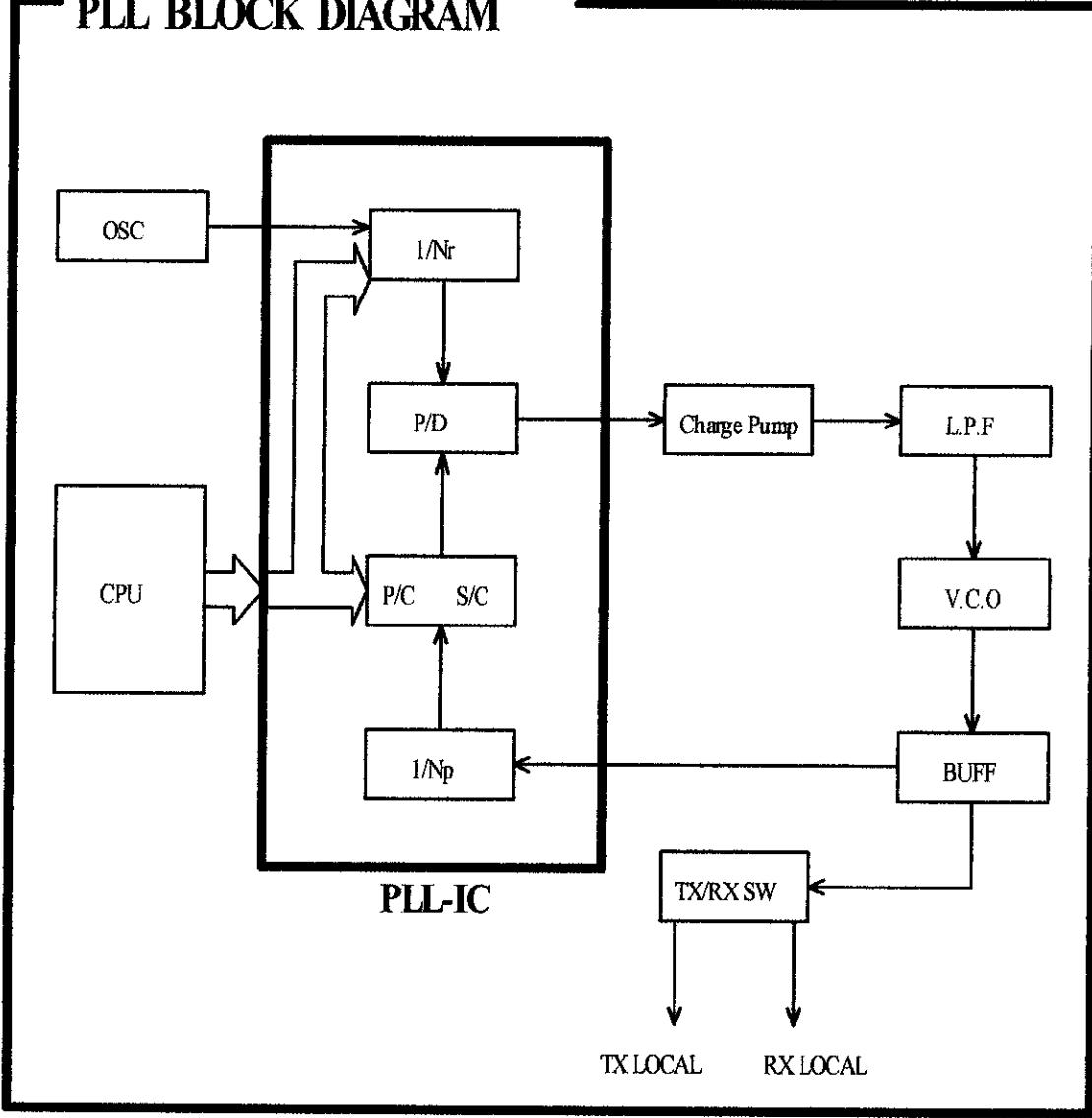
2. POWER AMP.

* Signal is amplified at Power AMP(Q17) to approximatery 3.5W. which goes through L.P.F (L14, C58,59) and to ANT SW(Q1) circuit. After going through ANT SW circuit the signal goes through 3 stage of L.P.F. to reduce the high frequency harmonics and then to ANT terminal.

PLL SECTION

- *PLL Block of this unit is controlled by the micro-processor which is UP DOWN channel switch which is converted to serial data.
- *The PLL operates at the transmit frequency or the required L.O.frequency(receive-21.7MHz) according to whether it is receive or transmit mode.
- *The PLL-IC(Q22) used in this circuit is a pulse swallow type and fundamental oscillator frequency divider,phase comparator,program counter,prescaler are all included internally.

PLL BLOCK DIAGRAM



1. PROGRAMMABLE COUNTER, SWALLOW COUNTER SECTION

* Frequency data goes to micro-processor(Q253) and is processed to 17 bit serial data and divider ratio is set.

* Signal from CPU is added to PLL-IC(Q22) pin No.6(CLOCK), pin No.10(DATA), pin No.11 (STROBE).

Calculation for divider ratio are set by the following;

TRANSMITTING FREQUENCY = Wanted Frequency / Step rate

RECEPTION FREQUENCY = (Wanted Frequency - 21.7MHz) / Step rate

* The signal from V.C.O. goes into pin No.1 of PLL where the prescaler in the PLL-IC divides it by 1/64, 1/65 and goes to the program counter section.

2. PHASE DETECTION CIRCUIT SECTION, CHARGE PUMP SECTION.

* The phase difference between fundamental oscillation frequency (21.25MHz) divided to $1/N_R$ internally in Q22 and frequency from programmable counter are detected.

Detected phase difference comes out as output from pin No.9 passes through Charge Pump and is supplied to PLL loop filter.

3. PLL LOOP FILTER SECTION.

* The signal from charge pump is converted to DC voltage by loop filter consisting of CR integral circuit.

Converted DC voltage is applied to vari-cap diode(Q404) of V.C.O. to change oscillation frequency within V.C.O..

4. V.C.O. CIRCUIT.

* This is an oscillator circuit consisting of LC circuit and Q402. V.C.O. oscillating frequency is controlled by changing voltage applied to vari-cap Q404.

* The V.C.O. of this unit is made to operate wide band and TX/RX switch over circuit are not used, also the V.C.O. are made nonadjustment.

5. PLL OUTPUT CIRCUIT.

* The output of the V.C.O. goes to BUFF AMP(Q401) and is amplified to about -6dBm. This goes to TX/RX switch-over circuit(Q6) and is output to the RX LOCAL and TX LOCAL.

6. POWER SUPPLY CIRCUIT.

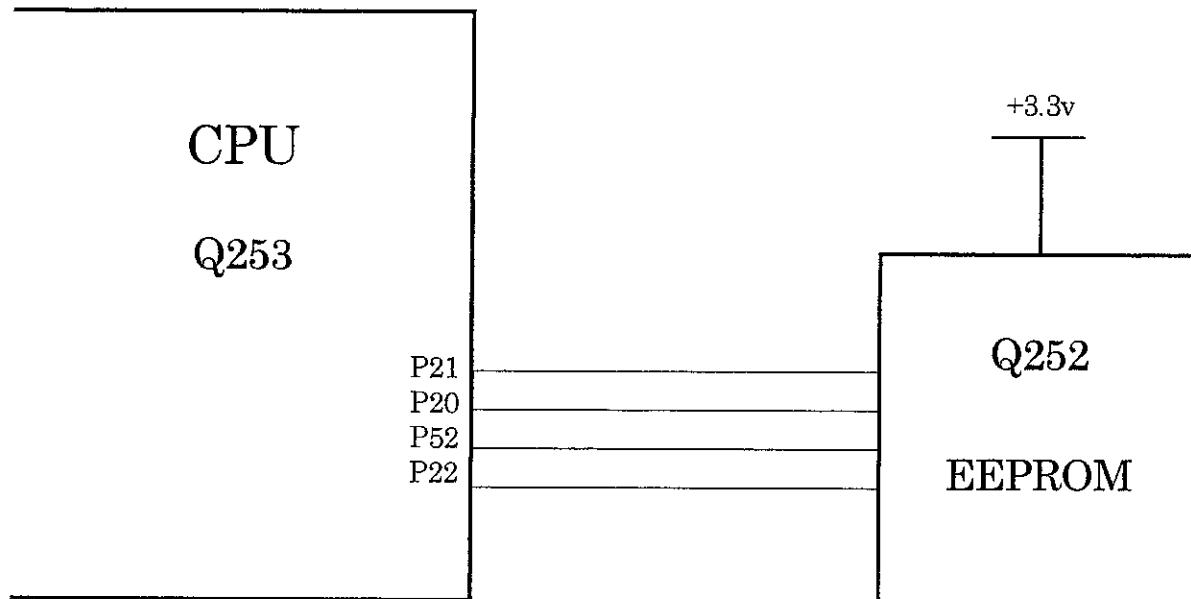
* A constant 3.3V Supply is provided by Q242. The 3.3V line is switched to each of TX SW(Q249), RX SW(Q248), PLL SW(Q247).

* The switch-over of each section is done by command from CPU(Q253).

EXPLANATION OF OPERATION OF CPU

CONTROL SECTION

1. Read in of EEPROM



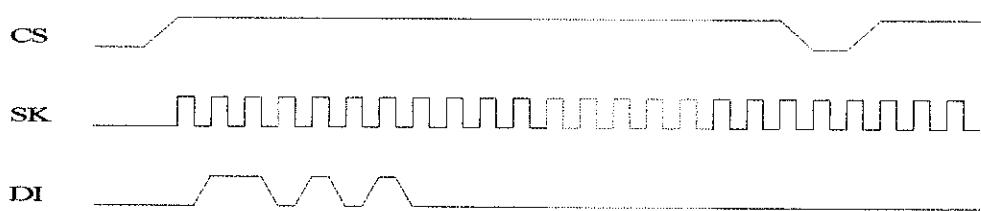
* The EEPROM(Q252) used in this unit has five function of read-out, write-in and others.

These functions are controlled by the CPU(Q253) port P21(DATA), P20(SK), P52(CS) and P22(DO).

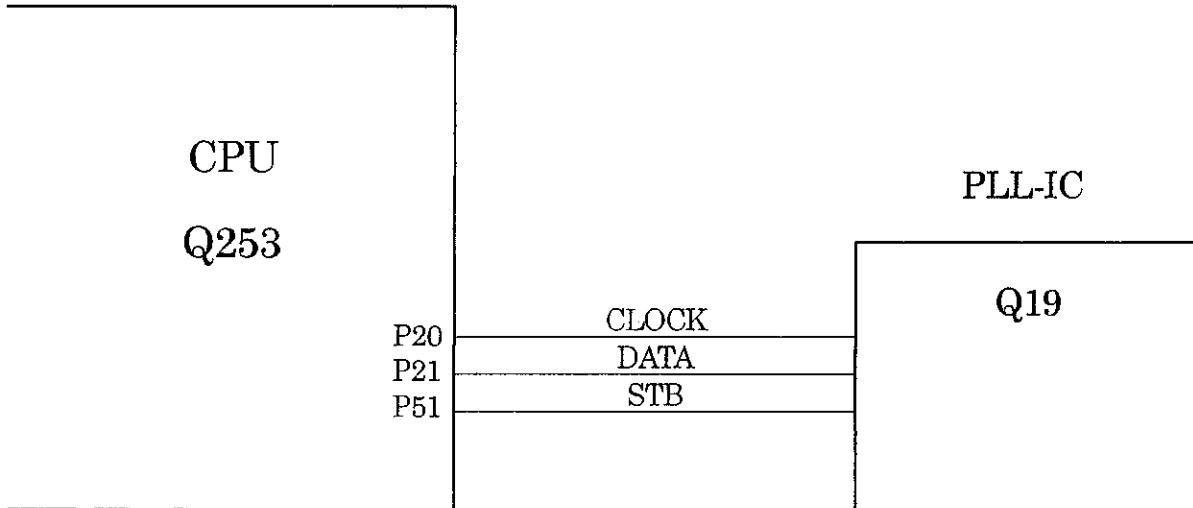
* the contents of EEPROM memory are as shown below:

1. Operate frequency information.
2. Private Code information.
3. Lock information
4. Turn off Beep information
5. Volume Control information
6. Squelch Control information
7. VOX Control information
8. Out of Range information

*the Read out format of EEPROM is as shown below:

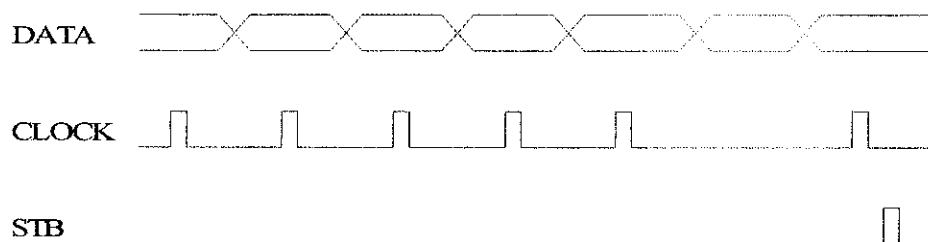


2. CODE OUTPUT FOR PLL-IC.



* P02(CLOCK), P01(DATA), P51(STB) of CPU(Q253) are sent out in serial form to control 12bit programmable reference divider and 17bit programmable devider.
 Output data are sent out in sequence from MSB in synchronization with the CLOCK
 And after the LSB is sent out, one positive pulse is sent out on STB to latch the data.
 In receive mode, when channel UP or DOWN, will be sent out to PLL-IC.

Sending out format is shown in drawing below:



Output data can be calculated with equation shown below:

$$\begin{aligned}
 N(RX) &= (\text{RX Frequency} - 21.7 \text{ MHz}) / \text{Step rate} \\
 N(TX) &= (\text{TX Frequency}) / \text{Step rate}
 \end{aligned}$$