

Technical Description

The Equipment Under Test (EUT) is Bluetooth Cube. The EUT has Bluetooth BLE feature. It is powered by a 3.7V internal rechargeable battery.

2.4GHz Bluetooth portion:

Modulation Type: GFSK

Antenna Type: Integral, Internal

Antenna gain: 0dBi

RF conducted power range: -8dBm to +2dBm

Frequency Range: 2402MHz - 2480MHz

The main components are described as below:

1. U4 BK3231S is 2.4GHz Bluetooth BLE core
2. 16MHz crystal is master clock for U4 BK3231S
3. U5, U6, U7 are motor drivers
4. U2 is 3.3VDC LDO



BK3231S Bluetooth SoC Datasheet

Preliminary Specification

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Disclaimer: Descriptions of specific implementations are for illustrative purpose only, actual hardware implementation may differ.

Revision History

| Rev. | Date | Author(s) | Remark |
|-------------|-------------|-------------------|--|
| 1.0 | 2015-1-7 | Yiming and Guofei | Draft version based on BK3231 datasheet |
| 1.1 | 2016-02-26 | mingsheng | Add the 32PIN SIP package inf |
| 1.2 | 2016.04.08 | Mingsheng.ao | Modified the SIP package removed P22,P23,VPP, added P35,P36,P37 ,which is based on the SIP package |
| 1.3 | 2016.04.11 | Mingsheng.ao | Modified the Description |
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1 General Description

1.1 Overview

The BK3231S chip is a highly integrated SoC, and it supports two wireless protocols, which are Bluetooth Basic Rate (BR), and Bluetooth Low Energy (BLE). It integrates a high-performance 2.4GHz RF transceiver, rich features baseband, ARM-core MCU and various peripheral IOs. It uses up-to-4Mbit external Flash to excute the programmable protocol and profile to support customized applications such as HID, Bluetooth 3D Glasses shutter, Remote controllers.

1.2 Block Diagram

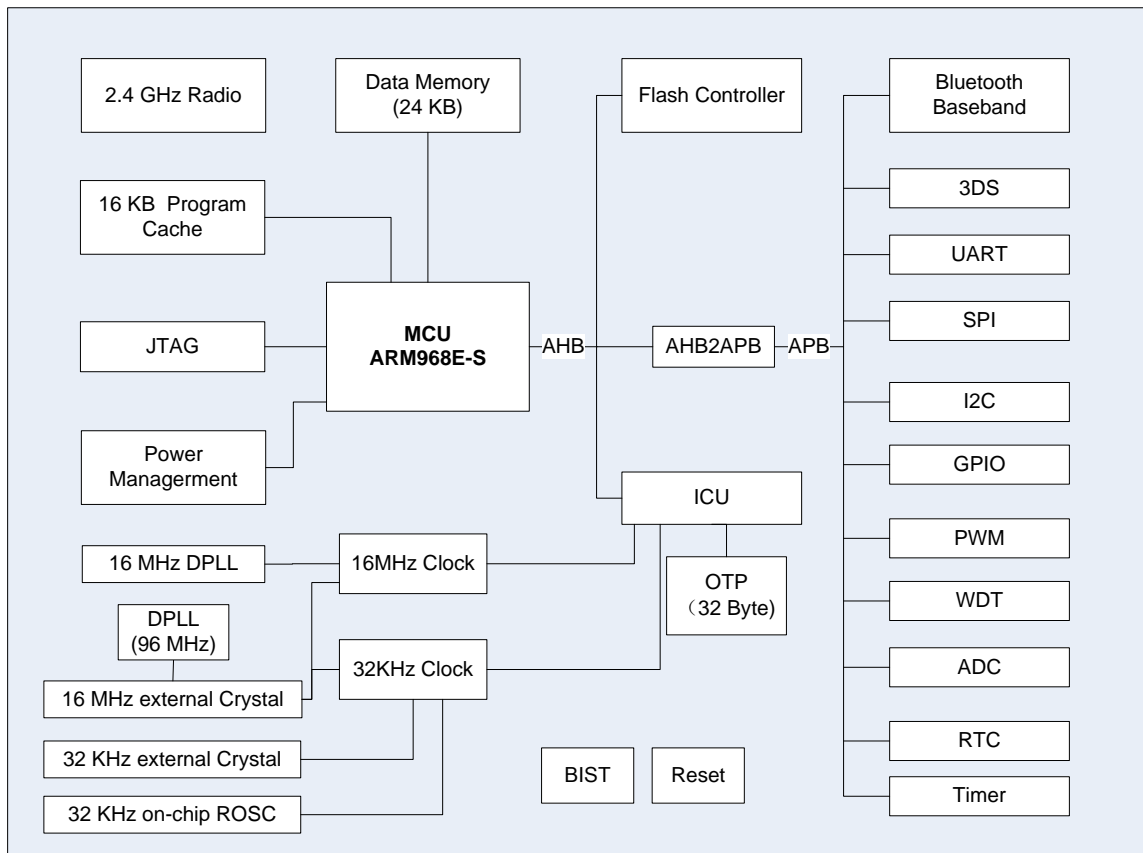


Figure 1 Block Diagram

1.3 Features

- Bluetooth® SIG Bluetooth Dual-Mode compliant
 - Bluetooth 3.0 Basic Rate (BR)
 - Bluetooth 4.0 Low Energy (BLE)
- ARM968 Core MCU integrated
- External Flash up-to-4Mbytes for Program and 24KB RAM for Data
- Low-power 2.4GHz Transceiver
- Operation voltage from 1.8V to 3.6 V
- -89 dBm sensitivity at 1 Mbps data rate and +4dBm transmit power for BLE application
- -86dBm sensitivity for 1 Mbps mode and 2 dBm transmit power for BR application
- External power-amplifier supporting
- Clock
 - 16 MHz crystal reference clock
 - 96MHz optional clock provided by internal DPLL
 - Internal 32kHz low-power oscillator with auto-calibration (± 200 ppm)
 - External 32kHz crystal oscillator as optional low-power clock source
- Interface and peripheral units
 - FLASH programming, JTAG, Dual I2Cs, SPI and UART interface
 - Integrated OTP for customization
 - On-chip high accurate temperature sensor
 - On-chip 7-channel 10bit general ADC
 - 6-outputs PWM
 - 4-outputs 3D Glasses shutter
 - Real-time counter
- Package Type
 - 56-pin QFN 7mmx7mm package
 - 32-pin QFN 4mmx4mm package

1.4 Application

- Wireless Self-Timer
- Wireless Keyboards



- Wireless Mouse
- Wireless Gamepad
- LED Lighting Remote Control
- Bluetooth 3D Glasses

2 Pin Information

The QFN56 package format for the full functions usage. It can be used as keyboard TX part and total 34 GPIO available. The pin assignment for QFN56 package is shown in Figure 2. Other package type such as QFN32 is also available by request with less GPIO.

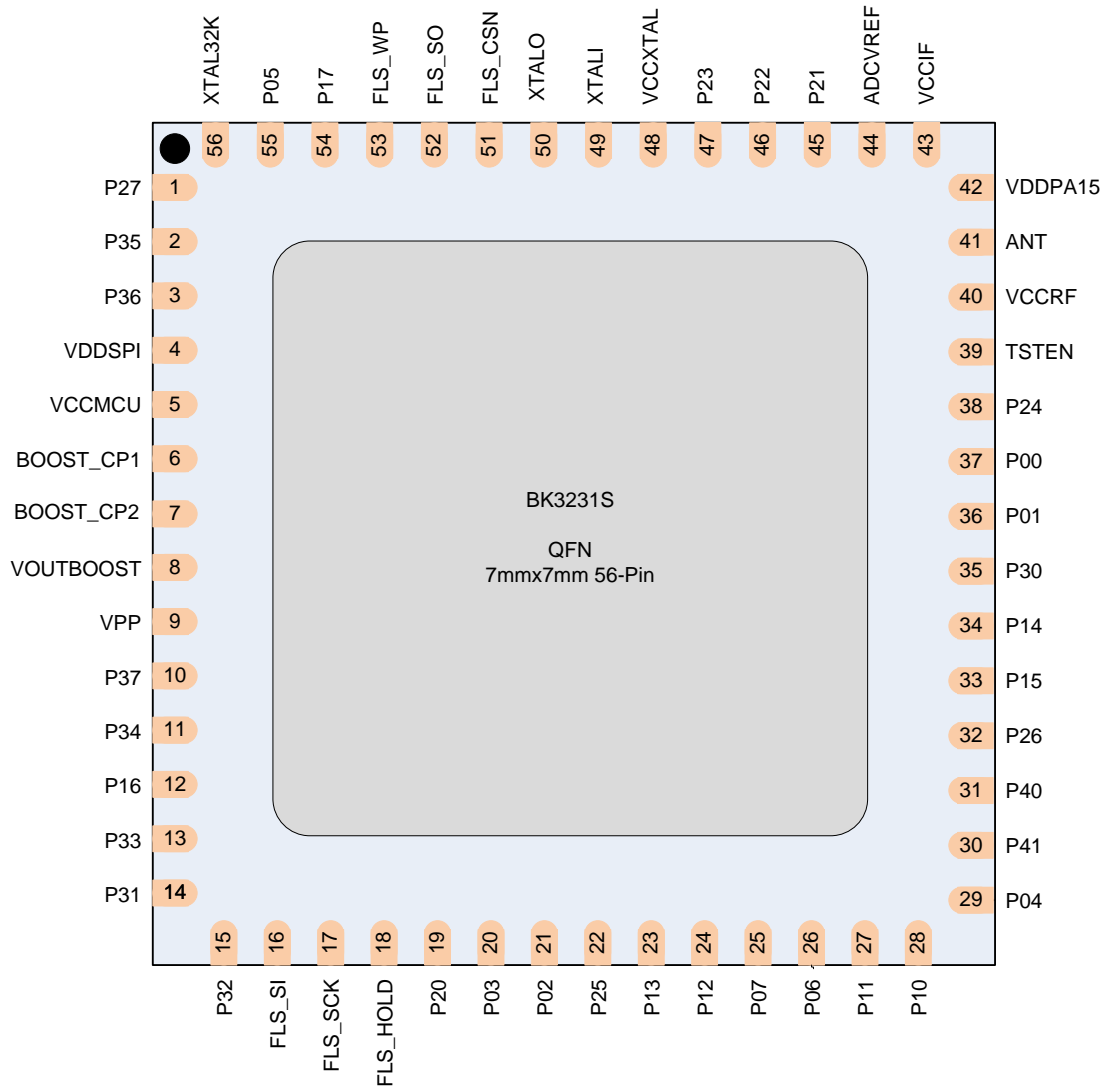


Figure 2 BK3231S QFN56Pin Assignment

Table 1 BK3231S QFN56 Pin Description

| NO | Name | Description |
|----|-----------|---|
| 1 | P27 | General I/O |
| 2 | P35 | General I/O, or input of ADC5 |
| 3 | P36 | General I/O, or input of ADC6 |
| 4 | VDDSPI | The output of digital LDO |
| 5 | VCCMCU | 3V power supply |
| 6 | boost_cp1 | The function PIN of boost,add 100nF cap between boost_cp1 and boost_cp2 |
| 7 | boost_cp2 | The function PIN of boost,add 100nF cap between boost_cp1 and boost_cp2 |
| 8 | voutboost | The output of boost |
| 9 | VPP | The 6V power supply of OTP,it can be used when download |
| 10 | P37 | General I/O, or input of ADC7 |
| 11 | P34 | General I/O, or input of ADC4 |
| 12 | P16 | General I/O, or clock for I2C1 |
| 13 | P33 | General I/O, or input of ADC3 |
| 14 | P31 | General I/O, or input of ADC1 |
| 15 | P32 | General I/O, or input of ADC2 |
| 16 | FLS_SI | The function PIN of flash |
| 17 | FLS_SCK | The function PIN of flash |
| 18 | FLS_HOLD | The function PIN of flash |
| 19 | P20 | General I/O, or UART TX |
| 20 | P03 | General I/O, or 3DS_PWM[3] |
| 21 | P02 | General I/O, or 3DS_PWM[2] |
| 22 | P25 | General I/O, or enable for TIMER1 |
| 23 | P13 | General I/O, or enable for PWM3 |
| 24 | P12 | General I/O, or enable for PWM2 |
| 25 | P07 | General I/O, or chip select for SPI |
| 26 | P06 | General I/O,or MISO for SPI |
| 27 | P11 | General I/O, or enable for PWM1 |
| 28 | P10 | General I/O, or enable for PWM0 |
| 29 | P04 | General I/O, or SCK for SPI |
| 30 | P41 | General I/O, or PLL enable |
| 31 | P40 | General I/O, or PA enable |
| 32 | P26 | General I/O, or enable for TIMER2 |
| 33 | P15 | General I/O, or enable for PWM5 |
| 34 | P14 | General I/O, or enable for PWM4 |
| 35 | P30 | General I/O, or input of ADC0 |
| 36 | P01 | General I/O, or 3DS_PWM[1] |
| 37 | P00 | General I/O, or 3DS_PWM[0] |



| | | |
|----|---------|--|
| 38 | P24 | General I/O, or enable for TIMER0 |
| 39 | TSTEN | Enable the testing function of memory |
| 40 | VCCRF | 3V power supply |
| 41 | ANT | The input of RF |
| 42 | VDDPA15 | The output of PA ldo |
| 43 | VCCIF | 3V power supply |
| 44 | ADCVREF | The output of reference voltage of ADC,it can be connected to a cap on the board |
| 45 | P21 | General I/O, or UART RX |
| 46 | P22 | General I/O, or clock for I2C0 |
| 47 | P23 | General I/O, or data I/O for I2C0 |
| 48 | VCCXTAL | 3V power supply |
| 49 | XTALI | The input of 16M crystal oscillator |
| 50 | XTALO | The input of 16M crystal oscillator |
| 51 | FLS_CSN | The function PIN of flash |
| 52 | FLS_SO | The function PIN of flash |
| 53 | FLS_WP | The function PIN of flash |
| 54 | P17 | General I/O, or data I/O for I2C1 |
| 55 | P05 | General I/O, or MOSI for SPI |
| 56 | XTAL32K | The input of 32K crystal oscillator |

The pin assignment for QFN32 package is shown in Figure 3.

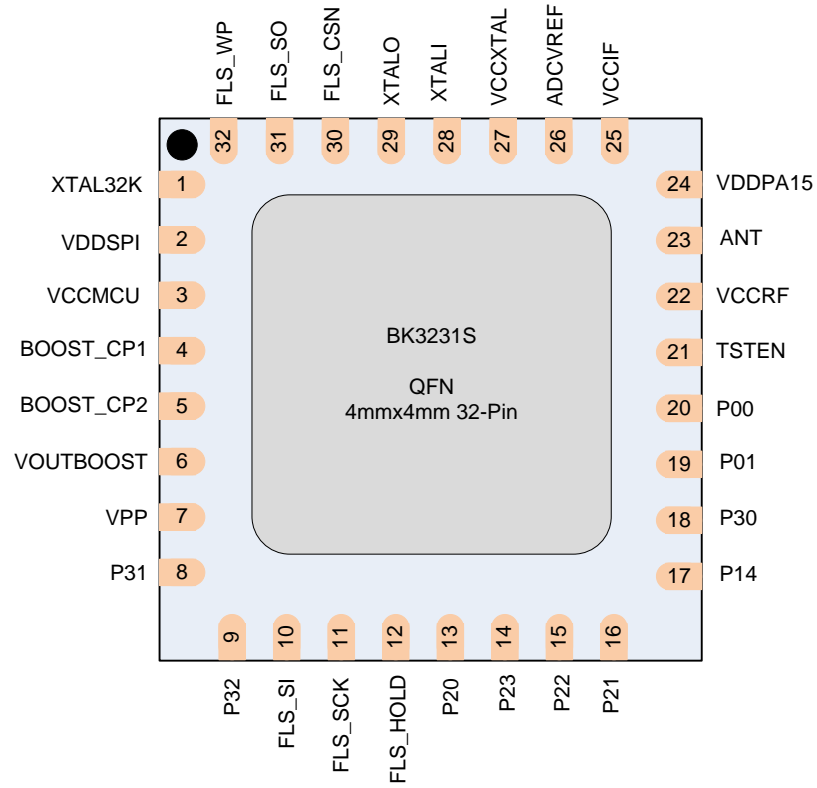


Figure 3 BK3231S QFN32Pin Assignment

Table 2 BK3231S QFN32 Pin Description

| NO | Name | Description |
|-----------|-------------|--|
| 1 | XTAL32K | The input of 32K crystal oscillator |
| 2 | VDDSPI | The output of digital LDO |
| 3 | VCCMCU | 3V power supply |
| 4 | boost_cp1 | Boost function PIN. Add 100nF cap between boost_cp1 and boost_cp2 |
| 5 | boost_cp2 | Boost function PIN. Add 100nF cap between boost_cp1 and boost_cp2 |
| 6 | voutboost | The output of boost |
| 7 | VPP | The 6V power supply of OTP,it can be used when download |
| 8 | P31 | General I/O , or input of ADC1 |
| 9 | P32 | General I/O , or input of ADC2 |
| 10 | FLS_SI | The function PIN of flash |
| 11 | FLS_SCK | The function PIN of flash |
| 12 | FLS_HOLD | The function PIN of flash |
| 13 | P20 | General I/O, or UART TX |
| 14 | P23 | General I/O , or data I/O for I2C0 |
| 15 | P22 | General I/O , or clock for I2C0 |
| 16 | P21 | General I/O, or UART RX |
| 17 | P14 | General I/O , or enable for PWM4 |
| 18 | P30 | General I/O , or input of ADC0 |
| 19 | P01 | General I/O, or 3DS_PWM[1] |
| 20 | P00 | General I/O, or 3DS_PWM[0] |
| 21 | TSTEN | Enable the testing function of memory |
| 22 | VCCRF | 3V power supply |
| 23 | ANT | The input of RF |
| 24 | VDDPA15 | The output of PA ldo |
| 25 | VCCIF | 3V power supply |
| 26 | ADCVREF | The output of reference voltage of ADC. It can be connected to a cap on the board |
| 27 | VCCXTAL | 3V power supply |
| 28 | XTALI | The input of 16M crystal oscillator |
| 29 | XTALO | The input of 16M crystal oscillator |
| 30 | FLS_CSN | The function PIN of flash |
| 31 | FLS_SO | The function PIN of flash |
| 32 | FLS_WP | The function PIN of flash |

The pin assignment for QFN32 package(SIP with flash) is shown in Figure 4

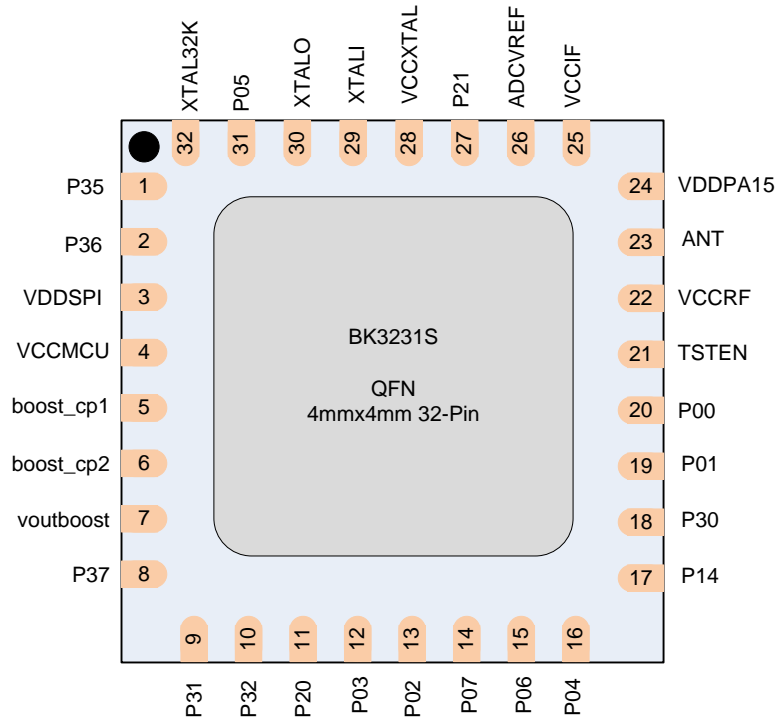


Figure 4 BK3231S QFN32Pin Assignment(SIP with flash)

Table 3 BK3231S QFN32 Pin Description(SIP with flash)

| NO | Name | Description |
|----|------------|--|
| 1 | P35 | General I/O, or input of ADC1 |
| 2 | P36 | General I/O, or input of ADC1 |
| 3 | VDDSPI | The output of digital LDO |
| 4 | VCCMCU | 3V power supply |
| 5 | boost_cp1 | Boost function PIN. Add 100nF cap between boost_cp1 and boost_cp2 |
| 6 | boost_cp2 | Boost function PIN. Add 100nF cap between boost_cp1 and boost_cp2 |
| 7 | voutboost | The output of boost |
| 8 | P37 | General I/O , or input of ADC1 |
| 9 | P31 | General I/O , or input of ADC1 |
| 10 | P32 | General I/O , or input of ADC2 |
| 11 | P20 | General I/O, or UART TX |



| | | |
|----|---------|--|
| 12 | P03 | General I/O, or 3DS_PWM[3], I2C1.SDA, WP_FL A |
| 13 | P02 | General I/O, or 3DS_PWM[2], I2C1.SCL, HOLD_FL A |
| 14 | P07 | General I/O, or SPI_NSS, CSN_FL A |
| 15 | P06 | General I/O, or MISO for SPI, SCK_FL A |
| 16 | P04 | General I/O, or SPI_SCK, SI_FL A |
| 17 | P14 | General I/O , or enable for PWM4 |
| 18 | P30 | General I/O , or input of ADC0 |
| 19 | P01 | General I/O, or 3DS_PWM[1] |
| 20 | P00 | General I/O, or 3DS_PWM[0] |
| 21 | TSTEN | Enable the testing function of memory |
| 22 | VCCRF | 3V power supply |
| 23 | ANT | The input of RF |
| 24 | VDDPA15 | The output of PA Ido |
| 25 | VCCIF | 3V power supply |
| 26 | ADCVREF | The output of reference voltage of ADC. It can be connected to a cap on the board |
| 27 | P21 | General I/O, or UART RX |
| 28 | VCCXTAL | 3V power supply |
| 29 | XTALI | The input of 16M crystal oscillator |
| 30 | XTALO | The input of 16M crystal oscillator |
| 31 | P05 | General I/O, or MOSI for SPI, SO_FL A |
| 32 | XTAL32K | The input of 32K crystal oscillator |

3 Function Description

3.1 Memory Address Mapping

Table 3 The Memory Mapping

| | Start Address | End Address | Total (Bytes) |
|-----------------------|---------------|-------------|---------------|
| Program Memory | | | |
| Flash space | 0x00000000 | 0x0003FFFF | 4M maximum |
| Data Memory | | | |
| SRAM | 0x00400000 | 0x00405FFF | 24K |
| AHB Peripheral | | | |
| ICU | 0x00800000 | 0x0080FFFF | 64K |
| BK24_BB | 0x00810000 | 0x0081FFFF | 64K |
| FLASH CONTROL | 0x00820000 | 0x0082FFFF | 64K |
| AHB2APB | 0x00F00000 | 0x00FFFFFF | 1M |
| APB Peripheral | | | |
| WDT | 0x00F00000 | 0x00F000FF | 256B |
| PWM | 0x00F00100 | 0x00F001FF | 256B |
| SPI | 0x00F00200 | 0x00F002FF | 256B |
| UART | 0x00F00300 | 0x00F003FF | 256B |
| I2C0 | 0x00F00400 | 0x00F004FF | 256B |
| GPIO | 0x00F00500 | 0x00F005FF | 256B |
| RTC | 0x00F00600 | 0x00F006FF | 256B |
| ADC | 0x00F00700 | 0x00F007FF | 256B |
| BT 3DS | 0x00F00800 | 0x00F008FF | 256B |
| I2C1 | 0x00F00900 | 0x00F009FF | 256B |
| Timer | 0x00F00A00 | 0x00F00AFF | 256B |
| XVR | 0x00F10000 | 0x00F1FFFF | 64K |
| CEVA DM IP | 0x00F20000 | 0x00F2FFFF | 64K |

3.2 Interrupt and Clock Unit

The MCU core clock can be selected from three clock sources: 32KHz clock, 16 MHz clock and 96 MHz DPLL.

The ARM968E-S supports two interrupt level. The FIRQ has higher priority than nIRQ. In the BK3231S, all peripheral interrupts are nIRQ except the Bluetooth transceiver. All interrupt can be enabled, disabled, and cleared. There are two low power modes: MCU stop and deep sleep, and any interrupt can be configured to be a wake up source to let MCU exit low power mode.

3.3 GPIO

There are totally 40 general purpose input/output ports (GPIO). All the 40 ports can be used for general I/O with selectable direction for each bit, or these lines can be used for specialized functions.

3.4 ADC

An 8bits SAR-ADC is integrated in the BK3231S. Total 8 channels can be selected used for ADC transfer. The ADC supports continue mode and single transfer mode, and the sample rate can be 1 KHz to 32KHz. In single transfer mode, it will generate interrupt every time after transform.

The ADC has four work modes they are sleep mode, single mode, and software mode and continue mode.

IDLE mode(mode==00): ADC is in idle state.

Single mode(mode==01): The ADC will enter idle mode when transfer is done and waiting MCU to read the result. You should write mode=1 again for another transfer.

Controlled by software (mode==10): In this mode, interrupt will be triggered after transfer and wait MCU to read. The interrupt will be cleared after MCU read, and then the transfer will start again.

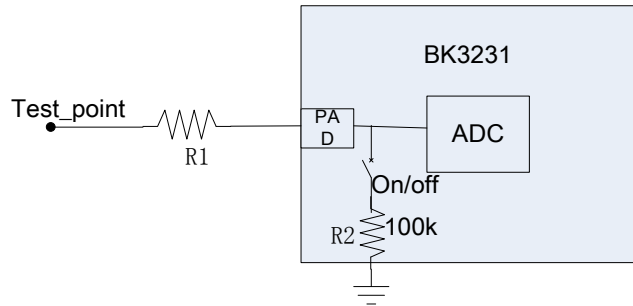
Continue mode(mode==11):The ADC will work at the sample rate set by register. The sample rate can be calculated by the next formula:

$$F_{\text{sample}} = \text{input ADC clock} / (2^{(\text{ADC_CLK_RATE}+2)} / 36(\text{or } 18))$$

The highest sample rate is 32k

The local interrupt flag of ADC need not be cleared by software; it will be set after transform and be cleared after the result has been read out. But the ADC INTstored ICU should be cleared after the ADC INT service finished.

The range of input voltage is from 0v to 1.5V. If the input voltage more than 1.5V, a resistor can be added to decrease the input voltage like the next diagram.



Note: There are eight GPIO can be ADC input. When used as this:

Voltage=data [9:0]/448; the saturate voltage is 1.5 volt.

3.5 UART

The UART interface has 128 bytes FIFO for both TX and RX. It will generate interrupt request when there is risk or event of FIFO underflow or overflow. For the RX, it will generate interrupt if found parity bit check error or stop bit check error.

When the UART RX line goes from idle state ('HIGH') to active state ('LOW') for a set UART clock cycle, it will generate wake up interrupt to activate MCU clock.

3.6 I2C-SMBus

The I2C I/O interface is a two-wire, bi-directional serial bus. The I2C is compliant with the System Management Bus Specification, version 1.1, and compatible with the I C serial bus. Reads and writes to the interface by the system controller are byte oriented with the I2C interface autonomously controlling the serial transfer of the data.

Data can be transferred at up to 1/10th of the system clock as a master or slave (this can be faster than allowed by the I2C specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation.

It is assumed the reader is familiar with the I2C-Bus Specification -- Version 2.0 and system Management Bus Specification -- Version 1.1.

The bi-directional SCL (serial clock) and SDA (serial data) lines must be connected to a positive power supply voltage through a pull-up resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines, so that both are pulled high (recessive state) when the bus is free.

3.7 SPI

The Enhanced Serial Peripheral Interface (SPI) provides access to a flexible, full-duplex synchronous serial bus. SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slaves.

There are four pins for SPI interface. The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. This signal is an output when SPI is operating as a master and an input when SPI is operating as a slave. Data is transferred most-significant bit first. When configured as a master, MOSI is driven by the MSB of the shift register in both 3- and 4-wire mode.

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. This signal is an input when SPI is operating as a master and an output when SPI is operating as a slave. Data is transferred most-significant bit first. The MISO pin is placed in a high-impedance state when the SPI module is disabled and when the SPI operates in 4-wire mode as a slave that is not selected. When acting as a slave in 3-wire mode, MISO is always driven by the MSB of the shift register.

In slave mode, the data on MOSI are sampled at the middle of period of every bit. In master mode, the data on MISO are sampled at the last clock period to acquire the maximal setup time.

3.8 PWM Timer

There are three timers, two of which is 16 bit and can be works as PWM waveform generator, while the other one is 20bit timer. The PWM waveform can be output to GPIO to drive external device such as LED.

3.9 Watch dog

The watch dog is used to reset the whole chip when the firmware runs out of order.

4 Electrical Specifications

4.1 General Specification

Table 4 General Characteristics

| Name | Parameter (Condition) | Min | Typical | Max | Unit | Comment |
|----------------------------|--------------------------|----------|---------|---------|------|---------|
| Operating Condition | | | | | | |
| VCC | Voltage | 1.8 | 3.0 | 3.6 | V | |
| TEMP | Temperature | -20 | +27 | +80 | °C | |
| Digital input Pin | | | | | | |
| VIH | High level | VCC-0.3 | | VCC+0.3 | V | |
| VIL | Low level | VSS | | VSS+0.3 | V | |
| Digital output Pin | | | | | | |
| VOH | High level (IOH=-0.25mA) | VCC- 0.3 | | VCC | V | |
| VOL | Low level(IOL=0.25mA) | VSS | | VSS+0.3 | V | |

4.2 BLE mode

Table 5 BLE mode RF Characteristics

| Name | Parameter (Condition) | Min | Typical | Max | Unit | Comment |
|-------------------------|--|-----|---------|-----|------|---------|
| Normal condition | | | | | | |
| IVDD | Deep sleep | | TBD | | uA | |
| IVDD | Active RX | | TBD | | mA | |
| IVDD | Active TX @ 2 dBm output power | | TBD | | mA | |
| Transmitter | | | | | | |
| PRF | Output power | | 4 | 5 | dBm | |
| PBW | Modulation 20 dB bandwidth | | 1 | | MHz | |
| Receiver | | | | | | |
| Max Input | 1 E-3 BER | 0 | | | dBm | |
| RXSENS | 1 E-3 BER sensitivity | | -89 | | dBm | |
| IIP3 | IIP3, Pin=-63 dBm; P _{unwant} =-39 dBm; f ₀ =2f ₁ -f ₂ , f ₂ -f ₁ =3 MHz or 4 MHz or 5 MHz | | TBD | | dBm | |



| | | | | | | |
|---------|---|--|--|-----|----|--|
| C/ICO | Co-channel C/I | | | TBD | dB | |
| C/I1ST | ACS C/I 1MHz | | | TBD | dB | |
| C/I2ND | ACS C/I 2MHz | | | TBD | dB | |
| C/I3RD | ACS C/I 3MHz | | | TBD | dB | |
| C/I1STI | ACS C/I Image channel | | | TBD | dB | |
| C/I2NDI | ACS C/I 1 MHz adjacent to image channel | | | TBD | dB | |

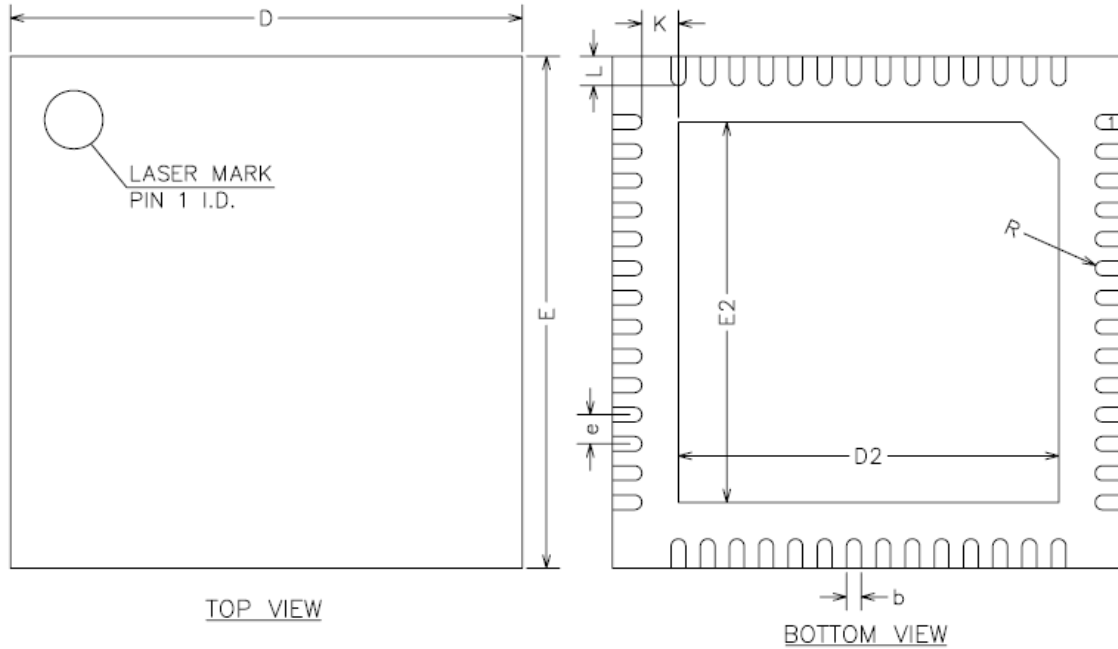
4.3 BR mode

Table 6 BR mode RF Characteristics

| Name | Parameter (Condition) | Min | Typical | Max | Unit | Comment |
|-------------------------|--|-----|---------|-----|------|---------|
| Normal condition | | | | | | |
| IVDD | Deep sleep | | TBD | | uA | |
| IVDD | Active RX | | TBD | | mA | |
| IVDD | Active TX @ 2 dBm output power | | TBD | | mA | |
| Transmitter | | | | | | |
| PRF | Output power | | 2 | 5 | dBm | |
| PBW | Modulation 20 dB bandwidth | | 1 | | MHz | |
| Receiver | | | | | | |
| Max Input | 1 E-3 BER | 0 | | | dBm | |
| RXSENS | 1 E-3 BER sensitivity | | -86 | | dBm | |
| IIP3 | IIP3, Pin=-63 dBm; P _{unwant} =-39 dBm; f ₀ =2f ₁ -f ₂ , f ₂ -f ₁ =3 MHz or 4 MHz or 5 MHz | | TBD | | dBm | |
| C/ICO | Co-channel C/I | | | 11 | dB | |
| C/I1ST | ACS C/I 1MHz | | | 0 | dB | |
| C/I2ND | ACS C/I 2MHz | | | -30 | dB | |
| C/I3RD | ACS C/I 3MHz | | | -40 | dB | |
| C/I1STI | ACS C/I Image channel | | | -9 | dB | |
| C/I2NDI | ACS C/I 1 MHz adjacent to image channel | | | -20 | dB | |

5 Package Information

5.1 QFN 7X7 56PIN:



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|--------|---------|------|------|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | 0.20REF | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 6.90 | 7.00 | 7.10 |
| E | 6.90 | 7.00 | 7.10 |
| D2 | 5.05 | 5.20 | 5.35 |
| E2 | 5.05 | 5.20 | 5.35 |
| e | 0.30 | 0.40 | 0.50 |
| K | 0.20 | - | - |
| L | 0.35 | 0.40 | 0.45 |
| R | 0.09 | - | - |



SIDE VIEW

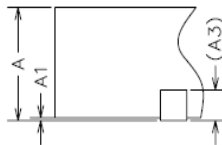
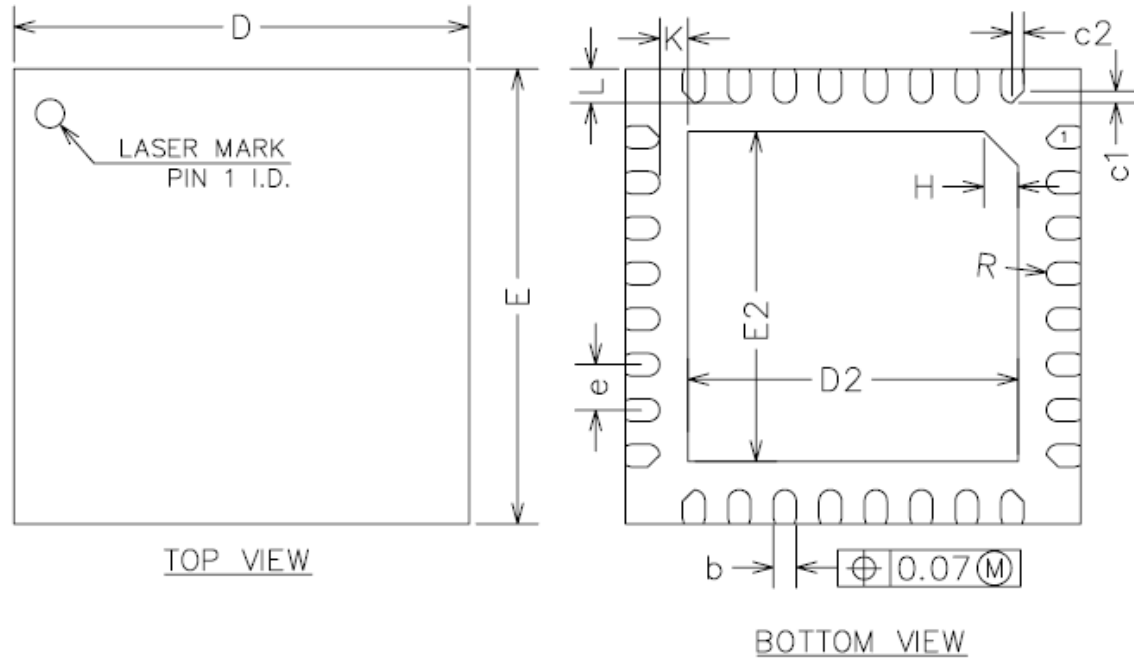


Figure 4 BK3231S QFN56Pin Package Information

5.2 QFN4X4 32PIN:



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

| SYMBOL | MIN | NOM | MAX |
|--------|---------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0 | 0.02 | 0.05 |
| A2 | 0.60 | 0.65 | 0.70 |
| A3 | 0.20REF | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 |
| D2 | 2.80 | 2.90 | 3.00 |
| E2 | 2.80 | 2.90 | 3.00 |
| e | 0.30 | 0.40 | 0.50 |
| H | 0.30REF | | |
| K | 0.25REF | | |
| L | 0.25 | 0.30 | 0.35 |
| R | 0.09 | - | - |
| c1 | - | 0.10 | - |
| c2 | - | 0.10 | - |

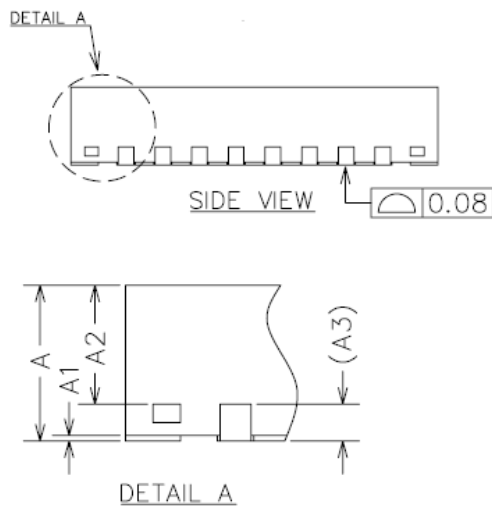


Figure 5 BK3231S QFN32Pin Package Information

6 Application Schematic

6.1 QFN7X7 56PIN:

TBD

6.2 QFN4X4 32PIN:

TBD

7 Order Information

Table 6 Order Information

| Part number | Package | Packing | Minimum Order Quantity |
|-------------|--------------------|-----------|------------------------|
| BK3231SQB | QFN7x7-56Pin | Tape Reel | 3000 |
| BK3231SQ32 | QFN 4mmx4mm 32-Pin | Tape Reel | 10K |

8 Contact Information

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