CIRCUIT DESCRIPTION

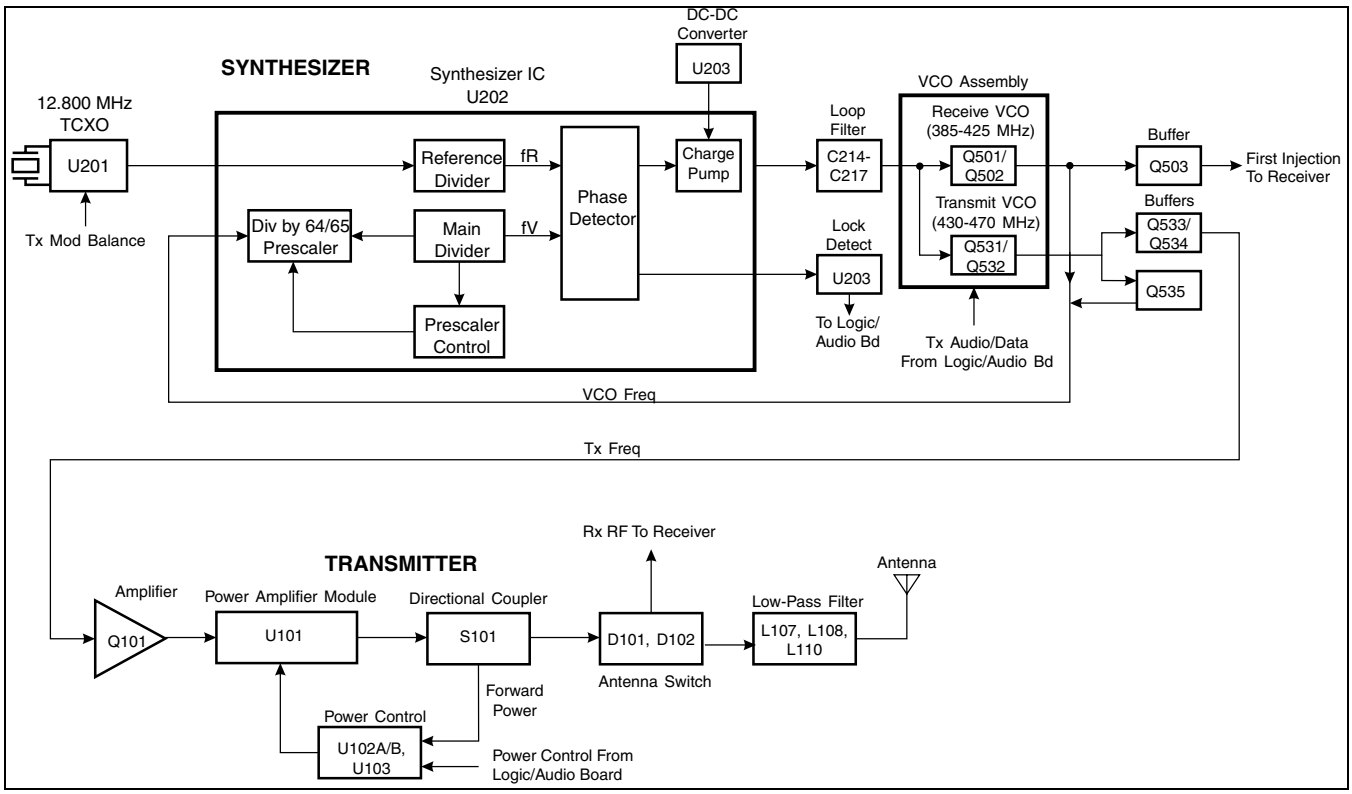

Figure 1 Synthesizer and Transmitter Block Diagram

GENERAL

The 7240 Portable is a compact two-way radio consisting of an RF board, Logic/Audio board, and Keypad/Display board. The RF board is shielded by a metal case. The radio is powered by a 7.5V NiMH battery pack and has a side connector that permits external access to many radio control functions and electrical connections.

The 4-watt transmitter operates in the 430-470 MHz range. It is modulated with microphone audio, subaudible signaling and squelch control signals, and in-band audio tones. To generate the fundamental transmitter frequency, the exciter incorporates phase lock technology to control the stability of the internal voltage controlled oscillator (VCO) with a very stable reference signal provided by an internal temperature compensated crystal controlled oscillator (TCXO). The synthesizer produces an output signal at the assigned transmitter frequency. A voltage-controlled oscillator (VCO) operating at the fundamental transmitter frequency produces this signal. A phase locked loop (PLL) controls and stabilizes the VCO frequency and locks it to the frequency of a high stability signal derived from a TCXO with 1.5 PPM stability that is located on the RF board. To suppress frequency pulling during transmission, the exciter isolates the frequency determining circuit from the rest of the transmitter chain with RF buffer amplifiers. If the synthesizer becomes unlocked, it sends a signal to the control logic on the Logic/Audio board which turns off the transmitter to prevent interference with other channels. A removable 3 dB gain antenna is mounted on the top of the radio for RF power transmission.

The circuit description which follows includes TCXO, VCO, Synthesizer/PLL, Exciter, RF Amplifier and Power Control sections.

SYNTHESIZER DESCRIPTION

NOTE: A synthesizer block diagram is located in Figure 1.

INTRODUCTION

The synthesizer output signal is produced separate receive and transmit VCOs on the RF board. The frequency of these VCOs is controlled by a DC voltage produced by the phase detector in synthesizer chip U202. The phase detector senses the phase and frequency of the two input signals. One signal is the reference frequency from TCXO U201, and the other is from the VCO. If these signals are not the same frequency, the phase detector changes the VCO control voltage which changes the VCO frequency until both signals are synchronized. The VCO is then "Locked" on frequency.

Channels are selected by programming the counters in U202 to divide by different numbers. This programming data comes from the microprocessor on the logic board. The frequency stability of the synthesizer in both the receive and transmit modes is determined by the stability of TCXO U201. The stability of this device is 1.5 PPM from –22° to +140° F (–30° to +60°). The receive VCO output signal is buffered and then fed to the receiver as the first injection signal, and the transmit VCO signal is also buffered and fed to the transmitter as the transmit signal.

RECEIVE AND TRANSMIT VCOS, BUFFER AMPLIFIERS (Q503, Q533-Q535)

There are separate receive and transmit VCOs on the RF board. The VCO control voltage is applied to both VCOs, but only one is active at a time because they are powered by separate R5V (receive) and T5V (transmit) power sources.

With the receive VCO, Q501 produces the first injection signal in the range of 385-425 MHz which is then amplified by Q502. With the transmit VCO, Q531 produces the transmit frequency in the range of 430-470 MHz) which is then amplified by Q532.

In the receive mode, part of the Q502 output signal is fed back through C227 and R210 to pin 10 of U202, and then other part is applied to buffer Q503. Filtering is provided by L506, C520, and C521, and the signal is then applied to one of the gates of dual gate GaAs FET mixer Q302. This is the first injection signal, and it is 45.3 MHz below the receive frequency.

In the transmit mode, part of the Q532 output signal is fed back through buffer amplifier Q535 to pin 10 of U202, and the other part is applied to a buffer amplifier formed by Q533 and Q534. This is a cascode amplifier formed by common-emitter stage Q533 and common-base stage Q534. A cascode amplifier provides amplification also good isolation. The output signal from Q534 is then applied to amplifier Q101 in the transmitter.

VCO AND TCXO MODULATION

Both the VCO and TCXO are modulated in order to achieve the required frequency response. If only the VCO was modulated, the phase detector in U202 would sense the frequency change and increase or decrease the VCO control voltage to counteract the change (especially at the lower audio frequencies). Conversely, if only the TCXO was modulated, the VCO frequency would not change fast enough (especially at the higher audio frequency).

However, by modulating both the VCO and TCXO, the two phase detector inputs remain in phase and no frequency shift is sensed. This produces a relatively flat audio response. Potentiometer 4 of U147 on the logic

board balances these signals, and potentiometers 1 and 3 set the data and audio deviation level. R190/R191 set the frequency of the TCXO by adjusting the DC bias of U148B.

SYNTHESIZER CHIP (U202)

Synthesizer chip U202 contains a prescaler, A, N, and reference counters, and a phase detector, and charge pump. Channels are selected by programming the A, N, and reference counters to divide by a certain number. This programming is performed by the microprocessor via the serial data bus which consists of the Clock, Data, and Latch Enable lines (pins 11-14 of U202).

The divide numbers are chosen so that when the VCO is operating at the correct frequency, the VCO-derived input to the phase detector is the same frequency as the TCXO-derived input. The TCXO-derived is produced by the reference counter in U202. This counter divides the 12.8 MHz TCXO frequency by 2388 to produce a 6.25 kHz input to the phase detector. Using a 6.25 kHz reference frequency allows channels to be changed in 6.25 kHz steps.

The VCO-derived input is produced by dividing the VCO frequency using the prescaler and N counter in U202. The divide number of the prescaler is controlled by the output signal from the A counter. The A and N counters function as follows:

Both the A and N counters begin counting down from the programmed number. When the A counter reaches zero, it halts until the N counter reaches zero. Both counters then reset and the cycle repeats. The A counter is always programmed with a smaller number than the N counter. When the A counter is counting down, the control output to the prescaler causes the prescaler to divide by 129. Then when the A counter is halted, the control output changes states and the prescaler divides by 128.

LOCK DETECT (Q201)

When the synthesizer is locked on frequency, the LD (Lock Detect) output of U202 on pin 8 is a high signal. This turns lock detect transistor Q201 off and the Lock Detect signal fed to the microprocessor is low. When an unlocked condition is indicated, low-going pulses appear on pin 8 which turns Q201 on and causes the Lock Detect signal to go high. The transceiver is then disabled by the control logic and an error condition is indicated in the display.

DC-DC CONVERTER (U203), LOOP FILTER

The supply voltage to an internal charge pump in U202 on pin 4 is produced by DC-DC converter U203. The DC-DC converter produces a 9.3-volt supply from the C5V input voltage. This converter has a built-in relaxation oscillator and rectifier. The frequency of operation is determined by L201. The built-in rectifier combined with an internal temperature compensated reference provide a stable output voltage with a minimum number of external components. The output voltage on pin 4 in U203 is filtered by R215, C218, C220 and then fed to pin 4 in U202.

The charge pump output on pin 6 of U202 charges and discharges C214 and C215 in the loop filter to produce the VCO control voltage. The loop filter is formed by R218-R221 and C214-C217. This is a low-pass filter which controls synthesizer stability and lock-up time and suppresses the 6.25 kHz reference frequency.

TRANSMITTER DESCRIPTION

NOTE: A transmitter block diagram is located in Figure 1.

DRIVER AMPLIFIER (Q101), POWER AMPLIFIER MODULE (U101)

In the transmit mode, the output signal from the transmit VCO is the transmit frequency. This signal is buffered by cascode amplifier Q533/Q534 and then fed to driver Q101 which provides the required input level to power amplifier module U101. Impedance matching between Q101 and U101 is provided by L102 and C106.

Power amplifier module U101 provides up to 4 watts of RF power at the antenna jack. It contains two internal amplifier stages, each of which has a separate supply voltage (Vcc, Vbb Control). The supply voltage to the first stage Vbb Control is from the power control circuit, and the supply voltage to the last stages (Vcc) is the unswitched battery supply.

ANTENNA SWITCH AND LOW-PASS FILTER

The antenna is switched between the receiver and transmitter by an antenna switch consisting of D101, D102 and several other components. In the transmit mode, the T5V supply is enabled and current flows through R105, L106, D101, L112, and D102. Since D101 is forward biased, the transmit signal has a low impedance path to the antenna.

L106/C112/D101 and L112/D102 each form discrete quarter-wave line that is AC grounded at one end. When one end of a quarter-wave line is AC grounded, the other end presents a high impedance to the quarter-wave frequency. Therefore, L106/C112 isolate the 5-volt supply from transmitter RF, and the other two circuits isolate the receiver. In the receive mode, D101 and D102 are no longer forward biased so the receive signal has a high impedance path into the transmitter and a low impedance path into the receiver. From the antenna switch the transmit signal is fed to a low-pass filter consisting of C113-C116, C118, and L107-L110. This filter attenuates harmonic frequencies occurring above the transmit band.

POWER CONTROL

The power output circuit maintains a steady power output level by controlling the supply voltage to the first stage in power module U101 (Vbb Control). The output power is monitored using a directional coupler consisting of microstrip two-line coupler, C123, D103, C124 and several other components. Reflected power is dissipated by R107 and forward power is detected by C123 and D103. These couplers produce a DC voltage that is proportional to the forward power.

The rectified DC level is buffered by voltage follower U102A and through R115 to pin 6 of U102B. This stage amplifies the difference between forward power signal on pin 6 and the reference voltage on pin 5. This reference voltage controls the power output, and it is set by the control logic through potentiometer 2 of U147 on the logic board.

As forward power increases, the output voltage on pin 7 decreases. U103 then turns off more which decreases the supply voltage applied to Vbb Control of U101. This decreases power to maintain a stable output level. The opposite occurs if forward power decreases.