DESCRIPTION OF CIRCUITRY

RULE PART NUMBER: 2.983 (d)(10)

THEORY OF OPERATION

1.0 PURPOSE

This report has been prepared to support the application for FCC Type Acceptance PER CODE OF FEDERAL REGULATIONS, TITLE 47, PARTS 2 AND 90 for the transmitter subsystem of the Transcrypt International / E.F. Johnson Radio Systems Model 242-2004 Repeater. The report presents necessary information concerning electrical circuit description, measured performance and physical construction and configuration.

2.0 REPEATER

The repeater facilitates communication between one station and another. It receives a relatively weak signal on an assigned frequency in the 400 to 512 MHz band, demodulates the signal to baseband, and retransmits baseband information at a selected level between 25 W and 125 W on the assigned transmitter UHF frequency between 400 MHz and 512 MHz. The level adjustment is continuous within the 25 W to 125 W range.

In normal operation, no external controls for setting transmitter power and frequency are available to an operator. Only the manufacturer, installation or maintenance personnel can make or change these settings using a personal computer and custom software which are not a part of the operating equipment.

3.0 TRANSMITTER CIRCUIT DESCRIPTION

The transmitter subsystem consists of three assemblies. They are the exciter, the high power amplifier and the RF interface. The exciter is at the head of the transmitter RF chain, and it generates a low level FM signal that is at the fundamental frequency of the transmitter. The high power amplifier boosts the level of the signal produced by the exciter to a selected, controlled level between 25 W and 125 W. The RF interface assembly provides an interface between the transmitter and the power, modulation, monitor and control functions of the repeater.

4.0 EXCITER

The exciter generates a frequency modulated signal at the fundamental transmitter frequency with an output level of nominally 16 dBm. To generate the fundamental transmitter frequency, the exciter incorporates phase lock technology to control the stability of the internal voltage controlled oscillator, (VCO), with a very stable reference signal from an internal temperature compensated crystal controlled oscillator, (TCXO). To suppress frequency pulling during transmission, the exciter isolates the frequency determining circuit from the rest of the transmitter chain with RF buffer amplifiers.

Multilevel voltage regulation isolates the frequency determining circuits from disturbances produced at the primary power source. As a part of the multilevel regulation strategy, the exciter provides internal regulation of critical voltages to ensure frequency stability and noise immunity from external noise sources.

When turning on the repeater, the processor on the main processor card, MPC, down loads the preprogrammed frequency information to the synthesizer integrated circuit, IC, located in the exciter. The synthesizer stores its respective frequency programming information in an internal register. Normally, there is no further update of the stored information. If the synthesizer becomes unlocked, it sends a signal to the MPC which turns off transmission to prevent interference with other channels.

4.1 SYNTHESIZER (U403)

NOTE: Refer to schematic diagrams appended to the end of the report.

The synthesizer produces an output signal at the assigned transmitter frequency. A voltage-controlled oscillator, (VCO) operating at the fundamental transmitter frequency produces this signal. A phase locked loop, (PLL), controls and stabilizes the VCO frequency and locks it to the frequency of a high stability, <0.0001%, (1.0 PPM) signal derived from a temperature compensated crystal controlled oscillator (TCXO), located in the Exciter Assembly. Figure 1 presents the synthesizer integrated circuit input and output connections, and Figure 2 presents the exciter block diagram.

Generally, the power supply connections use networks that keep RF signals from flowing into the power supply circuits. Typically, the circuits have low-pass topologies with cut-off frequencies very much below the operating frequency. In addition, the synthesizer is in a cast aluminum housing, and it has an aluminum cover with an RF gasket to ensure minimum RF leakage. All inter-assembly RF connections use shield coaxial cable.

The characteristic negative feedback process of the VCO PLL causes the phase difference between the VCO and the 17.5 MHz reference signal from the TCXO to be driven to zero. At the heart of the synthesizer is the synthesizer integrated circuit, U403, which controls the VCO frequency. The synthesizer, U403, contains a prescaler, R (reference), N, and A counters, phase detectors, a lock detector and counter programming circuitry. Programming of the counters within U403 causes it to divide by certain numbers which select the desired frequency. J201, pins 12, 19 and 20 provide programming access. Further, U403 receives a 17.5 MHz frequency reference signal from Y401, the voltage controlled, temperature compensated crystal controlled oscillator, TCXO.

A DC voltage produced by the phase detector within U403 controls the VCO. The voltage represents the voltage necessary to tune the VCO to the desired frequency plus the phase error between the VCO signal and the reference signal provided by the TCXO. The phase detector compares the phases and frequencies of two signals and causes the VCO control voltage to increase or decrease in proportion to the phase difference between them. When the phases are the same, the VCO is "locked" and held on frequency with the control voltage remaining constant. Once the VCO is locked to the TCXO source, the PLL only corrects the control voltage of the VCO to compensate for noise and phase drift.

Programming the three internal counters within U403 to divide by predetermined numbers selects the operating frequency. Programming of these counters originates in the Main Processor Card (MPC). Programming information flows from the MPC through the Interface Alarm Card (IAC) and into the synthesizer IC via J401, pin 20 to the Data input port of U403, pin 19.

Within the IC, the phase detector compares two signals designated as f_R and f_V. The internal reference frequency, f_R appears at the output of the R counter. The R counter produces f_R by dividing 17.500 MHz, by a predetermined fixed ratio. The R counter output frequency equals 6.25 kHz. Consequently, the synthesizer reference frequency is equal to 6.25 kHz and the frequency increment, or channel spacing, of the synthesizer is also equal to 6.25 kHz. The other signal frequency, f_V, is the VCO frequency divided by the prescaler and the programmable "N" counter.

Dividing the 17.500 MHz voltage controlled TCXO frequency by 2800 produces the f_R input frequency at 6.25 kHz. Since the VCO is on the final frequency and no frequency multiplication is used, the synthesizer output frequencies change in 6.25 kHz steps. The reference frequency at the phase detector is always 6.25 kHz.

Data applied to J401, pin 20 sets the N counter divide ratio. Each channel has a unique programming number so that the corresponding phase detector input frequency is identical to the reference frequency when the VCO is locked on the desired channel frequency.

Data loads into U403 serially on the Data input port at pin 19. Data clocks serially into the internal shift registers one bit at a time as a result of a low to high transition on the Clock input port at pin 18. The necessary number of Clock pulses come from the MPC via the IAC to J401, pin 19. For U403 to respond to data on this line, an ENABLE signal (Figure 2, "SYN CS EX) must be applied to pin 17 during the programming process period. Using an enabling signal protects the synthesizer from arbitrary reprogramming during other operations of the MPC.

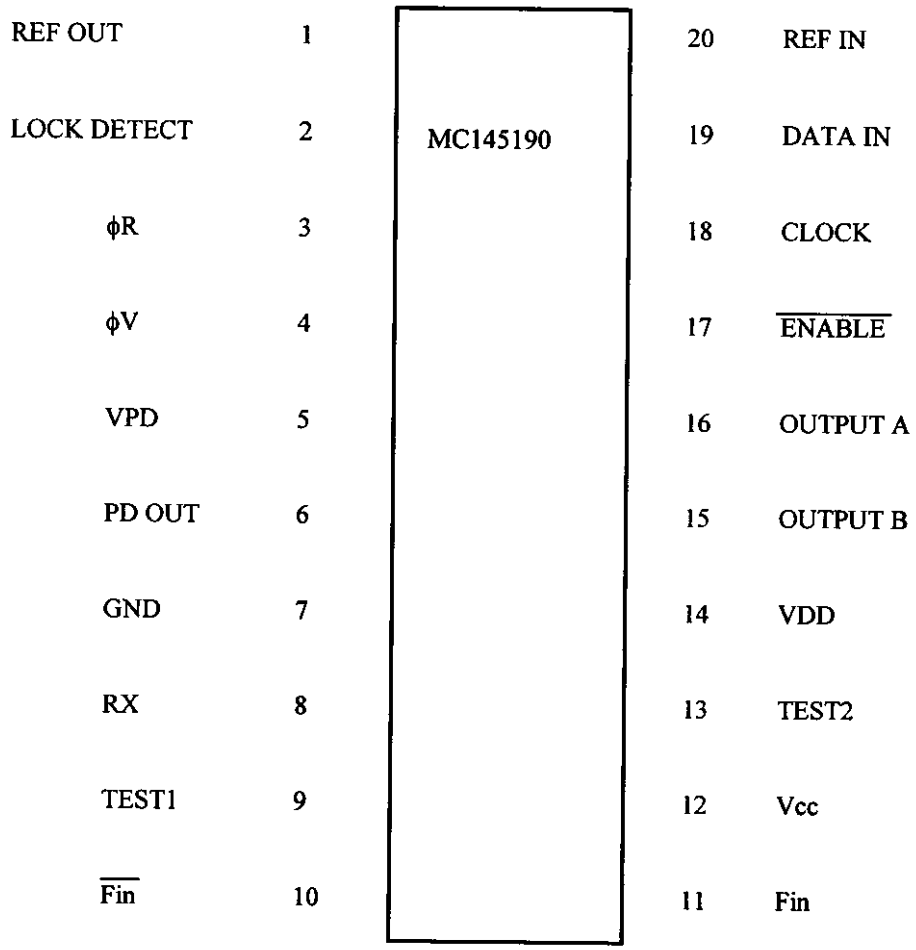

Figure 1. Synthesizer IC - MC145190

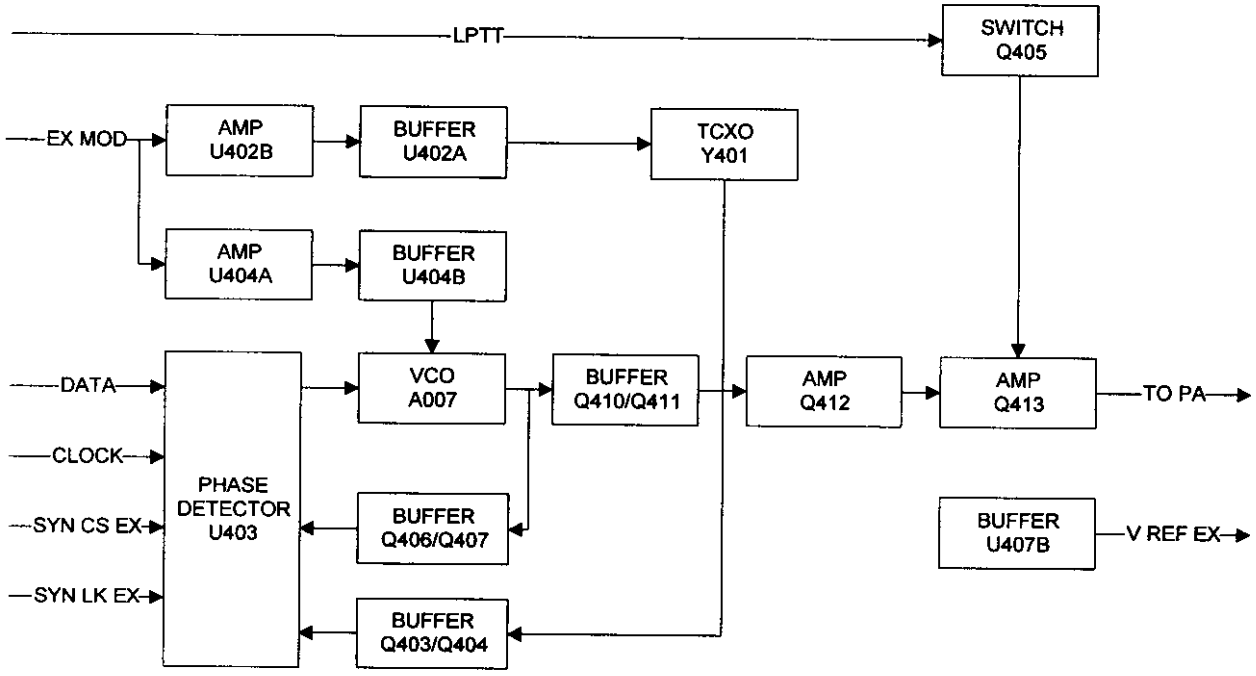

Figure 2. Exciter block diagram

Dividing the VCO frequency using the prescaler and N counter in U403 produces the f_V input signal frequency. Depending on the state of the N and A counters, the control logic within the VCO PLL sets the prescaler to divide by either 64 or 65. The N and A counters function as follows:

Both the N and A counters begin counting down from their programmed numbers. When the A counter reaches zero, it halts until the N counter reaches zero. Both counters then reset and the cycle repeats. The A counter is always programmed with a smaller number than the N counter. While the A counter is counting down, the prescaler divides by 65. When the A counter stops, the prescaler divides by 64.

Example: To illustrate the operation of these counters, assume a transmitter frequency of 450.250 MHz which is also the VCO frequency. To produce this frequency, the N and A counters are programmed as follows:

N = 1125 A = 40

To determine the overall divide number of the prescaler and N counter, one determines the number of VCO output pulses required to produce one N counter output pulse. In this example, the prescaler divides by 65 for 65 x 40 or 2600 input pulses. Then it divides by 64 for 64 x (425 - 40) or 69,440 input pulses. Consequently, the overall divide number, K, is (69,440 + 2600) or 72,040. The VCO frequency of 450.250 MHz divided by 72,040 equals 6.25 kHz which is the f_R input to the phase detector. The overall divide number K can also be determined by the following formula:

$K = 64N + A$

Where,

N = N counter divide number and
A = A counter divide number.

4.2 LOCK DETECTION

When the synthesizer is locked on frequency, the "Lock Detect" output signal from U403, pin 2 is on the average at a high level because the signal has a high duty cycle with only narrow negative-going pulses. When the synthesizer is unlocked, the signal is on the average at a low level because the duty cycle is low.

R440 and C423 form a low pass filter which produces an average dc signal representing the lock condition of the PLL. The filtered signal goes to J401, pin 16 and to the RF Interface J102, pin 16 for "locked" or "unlocked" status detection.

4.3 VCO AND TCXO FREQUENCY MODULATION

Both the VCO and TCXO are modulated by sub-audible control data and the information being transmitted in order to achieve the required frequency response. If only the VCO were modulated, the phase detector in U403 would be able to sense a frequency change at the sub-audible frequencies and would correspondingly vary the VCO control voltage to counteract it. Conversely if only the TCXO frequency were modulated, the VCO frequency would not respond fast enough at the higher audio frequencies of the information to achieve the desired frequency deviation. However, by modulating both the VCO and the TCXO, the inputs signals at the two phase detectors remain in phase and thereby they sense no frequency shift which results in a flat audio response. Potentiometers R425 and R446 balance the modulating signals.

4.4 BUFFER AMPLIFIER (Q410, Q411)

A cascode amplifier formed by Q410 and Q411 provides amplification and isolation between the VCO and exciter RF stages. A cascode amplifier provides high gain, high isolation and consumes only a small amount of power. The input signal to the amplifier is tapped from VCO A007 on pin 5. C441 provides DC blocking. Bias for the amplifier is provided by R458, R465, R466, R467 and R468. L406 is a RF choke and R463 lowers the Q of the coil. RF bypass is provided by C461, C442, C457, C444, and C480. The output of Q410/Q411 is terminated into a 6 dB attenuator made up of R459, R460, and R461.

4.5 RF AMPLIFIERS (Q412, Q413)

RF amplifier Q412 is biased by CR402, R469, and R470. C448 provides RF bypass from the DC line and R471, R472 provides supply voltage isolation. L409 on the collector acts as an RF choke to the supply line. The input to Q410 is matched to 50 ohms by C450 and L408. The output of Q410 is matched to 50 ohms by C449, L410, and C451 and then terminated into a 6 dB attenuator made up of R473, R474, and R475.

RF amplifier/buffer Q413 is similar in design to Q412. The collector and base voltage of Q413 is switched by Q405. The Logic Push-To-Talk (LPTT) on J401, pin 11 turns on Q405 and conducts the 15 V supply to the collector of Q405 and to Q413. The output of Q413 is matched to 50 ohms by L412 and C510. C465 provides DC blocking. The RF output of the exciter is on coaxial connector J402 to the power amplifier.

5.0 POWER AMPLIFIER (PA) (Refer to Figure 3)

The PA boosts the signal level from the exciter to a nominal preset value between 25 W and 125 W at any selected frequency between 400 and 512 MHz. An automatic level control loop sets and maintains the output level at the desired programmed value. The level control loop uses the microprocessor which resides on the Main Processing Card (MPC) assembly and provides programmable control of the RF output level by monitoring it at the DIRECTIONAL COUPLER assembly and controlling it with a voltage applied to the gain control pin of U501.

Generally, the RF stages use construction technology, circuit topology and other techniques that inhibit signal leakage, harmonic and spurious signal generation. The housing is made of machined aluminum and has an

aluminum cover that makes good contact with the housing to ensure minimum RF leakage. The RF circuits use microstrip construction which minimizes radiation and leakage because the signal and ground conductors are very close together. Each RF amplifier stage contains tuned networks that match the external circuits to the input and output impedance of the transistors at the RF operating frequency. Further, being frequency sensitive, the networks limit signal power flow at harmonic and spurious frequencies. In addition, the power supply bias connections use networks that keep RF signals from flowing into the power supply circuits. Typically, the bias circuits have low-pass topology with cut-off frequencies very much below the operating frequency.

5.1 PRE-DRIVER GAIN BLOCK U501

The RF input signal flows through U501. Amplifier, U501, boosts the level to approximately 5 Watts. The automatic level control loop controls the gain control voltage of U501 to achieve the programmed final output level. Following the pre-driver, the signal flows to the driver amplifier stage.

5.2 DRIVER Q502

Coming from the pre-driver, the RF signal flows into the driver stage Q501 which, operating as a common drain amplifier, boosts the level to approximately 12 watts. The circuit consists of transistor, Q501, and a combination of lumped element components and printed microstrip transmission lines which match the input and the output impedance of the transistor to the input and output impedance of the stage.

5.3 FINAL AMPLIFIER Q502 AND Q503

The final amplifier stage consists of two transistor amplifiers, Q502 and Q503, operating in parallel and coupled to the input and output connections of the stage by microstrip power divider and combiner networks. These networks are in the class of balanced bridge circuits commonly called Wilkinson combiners (dividers). At the input is a two way Wilkinson divider which splits the RF signal. A microstrip network in one leg delays the signal by 180°. At the outputs of the transistors amplifiers, a similar and reciprocal network combines the two amplified signals in-phase, and couples the combined signal to the output connection of the stage.

Each of the final transistor amplifiers is similar to the driver stage. Each amplifier, operating as a common drain amplifier, and boosts the level to approximately 125 watts. The circuit consists of a transistor, and a combination of lumped element components and printed microstrip transmission lines which match the input and the output impedance of the transistor to the input and output impedance of the stage.

The Wilkinson divider has the attribute that the outputs are nominally isolated from each other and that any mismatch power will nominally flow into an imbedded resistor rather than into the other companion amplifier. As a consequence, if one of the transistors fails, the other will continue operating with normal signal characteristics but with reduced output power.

5.3.4 POWER DETECTORS

In the MPC, embedded software monitors the individual operational status of the two amplifiers in the final stage through POWER SENSE circuits. A power sensing circuit at the output of each amplifier couples a small amount of the RF signal to a detector that converts it to a proportional dc voltage, POWER SENSE. From the amplifiers, the two detected signals flow to the RF Interface Board which communicates to the software function. When an amplifier fails, the software monitor process senses the condition, modifies the control process and reduces the programmed output power level via the amplitude control voltage at U501 to prevent over driving the remaining operational stage.

5.4 FORWARD AND REVERSE POWER DETECTOR, CIRCULATOR

A short jumper connects the output from the final amplifier stage to the directional coupler assembly. A circulator assembly, embedded between the forward and reverse power directional detectors, protects the transistors in the final and earlier stages from the consequences of power reflected from the load attached to the antenna terminal. The consequences can include spurious oscillation and destruction of the transistors.

Further, the circulator separates the directional couplers from each other and the forward directional coupler from load mismatches; as a result, the directivity of the forward power directional coupler and the accuracy of the forward power measurement are high and independent of any load mismatches.

Each directional coupler circuit consists of a microstrip directional coupler element and a diode detector, U601 or U651. The detector converts the RF signal power to a proportional dc voltage. The detected voltages flow to the RF Interface Board which communicates with the embedded processor and the monitor and RF power control software processes.

5.5 LOW-PASS FILTER

Situated between the circulator and the RF output, the low-pass filter provides rejection of harmonics of the fundamental transmitter frequency and spurious signals to ensure that the equipment meets emission specifications. The circuit is a nine element low-pass microstrip structure. It has a nominal -3 dB cut-off frequency at 680 MHz.

5.6 THERMAL SENSOR (U507)

Temperature sensor U507 provides thermal protection. The active operating range of the sensor is from 0° C to +100° C (+32° F to +212° F). Amplifier U506A operates as a buffer amplifier. When the temperature reaches +50° C at the sensor, it actuates control circuits which turn on the fan; and at +45° C, it turns the fan off. Furthermore, circuits within the RF Interface board reduce the RF output level to one-half power if the temperature exceeds 90° C; and if the temperature exceeds 95° C, they turn off the PA.

TRANSISTOR, DIODE, AND IC FUNCTIONS

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Transmitter

Designator	Part Number JEDEC or Vendor Type	Function
Power Amplifier:		
A011	023-2004-600 EFJ0232004600	UHF Low Pass Filter
A010	023-2004-660 EFJ0232004660	FWD/REV Power Detector
CR601	523-1504-033 BAS70	Detector Diode
CR651	523-1504-033 BAS70	Detector Diode
U601	544-2019-004 LM2904	Op Amp
U651	544-2019-004 LM2904	Op Amp
U652	544-2603-039 LM78L05ACM	Voltage Regulator, 5 Volts
U501 400-430 MHz	544-4001-067 M67709M	RF Predriver
U501 430-470 MHz	544-4001-065 M67709	RF Predriver
U501 470-512 MHz	544-4001-068 M67709SH	RF Predriver
Q501	576-0006-119 MRF175LU	RF Final
Q502	576-0006-119 MRF175LU	RF Final
Q503	576-0006-119 MRF175LU	RF Final
U502	544-2039-002 MAX472ESA	Current Sense IC
U503	544-2039-002 MAX472ESA	Current Sense IC
U504	544-2039-002 MAX472ESA	Current Sense IC
U505	544-2039-002 MAX472ESA	Current Sense IC
CR501	523-2016-100 BZX84C10LT1	Varactor Diode
CR502	523-2016-100 BZX84C10LT1	Varactor Diode
CR503	523-2016-100 BZX84C10LT1	Varactor Diode
U507	544-2032-003 LM35DM	Temperature Sensor
U506	544-2019-004 LM2904	Buffer Amplifier
U508	544-2603-039 LM78L05ACM	Voltage Regulator

Designator	Part Number JEDEC or Vendor Type	Function
Power Amplifier: Continued		
U509	544-2603-039 LM78L05ACM	Voltage Regulator
Exciter:		
Q412	576-0003-604 MRF5812	Buffer
Q413	576-0004-098 MRF8372	Buffer
Synthesizer and VCO:		
U403	544-3954-026 MC145190	Synthesizer/Prescaler
Q406	576-0003-658 MMBT3904L-T1	Buffer
Q407	576-0003-636 NE85633	Buffer
Q410	576-0003-658 MMBT3904L-T1	Buffer
Q411	576-0003-636 NE85633	Buffer
Q801	576-0001-300 MMBT5089LT1	Capacitance Multiplier
Q802	576-0003-636 NE85633	VCO
CR801	523-5005-022 BB535	Modulation Varactor
CR802	523-5005-022 BB535	VCO Varactor
CR803	523-5005-022 BB535	Varactor Diode
TCXO:		
Y401	518-7117-500 EFJ 17.5 MHz TCXO	1.0 PPM TCXO
Q403	576-0003-658 MMBT3904L-T1	Buffer
Q404	576-0003-658 MMBT3904L-T1	Buffer

TRANSMITTER TUNE UP PROCEDURE

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TRANSMITTER TUNE UP PROCEDURE

1.0 Set R663 on F/R Power Detect Board fully clockwise. Set R510, R521, and R530 on the PA board fully counter clockwise.

2.0 Use and ohmmeter to verify all feed-through capacitors are not shorted to ground except for the feed-through that is ground.

2.1 Inspect the Power Amplifier. Make sure that the RF power transistors are properly soldered and that all components/connections from the final collectors to the circulators are properly soldered.

3.0 Connect the power supply Ground lead to P105, the 15.0 Vdc lead to P103, the 26.5 Vdc lead to P101, and the 36 pin cable to J101 on the RFIB.

3.1 Connect an attenuator and power meter to A8.

3.2 Adjust R76 on the RFIB to attain 2.5 volts dc on pin 6 of U111.

3.3 While monitoring the current on P101, adjust R510 to set the input current to 100mA ±2.5 mA. Set R521 to add another 100 mA ±2.5 mA (200 mA ±5.0 mA total) to the total current measured. Set R530 to add another 100 mA ±2.5 mA (300 mA ±7.5 mA total) to the total current measured. Verify that the total input quiescent current is 300 mA ±7.5 mA.

4.0 Run PC Test Software and set the power level to #160.

5.0 Set the RF Signal Generator to +18 dBm ± 0.2 dB @ 415.000 MHz for Range 3 RF decks.
Set the RF Signal Generator to +18 dBm ± 0.2 dB @ 450.000 MHz for Range 4 RF decks.
Set the RF Signal Generator to +18 dBm ± 0.2 dB @ 490.000 MHz for Range 5 RF decks.

6.0 Key the transmitter.

7.0 Adjust Forward Power Calibration Pot R663 to 125 Watts ± 0.1 dB (±3 Watts).

8.0 Verify from the test computer that Output 1 is within 20% of Output 2, and Output 3 is less than #130.

9.0 Measure the output power at 400 MHz and 430 MHz for Range 3 RF decks.
Measure the output power at 430 MHz and 470 MHz for Range 4 RF decks.
Measure the output power at 470 MHz and 512 MHz for Range 5 RF decks.
Verify that the output power is 125 Watts ±0.25 dB (±5 Watts). Set the RF signal generator back to the appropriate frequency as detailed in #5 above.

10.0 Unkey the transmitter.

11.0 Set power level to #160. Remove load cable from A8, the Transmit Antenna Connector. Key the transmitter.

TRANSMITTER TUNE UP PROCEDURE

Continued

12.0 Adjust Reverse Power Calibration Pot R680 for equal voltages on W126 and W121 or by setting Forward Power and Reverse Power equal on the test computer. Unkey the transmitter.

13.0 Apply "Glyptol" to R76, R510, R521, R530, R663, and R680.

14.0 Toggle F3 on the test computer to verify that the fan(s) turn on and off.

15.0 Measure the temperature detector voltage @ W127 on the RFIB. Normal output at +25° C ambient is approximately 2.1 Vdc.

TX Power: 25 Watts Minimum.; 125 Watts Maximum.; TX Current: 18.0 A Maximum

INSTRUCTION BOOK

RULE PART NUMBER: 2.983 (d)(8)

A complete Service Manual/Operators Manual is attached with this filing.