SECTION IV

THEORY OF OPERATION

4.1 GENERAL

This manual covers KX 165A configurations.

4.1.1 KX 165A FEATURES

The KX 165A is a single unit, panel mounted communication transceiver/navigation receiver with glideslope receiver and VOR/LOC Converter. The functional capabilities are:

A. A microprocessor controlled communication transceiver which operates from 118.00 MHz to 136.975 MHz in 8.33 kHz increments providing 2280 channels. 32 programmable memories.

B. A microprocessor controlled navigation receiver for VOR/LOC signals from 108.00MHz to 117.95MHz in 50kHz increments providing 200 channels.

C. A microprocessor controlled glideslope receiver operating from 329.15 MHz to 335.00 MHz in 150kHz increments for 40 glideslope channels.

D. A microprocessor controlled VOR/LOC converter capable of calculating and displaying bearing VOR radial digitally.

E. A microprocessor controlled VOR/LOC converter I/O board for use with indicators that do not contain an internal converter.

F. DME Channeling

1. Provides data to interface with KN 62/A/64 DME or the KDI 572/574 or KPI 553A indicator which will in turn control the KN 63 DME or the KDM 706 DME.

2. Provide data to interface with KA 120 Adapter which will in turn channel 2 x 5 or slip code DME's.

G. Digital Display of:

1. Communication "USE" and "STANDBY" frequencies.
2. Navigation "USE and "STANDBY" frequencies.
3. VOR Radial information displayed in navigation "STANDBY" window.
4. Internal course deviation indicator for VOR and localizer.
5. Elapsed timer: countdown and elapsed time.

H. Navigation and Communication frequency information is stored in a non-volatile memory. Information is stored when the radio is turned off and will re-channel to the same frequencies when turned on.

I. Front panel lighting of bezel and knobs.

4.2 BLOCK DIAGRAM THEORY OF OPERATION

Refer to Figure 4-1 for the following block diagram explanation. The KX 165A Navcom transceiver includes a VHF communication receiver and transmitter, VOR Navigation receiver, glideslope receiver, VOR/LOC converter I/O, front panel with display, power supply, and central processing unit with various interface circuits. The CPU controls the functions of the unit, and includes memory, I/O, and several other functions. Each major function block diagram is described in subsequent sections.

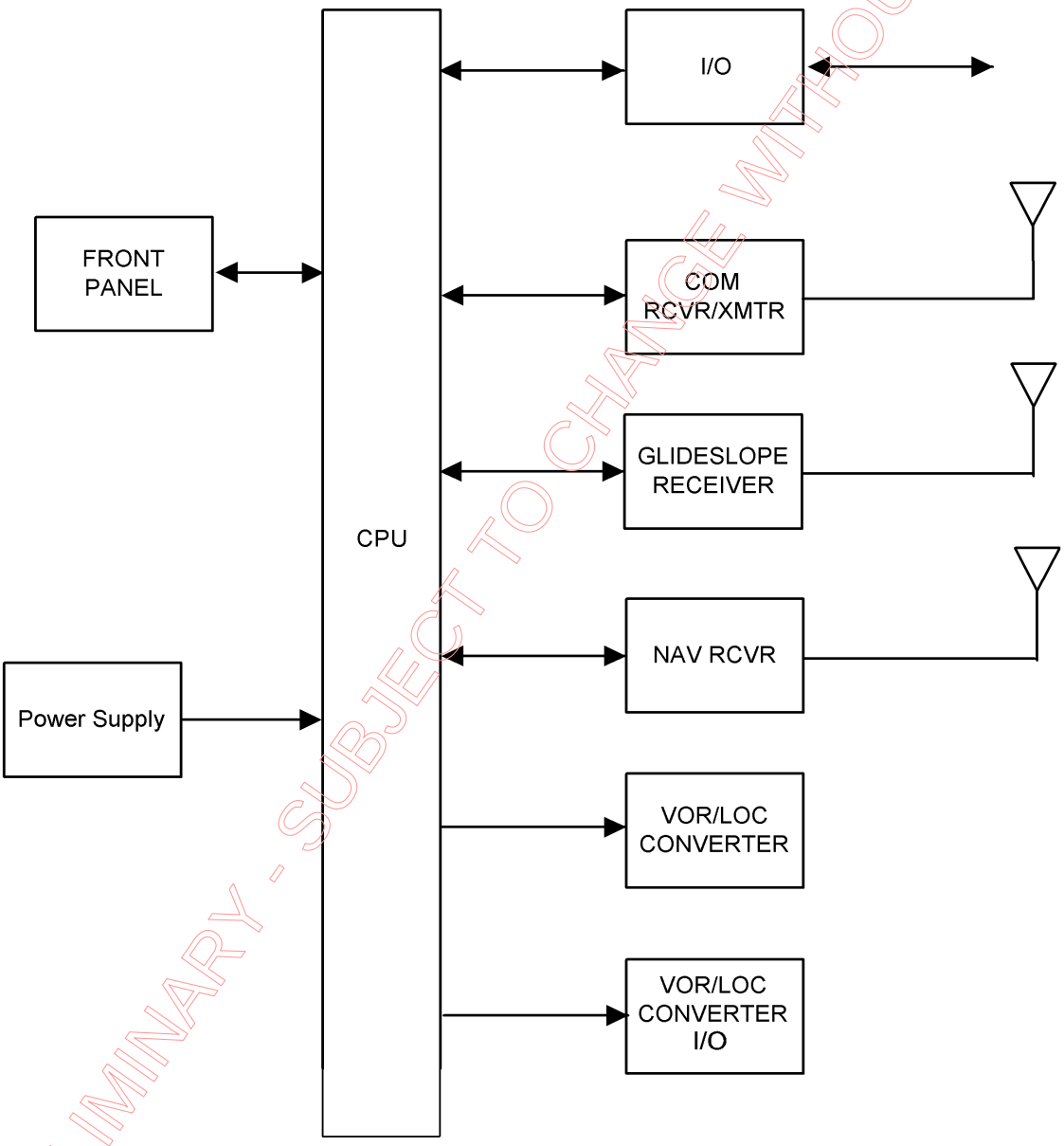

Figure 4-1 KX 165A Block Diagram

4.2.1 COM RECEIVER

Refer to figure 4-2. The front end of the Com receiver employs a dual-gate FET RF amplifier embedded in a 4-pole tracking preselector. This RF amplifier FET also provides RF AGC action. A doubly-balanced mixer converts the RF to a first IF at 21.4 MHz and is followed by a bipolar IF amplifier. In radios which use 25 kHz bandwidths exclusively, the IF amplifier is followed by six poles of crystal filtering. The IF amplifier is followed by an IF filter board in Radios which are both 25 kHz and 8.33 kHz channel capable. This IF filter board switches the IF between a six pole 25 kHz (wide) crystal filter and an 8.33 kHz (narrow) eight pole filter. Selecting wide or narrow channel tuning determines which filter is used. The filtered 21.4 MHz output is amplified by another IF amplifier transistor and passed to the inputs of an AM Receiver IC.

This IC amplifies the first IF signal, mixes it down to 450 kHz, passes the signal through an external ceramic filter before it is further amplified in the receiver IC and detected. The detected signal is used to develop IF AGC voltage and the detected signal is also output from the IC to drive audio filters and amplifiers. RF AGC voltage is derived from the IF AGC voltage. A high-side-injection first LO signal is derived from a synthesizer circuit which employs a dual-modulus Synthesizer IC, an active integrator, a loop filter and a VCO. Amplification of the VCO output is accomplished with a MMIC. In transmit the synthesizer locks up on the desired transmit frequency and a discrete bipolar amplifier is used to amplify the MMIC output to provide a drive signal to the transmitter. The 20.95MHz synthesizer reference frequency is generated by a crystal oscillator on 25kHz units, and by a TCXO on radios which are 25/8.33kHz capable. This reference frequency also serves as the second LO injection signal. The detected audio signal from the AM IC is lowpass filtered and amplified. A compressor circuit provides a relatively constant audio output level regardless of the percent of modulation of the incoming signal. Squelch action is controlled by both an audio noise detector squelch and a carrier squelch signal derived off the RF AGC. Squelching is accomplished in the audio path on the Receiver Board as well as by another squelch gate on the Main Board. On the Main Board, the audio signal passes through the Com volume control to the audio amplifier.

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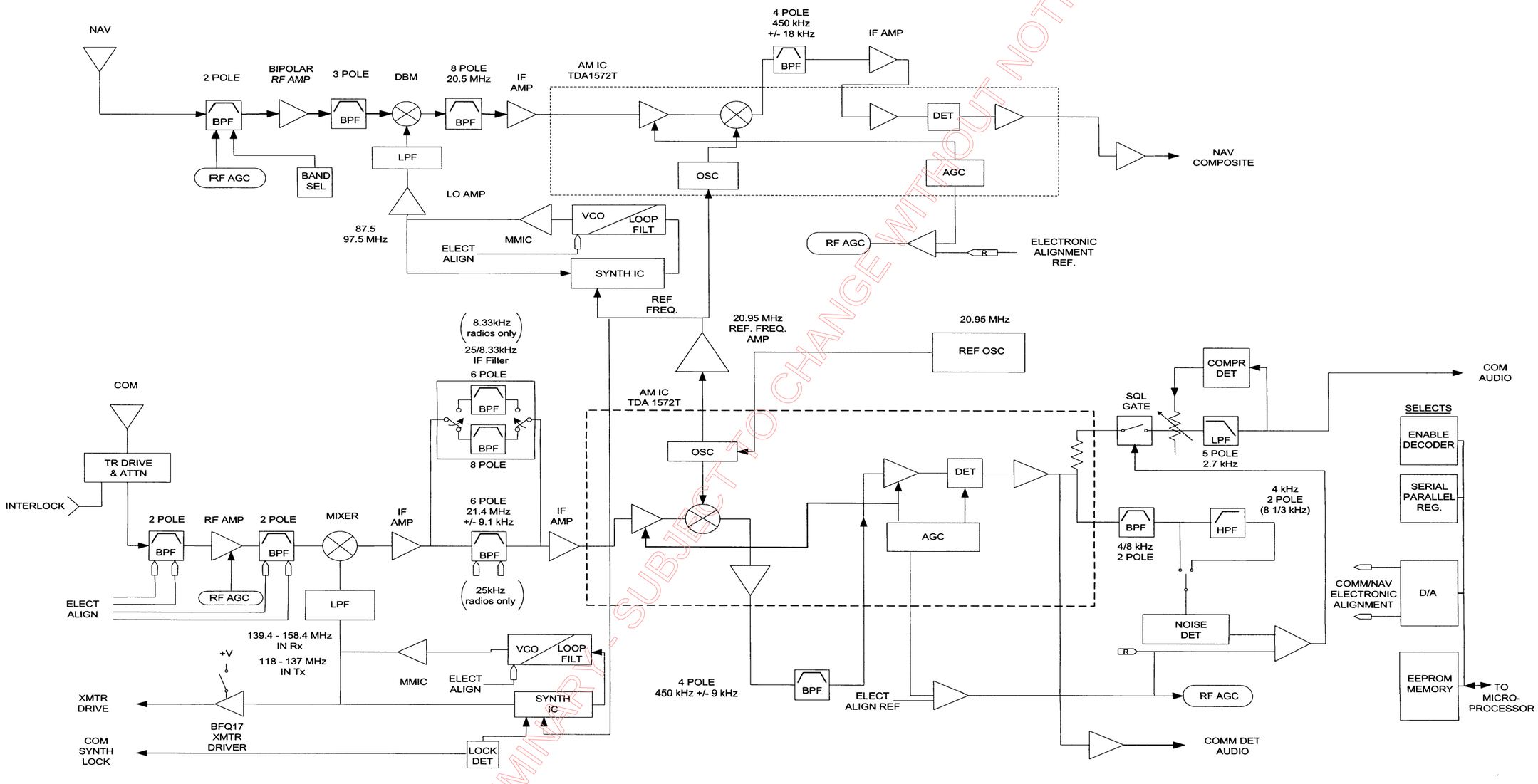

Figure 4-2 KX155A NAV/COM Receiver - Main Board Audio Circuitry

Sheet 1 of 2

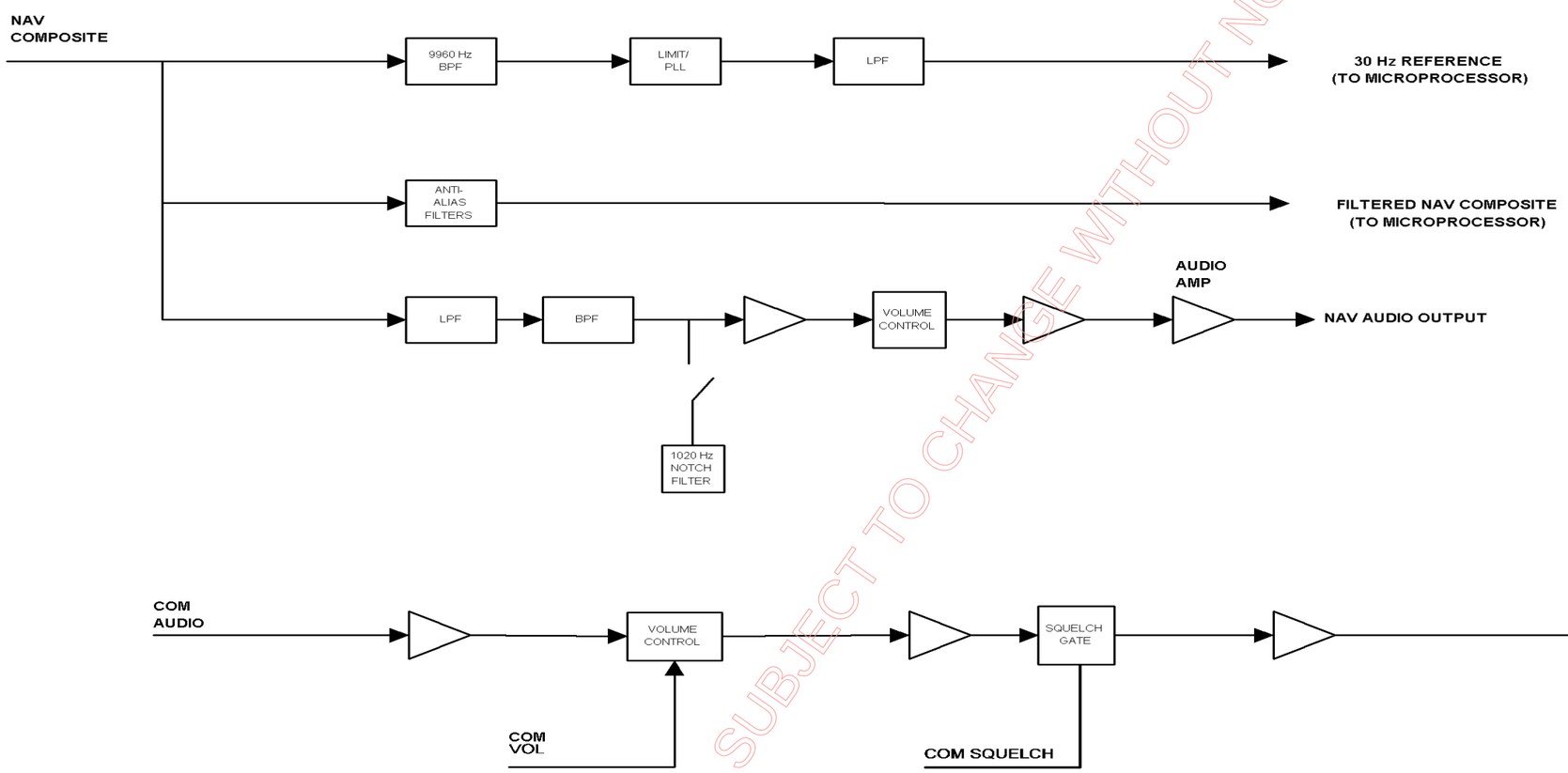

Figure 4-2 KX155A NAV/COM Receiver - Main Board Audio Circuitry

Sheet 2

4.2.2 TRANSMITTER

The transmitter produces an amplitude modulated (AM) signal within the COM BAND frequency range of 118 to 137 MHz. The output power of the signal at the COM ANT is 10 watts minimum. Refer to figure 4-3 for the following description of the transmitter.

The audio from the microphone is amplified and passed through a mic gain control which establishes the audio level used to modulate the transmitter. The mic audio signal is limited before it passes through the response amplifier which drives the modulator/power control stage that amplitude modulates the transmitter.

A buffered RF signal derived from the frequency synthesizer drives the transmitter chain. The chain consists of the predriver, driver, final amplifier, LPF and Directional Coupler. The directional coupler is used to sample the RF power. The sampled RF power is detected and buffered, then routed to the modulator/power control stage to maintain the transmitter power output. The output of the modulator/power control stage modulates the gate of the final amplifier and also drives a low level modulator which modulates the predriver.

The T/R switch is embedded within the LPF. In transmit, the receiver is isolated by a PIN diode. In receive, the PIN diode conducts the received signal to the receiver board.

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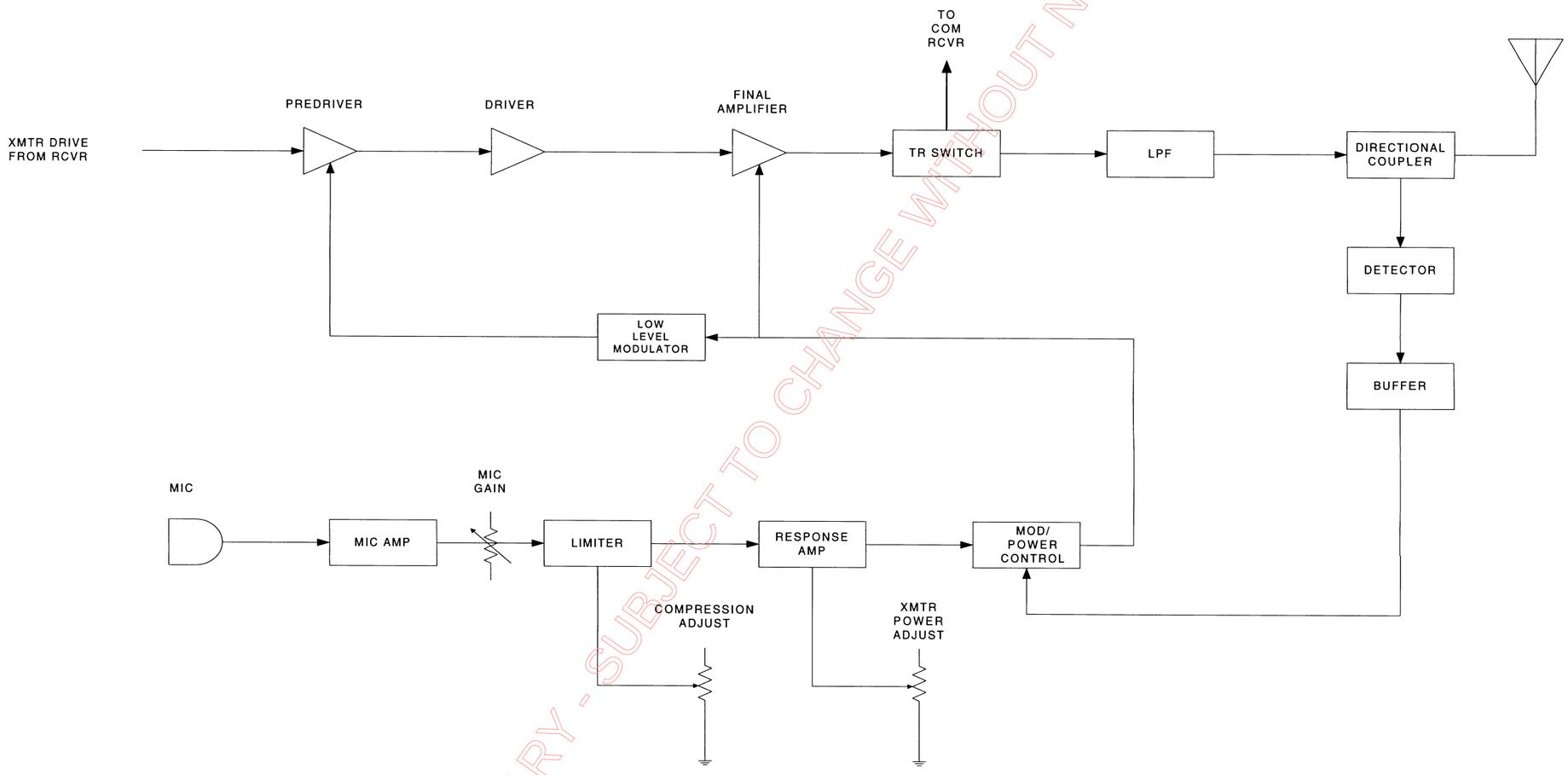

Figure 4-3 Transmitter Block Diagram

4.2.3 VOR/LOC RECEIVER

4.2.3.1 Principles of VOR system

4.2.3.1.1 General

The basic function of VOR is to provide a means to determine an aircraft's position with reference to a VOR ground station and also to follow a certain path toward or away from the station. This is accomplished by indicating whether the aircraft is on a selected VOR station radial or by determining which radial the aircraft is on. A means to differentiate between radials and identify them is therefore necessary. For this purpose, advantage is taken of the fact that the phase difference between two signals can be accurately determined. The phase difference between two signals which are generated by the VOR station is varied as the direction relative to the station changes so that a particular radial is represented by a particular phase difference. Refer to Figure 4-4. One non-directional reference signal is generated with a phase that at any instant is the same in all directions. A second signal is generated with a phase that at any instant is different in different directions. The phase of the variable phase signal is the same as the phase of the reference signal only at the 0° radial (North). As the angle measured from the 0° radial increases, the phase of the variable phase signal lags the phase of the reference signal by the number of degrees of the angle from 0°. The reference and variable phase signals, which are 30Hz voltages, are carried by RF to make radio transmission and reception possible. The VOR receiving equipment must separate the 30Hz reference and variable phase signals from the RF carrier and compare the phase of the two signals. The phase difference is indicated on a course indicator or RMI.

4.2.3.1.2 VOR generation

The VOR electromagnetic field is composed of the radiation from two ground based antennas radiating at the same carrier frequency. The first is a non-directional antenna radiating an amplitude modulated carrier. The frequency of the modulating signal varies from 9480Hz to 10440Hz back to 9480Hz 30 times per second. That is, a 9960Hz subcarrier amplitude modulates the RF carrier and is frequency modulated by 30Hz.

The second antenna appears electrically as a horizontal dipole which rotates at the rate of 30 revolutions per second. The dipole produces a figure 8 field pattern. The RF voltages within the two lobes are 180° out of phase. The RF within one of the lobes is exactly in phase with the RF radiated from the non-directional field. The rotating figure 8 pattern reinforces the non-directional pattern on the side. See Figure 4-4. This results in a cardioid field pattern which rotates at the rate of 30 revolutions per second; the rate at which the dipole antenna rotates.

The signal received by aircraft within radio range of the VOR station is an RF carrier with amplitude varying at the rate of 30Hz because of the rotation of the cardioid pattern. The carrier is also amplitude modulated at the station by the 9960Hz signal which is, in turn, frequency modulated on a sub-carrier so that it may be separated from the 30Hz variable phase signal.

4.2.3.1.3 Principles of localizer system

The localizer facility provides a visual display of the aircraft's position relative to a straight line of the runway. The ground based localizer antenna system generates two patterns. Refer to Figure 4-5. One pattern is directed toward the right side of the runway, the second to the left. The two patterns have the same carrier frequency but different audio modulating signals. The pattern to the left of the runway (in normal approach) is 90Hz, amplitude modulated, while the pattern to the right is 150Hz, amplitude modulated.

The ratio of the levels of the 90Hz to 150Hz audio, after demodulation, is dependent only upon the position of the aircraft within the patterns. The patterns are adjusted so they are of equal strength

on a vertical plane extending out from the runway centerline. When the aircraft is on this plane, the 90Hz and 150Hz voltages are equal.

4.2.3.2 NAV (VOR/LOC) Receiver

Refer to figure 4-2 for the Nav receiver description. In order to satisfy the requirements for immunity from interference caused by FM Broadcast stations, the front end of the Nav receiver employs a high-dynamic-range RF amplifier embedded in a 5-pole-band-switched preselector. The preselector also includes pin diodes to provide RF AGC action. A high-level-doubly-balanced mixer converts the incoming signal to a 20.5 MHz first IF frequency. Eight poles of crystal filtering follow the mixer. The filtered 20.5 MHz signal is amplified by a first IF amplifier transistor then is applied to the input of an AM Receiver IC. This IC amplifies the first IF signal, mixes it down to 450 kHz, passes the signal through an external ceramic filter and JFET amplifier, then further amplifies the signal at 450 kHz and finally detects the signal. The detected signal is used to develop IF AGC voltage and the detected signal is also output from the IC to drive audio filters and amplifiers. RF AGC voltage is derived from the IF AGC voltage. The low-side-injection first LO signal is derived from a synthesizer circuit which employs a dual-modulus Synthesizer IC, an active integrator, a loop filter and a VCO. Amplification of the VCO output is accomplished with both a MMIC and a discrete bipolar amplifier. The synthesizer reference frequency of 20.95 MHz is taken from the Com section of the receiver board. This reference frequency also serves as the second LO injection signal. The detected signal is applied to a buffer-amplifier without any audio filtering to provide the VOR/LOC composite signal to the Main Board. On the Main Board the Nav composite signal then splits into three paths: 1) 30 Hz reference, 2) anti-alias filters, and 3) Nav audio.

For the 30 Hz reference, the Nav composite passes through a 9960 Hz bandpass filter and a limiter stage before going to the phase locked loop (PLL) FM demodulator. The PLL extracts the 30 Hz reference modulation from the composite signal so it can be passed to the microprocessor.

The anti-alias filters are low pass filters that filter the composite signal before it is passed to the microprocessor for signal processing used in the converter function.

The Nav composite signal also passes through a low pass filter to strip off the 9960 Hz sub-carrier leaving the 30 Hz “variable” signal. The resultant audio signal passes through a bandpass filter that establishes the frequency response of the signal. The signal passes through a front panel selectable ident filter before being routed to amplifier stages, volume control, and finally the audio amplifier.

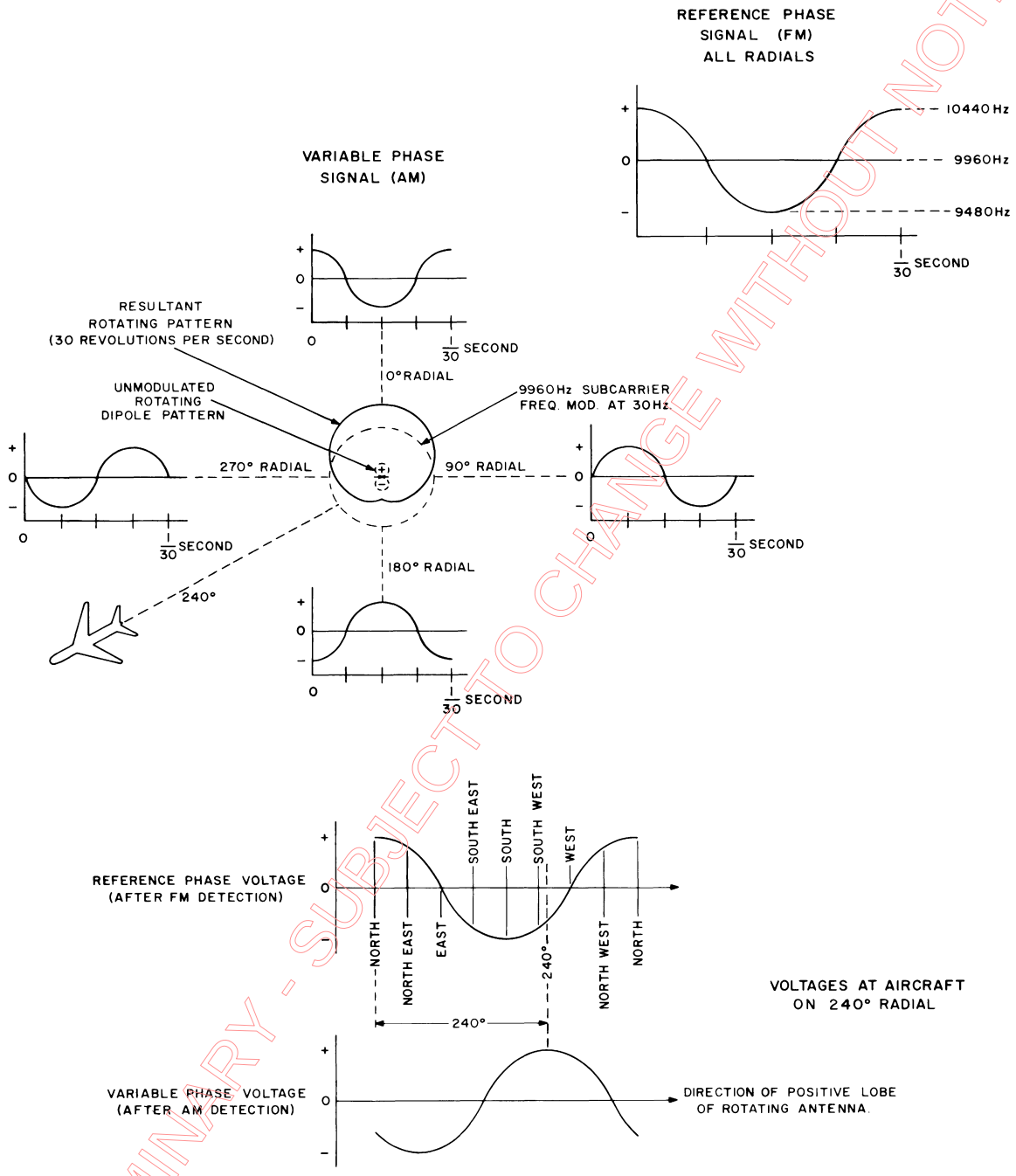

Figure 4-4 VOR Signal Generation

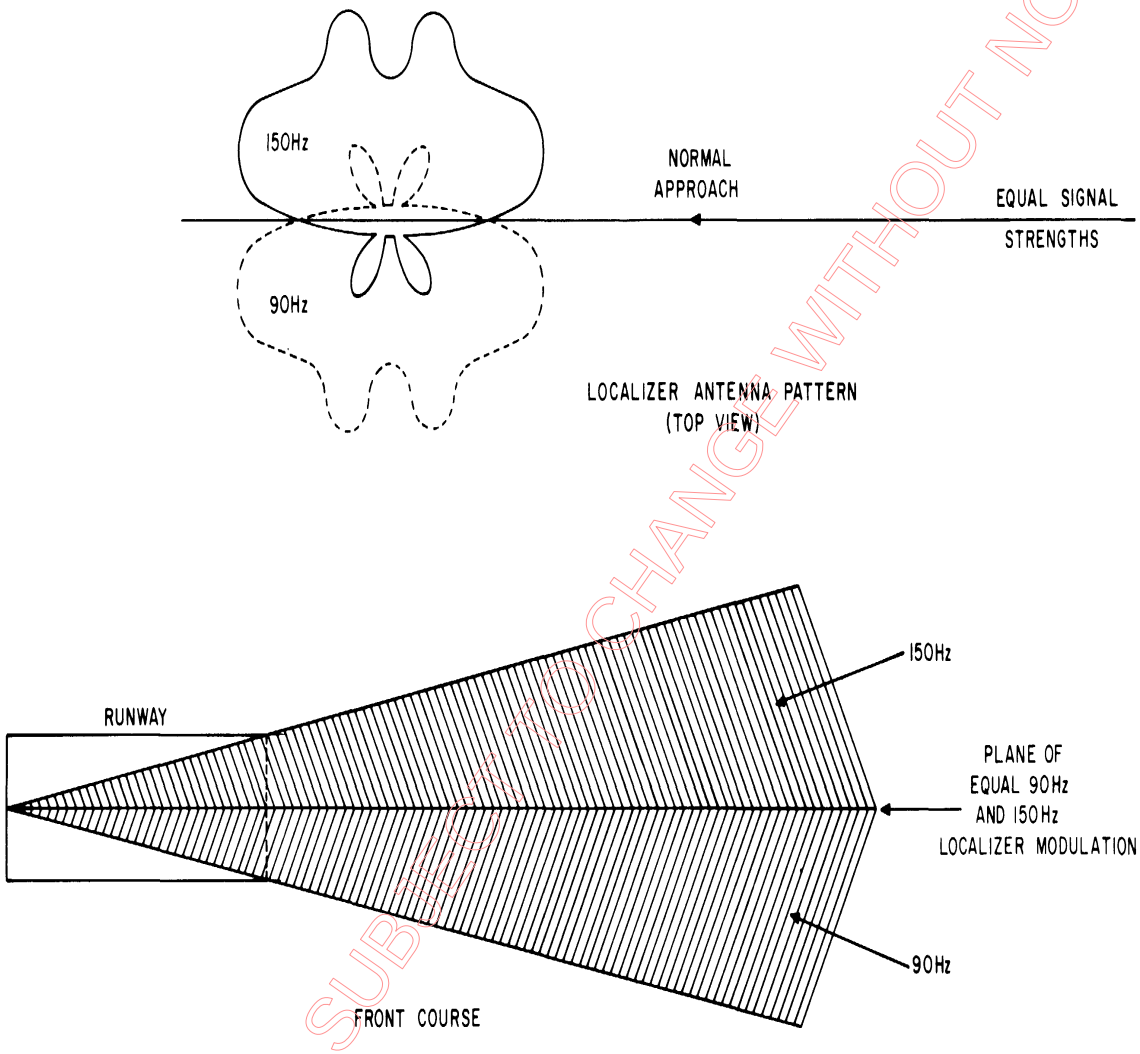

Figure 4-5 Localizer Signal Generation

4.2.4 GLIDESLOPE RECEIVER

4.2.4.1 Principles of glideslope system

The glideslope signal is radiated by a directional antenna array located near the approach end of the runway. The signal consists of two intersecting lobes of RF energy. The upper lobe contains 90Hz modulation and the lower lobe contains 150 Hz modulation. The equal tone amplitude intersection of these two lobes forms the glide path. A typical glide angle is 2.5 degrees. If the aircraft is on the glide path, equal amplitudes of both tones will be received and the deviation bar will be centered. If the aircraft is above the glide path, 90 Hz modulation predominates and the visual display is displaced downward. If below the glide path, 150 Hz predominates and the display is displaced upward.

4.2.4.1.1 GS Receiver 200-09447-0000

Refer to the Figure 4-7 for a block diagram of Glideslope Receiver board 200-09447-0000.

The Glideslope Board contains a receiver that may be tuned throughout the Glideslope frequency band of 329.15 to 335.00 MHz. The Glideslope operation frequency is paired with a selected Localizer frequency. Therefore, Glideslope operating frequency is not viewed/selected directly from the front panel. The radio selects the proper Glideslope frequency based upon the Localizer channel.

Digital and analog I/O comes from the VHF Main Board via a 12 pin ribbon cable. The receiver gets its synthesizer tuning, and DC power from the VHF Main board. The RF Input comes in externally through the antenna connection on the back of the radio. There is a rear edge card connector that is used to output analog converter signals necessary to drive an external indicator.

The RF signal coming from the antenna connector passes through a dual gate FET VGA (variable gain amplifier) and a fixed gain MMIC amplifier. This amplified signal is the RF input to a mixer with a LO 30 kHz below the RF and an IF of 30 kHz. The IF Filter and Amplifiers consist of three fixed gain IF amplifiers, one IF VGA amplifier, and a 50 kHz 9-pole low pass filter. The 30 kHz IF is passed through an AM detector resulting in an AC audio composite and a DC level. The AC composite audio signal contains the 90 and 150 Hz tones needed to produce an up/down indication on an aircraft's indicator. The DC level is used by the IF and RF AGC amplifiers to maintain a constant Detector input power.

The audio composite is digitally processed on the main board to determine the level of Glideslope external indicator deflection and flag level. These values are sent from the Main Board to the Glideslope Receiver board via the serial data buss. A quad digital potentiometer receives the serial data. One digital potentiometer controls the flag level. Two other digital potentiometers control the Glideslope indicator deflection. An IF AGC signal is also sent back to the VHF main board for use in automatic test and for automatic detection of the presence of the 200-09447-0000 Glideslope Board. The IF AGC voltage is also available at the rear edge card connector for automatic test use.

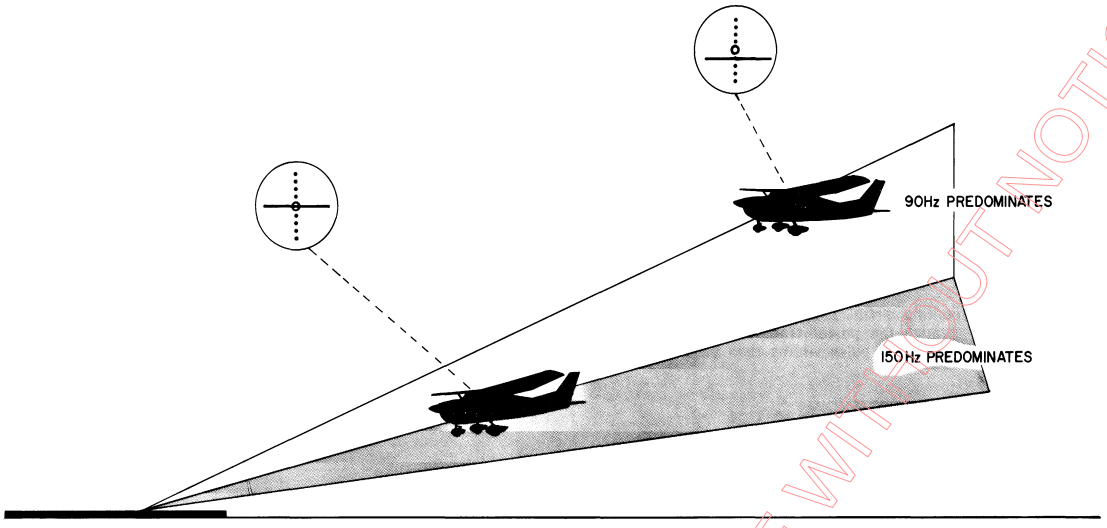

Figure 4-6 Glideslope

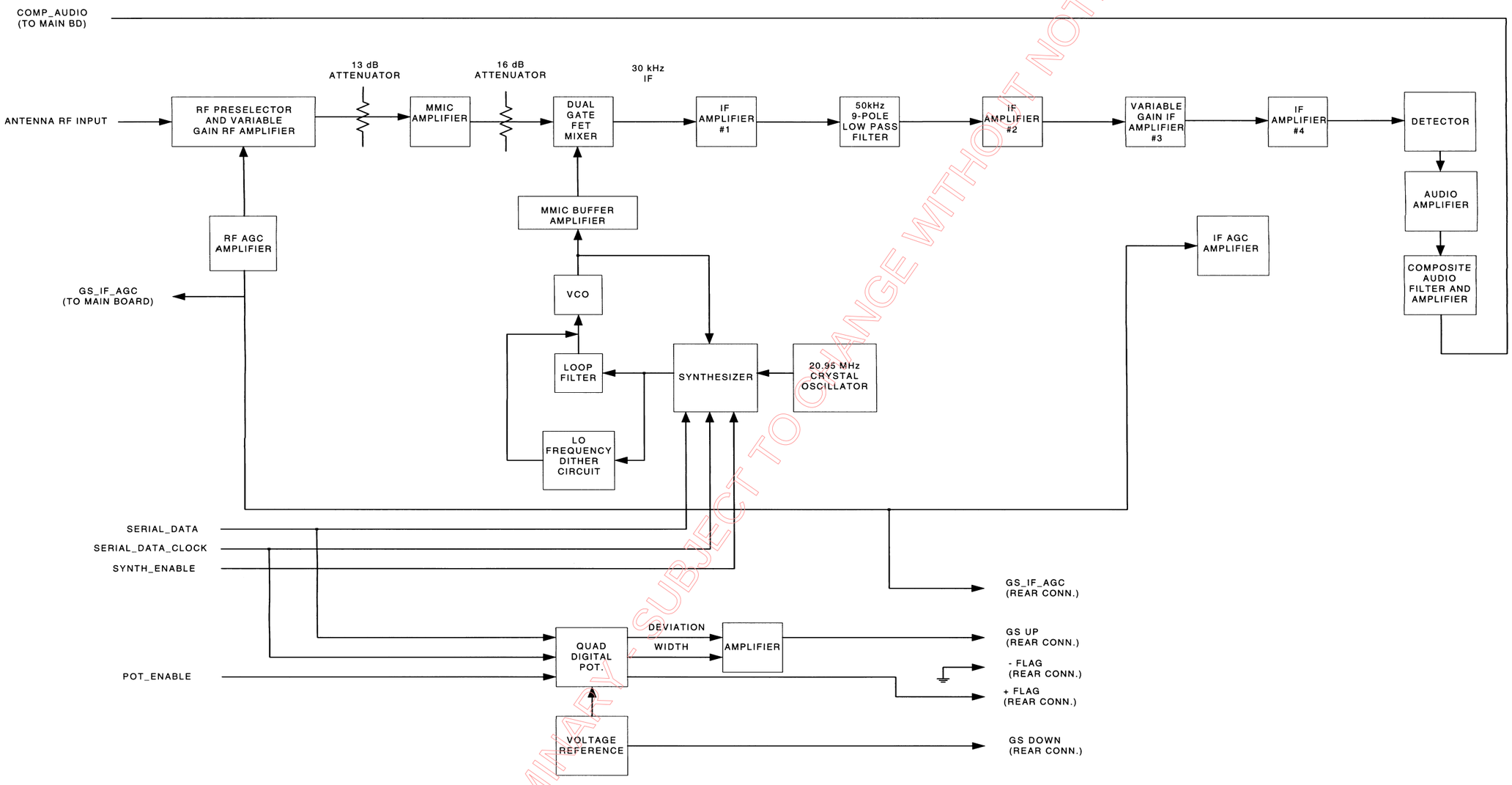

Figure 4-7 200-09447-000 KX 165A
Glideslope Receiver Block Diagram

4.2.5 CENTRAL PROCESSING UNIT (CPU)

The CPU controls the function of the unit and its connections can be seen in figure 4-8. An external crystal sets the clock frequency for the CPU. The CPU also communicates to a RS-232 IC that converts the CPU levels to those that are RS-232 compatible. An electronically erasable programmable read-only-memory device (EEPROM) is used to store alignment information and other configuration data. The flash memory is used to store the unit software and the static random access memory (SRAM) is used to supplement CPU memory. DME I/O conditions signals from the CPU so they can be used to channel external DME equipment. Discrete I/O pass through filter networks and switch transistors are then routed to the CPU for control purposes. A voltage monitor on the 5V controls the reset line to the microprocessor, when the voltage on the 5V line is below 4.75 VDC the CPU is held in the reset state.

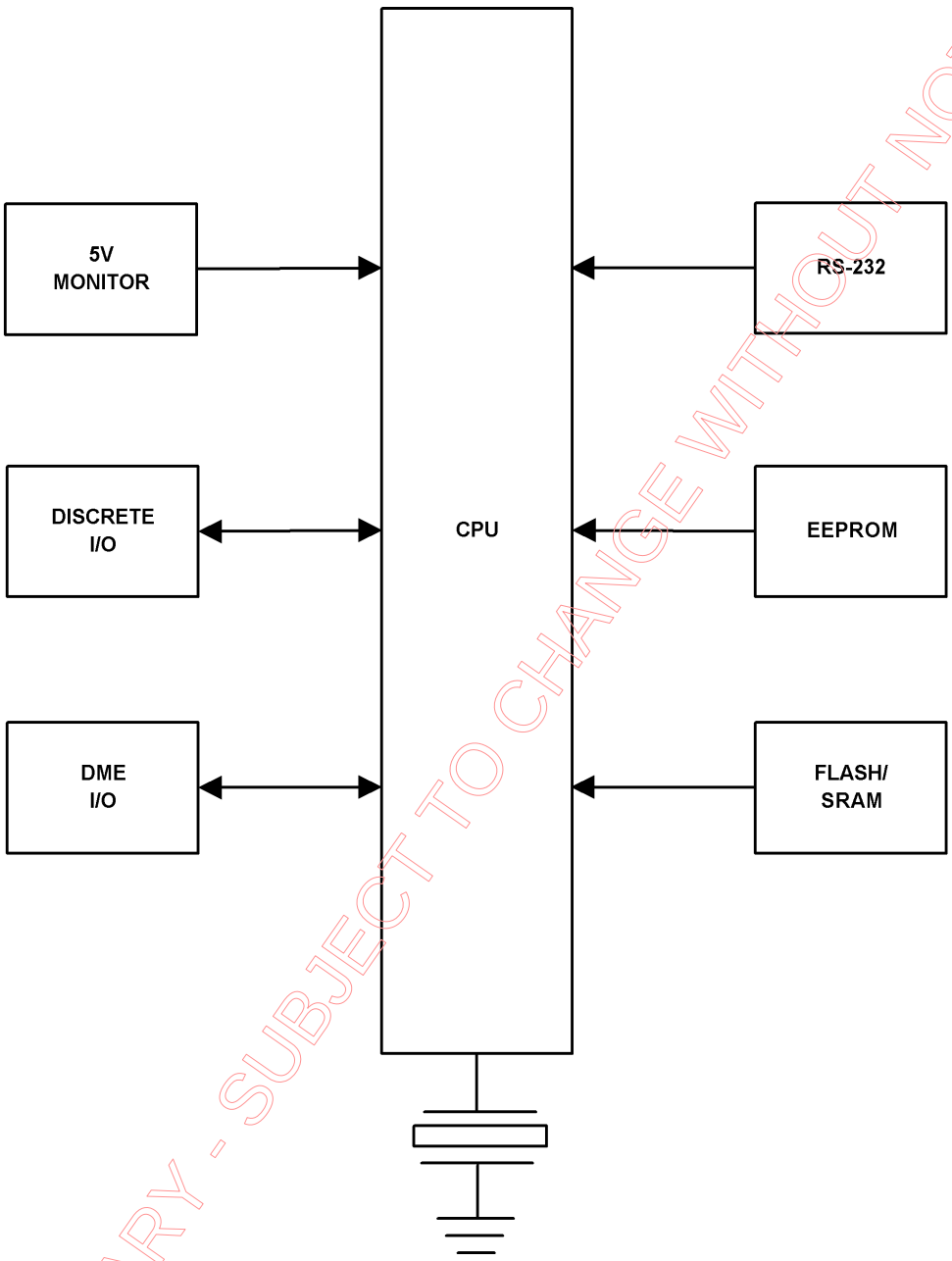

Figure 4-8 CPU Block Diagram

4.2.6 POWER SUPPLY

Refer to figure 4-9 for the power supply block diagram. The unit uses a switching power supply to generate voltages that supply the various electrical functions. The power supply converts 11-33 VDC to 5 VDC, 9VDC, -12VDC, and -200 VDC. Refer to the power supply block diagram located in figure 4-9. The 11-33 VDC aircraft bus is filtered via a hash filter. The output of the hash filter goes to the transmitter and to the transformer. A switch connected to the transformer chops the input voltage so the transformer can convert the input dc voltage to the several different voltages. Each voltage output from the transformer requires a rectifier diode and filter capacitor to complete the conversion to dc voltages. The -200 VDC line also has a post regulator in order to accurately control the voltage that droves the display module. The output of the 9 VDC line is fed back to the regulator IC which keeps the output voltages constant over varying loads. Before the switching regulator stabilizes, a pre-regulator from the aircraft bus is used to supply power to the regulator IC.

4.2.7 FRONT PANEL AND DISPLAY

The front panel display block diagram can be seen in figure 4-10. The Front Panel and Display Module contain the display interface, knobs and buttons for pilot to enter data. The display interface should receive signals from the main board and drive the gas discharge display. The knobs and buttons' data will be sent to the microprocessor on the main board.

The front panel module has two dual concentric INC/DEC optical encoder switches with one pull switch each, four push-button switches, two volume control pots with pull switches and one of the volume controls has a rotary power on/off switch. The front panel buttons and switches are read by periodically latching the state of the switches into the two parallel-to-serial converters/shift registers and shifting the data into the processor on the main board. The optointerrupter INC/DEC switches consist of an IR LED and a phototransistor in a single package. In order for the IR light to be detected by the phototransistor a metallic surface with alternating reflective and non-reflecting surfaces is rotated in front of the photointerrupters.

The unit display is a segmented gas discharge display that is formatted as 24 cathode and 20 anode buses. Each segment can be addressed by one combination of cathode and anode driver line. The display is run by cycling through the cathode bus one at a time and turning on the appropriate anodes. The display is updated by first sending the anode driver data and latching the data into anode driver output latch. Then the cathode data stream is sent to the cathode driver and then the DISPLAY ENABLE line is toggled. The cathode driver outputs are activated and the display lights. This process is repeated for all 24 of the cathode buses on the display to complete one full cycle of updating the display. The frame update rate of the display is approximately 70 Hz.

The front panel contains the potentiometers for the nav and com audio volume controls. The voltage on the wipers of the potentiometers are read by the A to D converters on the main board processor which in turn control the volume by setting the digital pots on the main board.

The photocell is a variable resistor in which the resistance is dependent on the amount of light incident to the photocell. When biased in a voltage divider configuration with another resistor the A to D converter on the main board can read the changing voltage and change the intensity of the display drive to track the existing light conditions.

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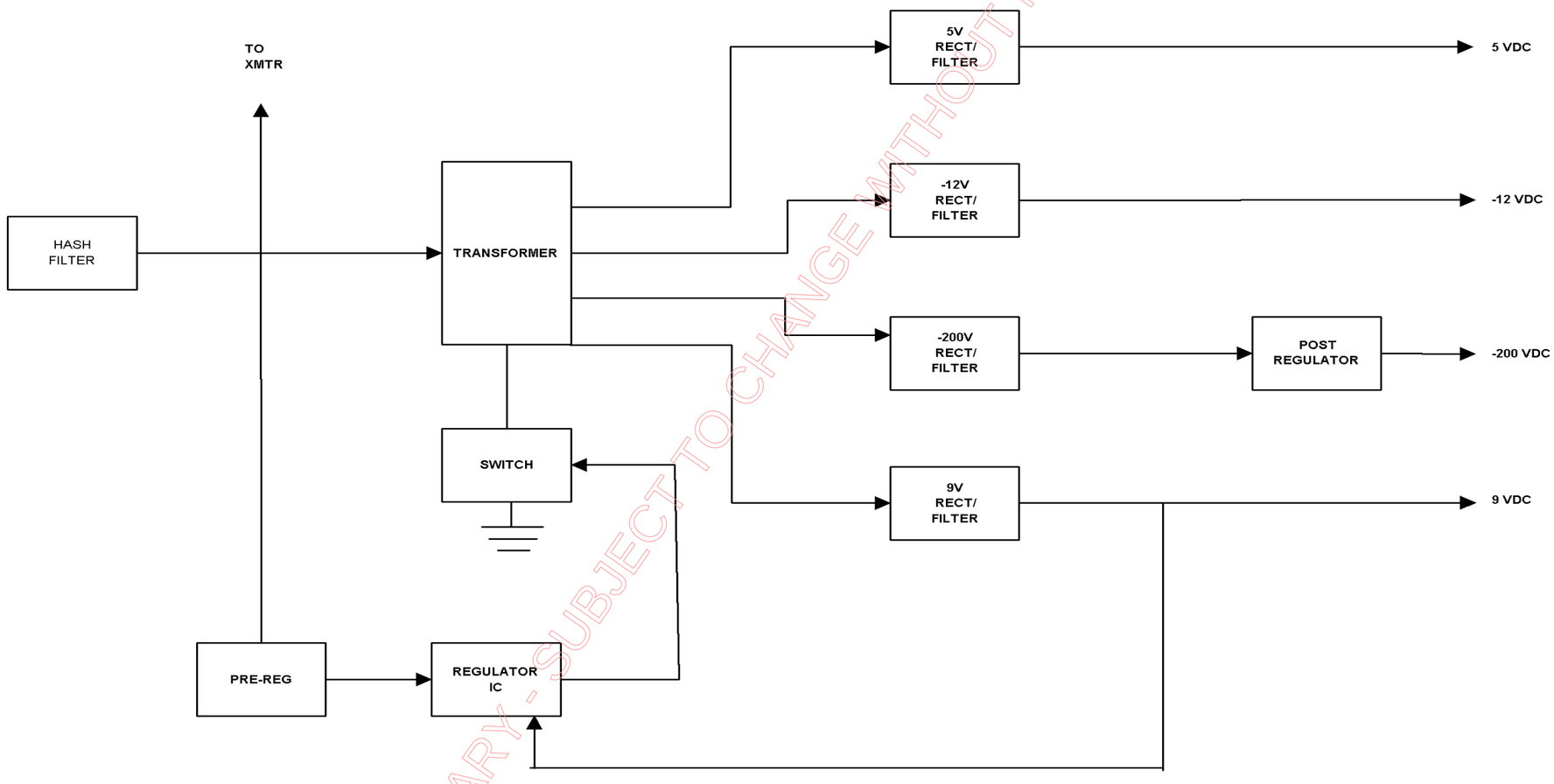

Figure 4-9 Power Supply Block Diagram

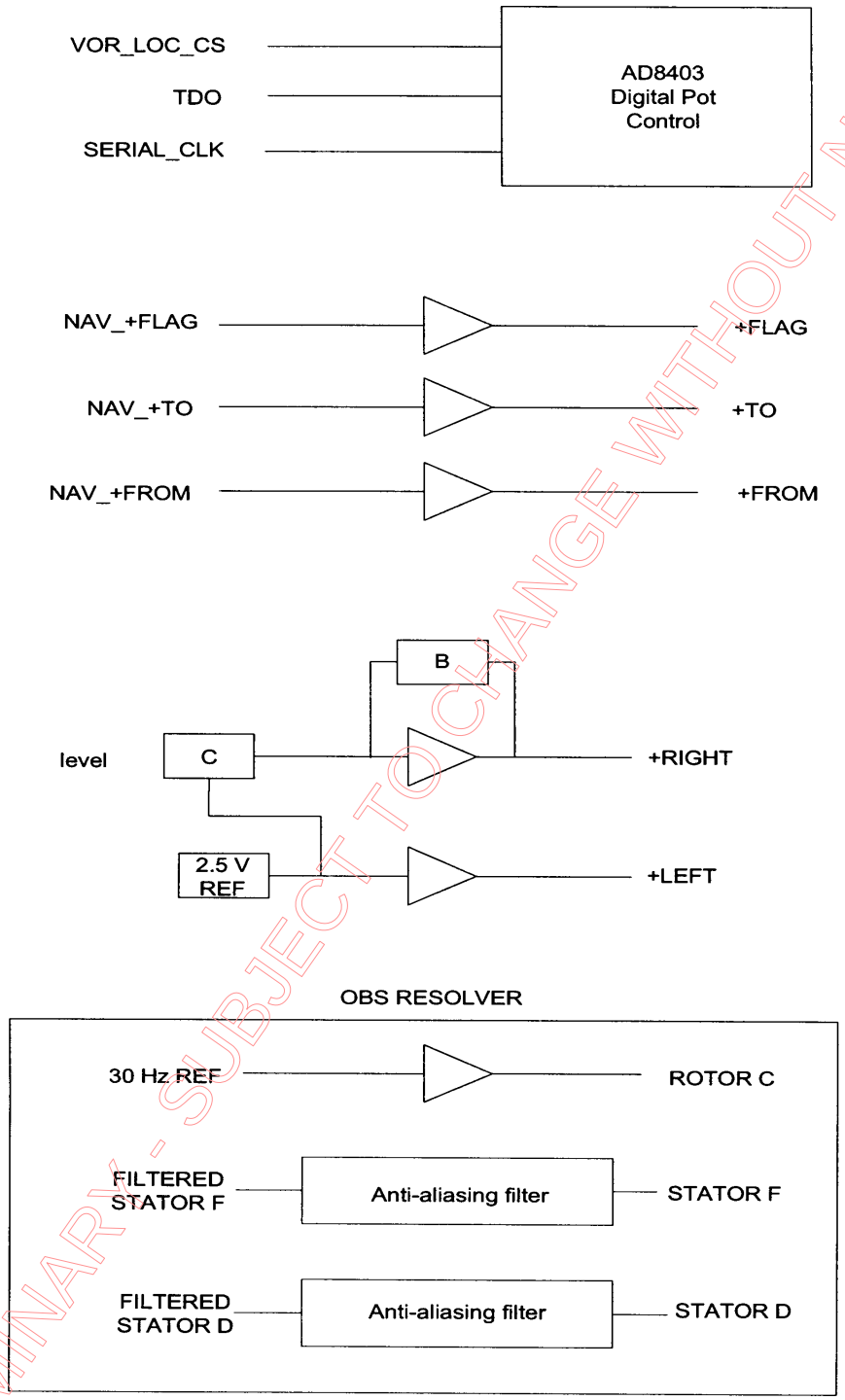

Figure 4-11 VOR/LOC Converter Board Block Diagram

4.2.8 VOR/LOC Converter Board

Refer to Figure 4-11. The VOR/LOC converter I/O board generates the analog signals needed to interface to an indicator with OBS. External system outputs from the board are TO/FROM flag drive, Warning Flag drive, D-Bar drive, and Reference Stator drive for Indicator OBS resolver. External system inputs to the board are return Stator signals from the OBS resolver.

Discrete logic level signals from the Main board control each of the flag driver circuits. Digitally programmable Potentiometer C controls the D-Bar centering. A 5V reference is resistively divided to produce a input voltage to the +RIGHT drive amplifier. The Input to the +Left drive amplifier is one half the 5V reference. The Gain or slope of the D-Bar output is set by digitally programmable potentiometer B. The serial control of these potentiometers come from the Main Board. A Buffer amplifier isolates the recovered 30 Hz VOR Reference from the Main board signal and outputs it to the external indicator OBS. The returning OBS stator signals are filters on the board and returned to the Main Board. Here they are sampled and used for OBS position calculations.

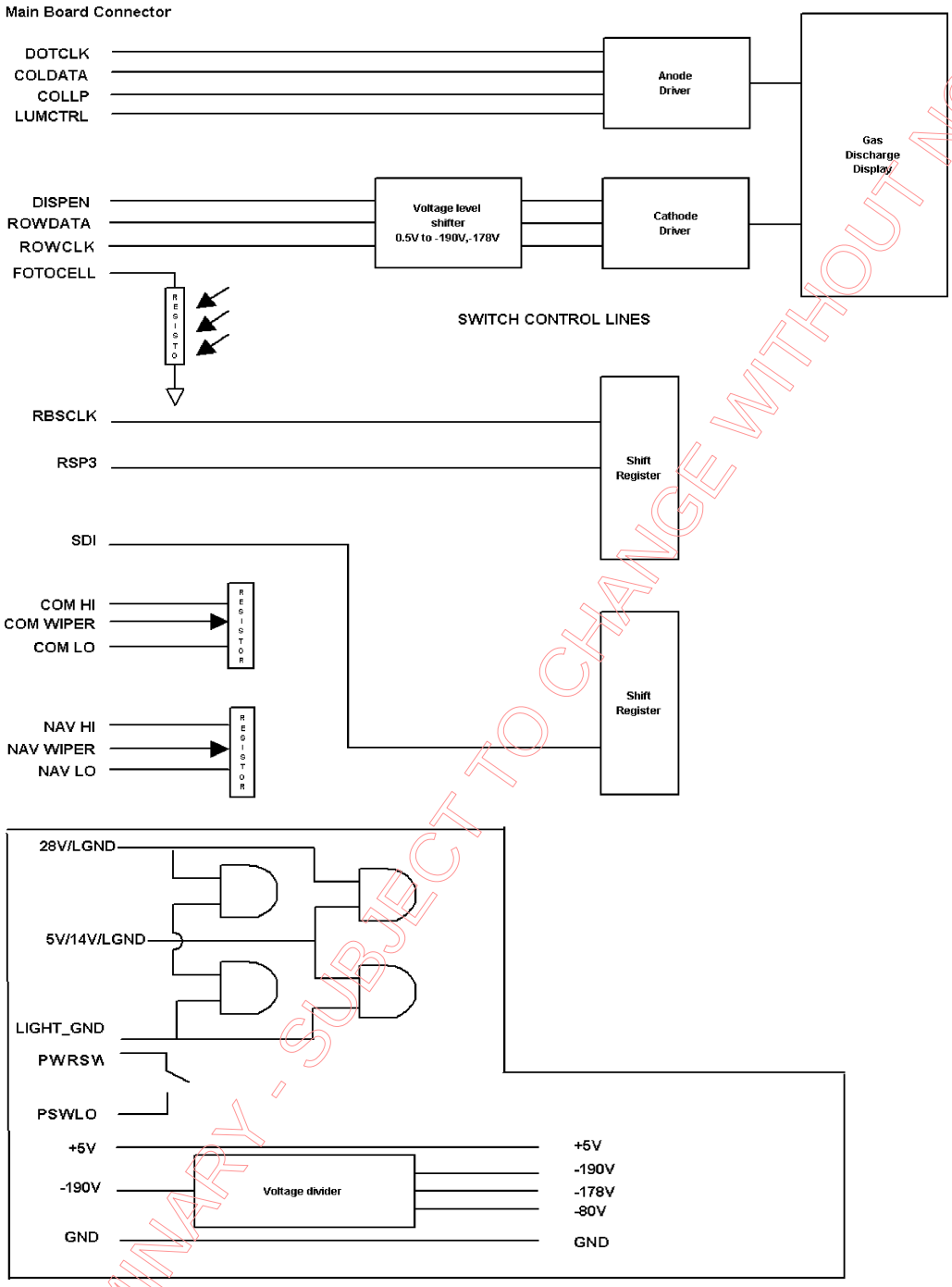

Figure 4-11 Front Panel and Display Diagram

4.3 DETAILED CIRCUIT THEORY

The detailed circuit theory description is broken into the following functions:

1. Com receiver/IF board
2. Transmitter
3. Nav (VOR/LOC) receiver
4. Glideslope receiver
5. Audio board
6. CPU
7. Power supply
8. VOR/LOC Converter I/O Board

These functions may involve more than one assembly; therefore, component designators will point to the assembly on which the parts are found. For example, R1 is on the glideslope reference oscillator, and C1001 is found on the main board.

Table 4-1 Component Designators

1000	Main
2000	Bezel (front panel)
3000	NAV/COM Receiver
4000	Transmitter
5000	Not used
6000	Audio
7000	VOR/LOC Converter I/O Board

4.3.1 COM RECEIVER

4.3.1.1 Digital/Analog Interface Circuitry

Clock, Data and Enable signals generated by the microprocessor on the Main board are used to program the following sections of the receiver:

- Synthesizers for the two receivers (U3011 and U3018)
- Two digital to analog converters (DACs) for alignment functions (U3005 and U3006)
- A serial to parallel register for controlling various modes of the receivers (U3002)
- An EEPROM which stores alignment values for the receiver (U3007)

The enable decoder, U3003, determines which of the devices above read the serial data being sent by the microprocessor. A high on the outputs of U3003 enables that respective device. Select 1, Select 2, Select 3 and Enable lines from the microprocessor control U3003.

4.3.1.2 Digital to Analog Converters

Digital to analog converter (DAC) U3005 drives the varactor tuned Com preselectors as well as provides alignment voltages to the unit's master reference oscillator and sets the threshold of the Com squelch. Another DAC, U3006, provides the alignment voltages for the Com IF filter adjustments, the Com and the Nav RF AGC activation levels as well as the Com and the Nav VCO adjustments. A precision regulator, U3027, provides the DACs with a stable 8.4 VDC supply voltage.

4.3.1.3 Serial to Parallel Register

The outputs of the serial to parallel register, U3002, controls four functions. When the volume control knob is pulled out by the pilot, driving U3005 pin 2 from its normally low state to a high, the squelch can be manually forced open. The Nav RF preselector is controlled by U3005 pin 2, which will be high if the Nav operating frequency is below 113.6 MHz, and will be low at frequencies of 113.6 MHz and above. When U3002 pin 3 is high, the Com receiver audio level compressor is disabled, a feature that may be used during some bench tests.

4.3.1.4 EEPROM

The non-volatile EEPROM, U3007, stores the alignment information for each receiver board. This EEPROM is read by the microprocessor when the unit is first turned on. The values in U3007 are updated when the technician adjusts any of the alignment functions controlled by U3005 and U3006.

4.3.1.5 Voltage Regulator and T/R Inverters

Voltage Regulator and T/R Inverters

Voltage regulator U3009 provides a stable voltage for sensitive synthesizer circuitry.

The microprocessor sends transmit-receive commands to the receiver board via P3001 pin 2. This pin is high when the unit is in transmit. TX switch driver U3001-G, pin 10 is low in transmit and high in receive. The output of inverter U3001-B is high in transmit and low in receive.

4.3.1.6 T/R Switch Drive and Interlock Attenuator

Received signals arrive at Receiver board J3006 from the T/R switch located on the Transmitter board. When Q3004 is turned on, a positive voltage appears at the center conductor of J3006 to turn on the T/R diode located on the transmitter board. In transmit, a negative voltage is developed at the center conductor of J3006 by a small amount of rectification in the T/R diode itself, holding the T/R diode off.

CR3004 and CR3005 form a 14 dB attenuator which is activated in transmit or when the unit's interlock feature is enabled externally. Q3001, Q3002 and Q3003 drive the attenuator active when the collectors of Q3002 and Q3003 are at a positive voltage. A negative voltage at the collectors of Q3002 and Q3003 allows the incoming signal to pass through the attenuator with little attenuation.

4.3.1.7 Preselector and RF Amp

L3006 and L3007 are part of the varactor tuned Com preselector, which feeds RF Amp Q3010. The gain of Q3010 is maximum when its gate 2 is above 7 volts. At signals stronger than about -85 dBm at the receivers input, the voltage on gate 2 will drop, reducing the gain of Q3010, providing RF AGC action. Q3010's output is fed to two more varactor tuned preselector poles consisting of L3009 and L3011. The voltage on the varactors CR3006-CR3009 will vary from about 4 VDC at 118.0 MHz to about 7.0 V at 136.9 MHz. In transmit, the preselector poles are detuned to reduce the overloading of the receiver.

4.3.1.8 First Mixer and First IF

A doubly-balanced mixer, U3028, converts the incoming signal to the 21.4 MHz first IF frequency. The first local oscillator signal is applied to pin 6 of the mixer. The First IF amplifier Q3011 amplifies the 21.4 MHz signal and feeds it to either the first IF filter FL3001 or the IF Filter board. On radios which are 25/8.33kHz capable the IF Filter board is installed. It switches between an eight pole narrow bandwidth crystal filter or a six pole wide bandwidth crystal filter depending on the radio being tuned to a wide (25kHz) or narrow (8.33kHz) channel. Radios which use 25kHz bandwidths exclusively use FL3001 and the IF Filter board is not installed. The filtered 21.4MHz IF signal is amplified by IF amp Q3017 before being passed to pin 18 of U3015, an AM receiver IC.

4.3.1.9 AM Receiver IC and Second IF

U3015, includes an additional gain controlled 21.4 MHz amplifier, a second mixer, amplification at 450 kHz, a detector and AGC circuitry. The 21.4 MHz signal applied to U3015 pin 18 is amplified then mixed down to 450 kHz, the second IF frequency. The 20.95 MHz reference oscillator is applied to U3015 pin 16 to serve as the second LO.

The 450 kHz second IF signal output at pin 1 of U3015 is impedance matched by L3015 and C3066 to FL3006, a 450 kHz ceramic filter. The filtered signal is then returned to U3015 at pin 3, amplified within the IC, then passed to an internal detector. The gain of both the 21.4 MHz and 450 kHz amplifiers internal to U3015 is controlled by the AGC voltage on pin 7. AGC time constants are established by C3120 and C3134. The amplified 450 kHz signal is available at pin 12 of U3015 (TP3005) to allow easy viewing of the signal with an oscilloscope.

4.3.1.10 Reference Oscillator

In 25kHz radios a 20.95 reference frequency oscillator consisting of Y3002 and Q3022 generates a stable reference frequency to be utilized by the synthesizers. Varactor CR3013 circuitry provides a variable capacitance to fine tune the frequency of Y3002. Units that are both 25kHz and 8.33kHz channel capable have Y3001 installed. This is temperature compensated oscillator used so that the radio remains in specification despite the narrower bandwidths of 8.33kHz channels. This reference frequency is buffered by Q3021 and fed to U3015 to serve as the second local oscillator for U3015. U3015 also outputs the 20.95 MHz signal on pin 14. Q3023 amplifies and buffers this 20.95 MHz reference signal for distribution to other receiver circuits.

4.3.1.11 Com Audio and Receiver Compressor

Detected Com audio from U3015 pin 6 is sent to buffer transistor Q3025 to provide an unsquelched-constant-level output to the unit's rear connector for use by external equipment. U3015 also outputs detected audio on pin 9, which is routed through R3180 then to compressor FET, Q3024. The purpose of the receive audio compressor is to hold the audio level the pilot hears at a nearly constant level regardless of the percent of modulation of the received signal. CR3015 is a clipper that limits the level of noise and transients.

If squelch gate Q3016 is turned on, the signal is fed through to the Audio LPF which amplifies the signals below 2.7 kHz and attenuates higher frequencies. U3008-B and U3008-A stages both have a gain of about 3. Audio out of U3008-A is fed to the Main board via P3002 pin 1 and also the compressor amp, U3008-C. The compressor amp inverts the signal and then feeds it to the compressor detector consisting of CR3017 and C3151. If the incoming signal has a modulation percentage of less than about 20%, the voltage at the gate of Q3024 is high enough to hold Q3024 off, letting the audio signal pass unattenuated to the audio LPF. On signals that are modulated at greater than about 20%, the detected voltage across C3151 will drop enough to turn on Q3024. Q3024 then acts as a variable resistor, attenuating the detected signal out of U3015 as necessary to hold the audio output at a constant level. For testing purposes it may be desirable to disable

the compressor; this is accomplished by Q3005. When the input to Q3005 is driven high by the microprocessor via U3002, the compressor is disabled.

Com receiver audio is output from the receiver board via J1002 pin 1. The signal routes to U1023C on the main board which has a gain of about 0.5. The signal goes to U1029A which has a gain of about 2.5, and then is directed to digital pots U1028A&D which control volume. After the volume control, the audio signal is fed to U1029, an amplifier circuit that has a gain of about 0.3, and then to U1027B which has a gain of about 35. T1001 transforms the signal in order to drive a 500 ohm load.

The com receiver audio is squelched when the gates of Q1024 and Q1029 are pulled high.

4.3.1.12 Noise Squelch

Detected Com audio from U3015 pin 6 is applied to the squelch noise bandpass filter U3013-D. Squelch operation differs depending on whether the unit is tuned to a 25kHz or a 8.33kHz channel.

When tuned to a 25kHz channel U3010-C, U3017-C and Q3018 are off, and U3010-D is on. this sets the BPF U3013-D to a center frequency of 8kHz and routes the output directly to the noise detector CR3016. When no desired signal is present the amount of 8kHz noise will be high, charging C3152 up to about 2.5Vdc and exceeding the threshold on pin 9 of squelch comparator U3013C. This allows audio to pass by turning on Q3016 through inverted transistor Q3007. When a desired signal is present the 8kHz noise will drop, and allow Q3016 to turn on and pass audio to the audio LPF U3008-B.

When tuned to an 8.33kHz channel Q3018 is turned on which shifts the center frequency of BPF U3013-D to approximately 4kHz. Because of this the 8.33kHz squelch operates off of 4kHz noise. The output of the BPF is switched to the HPF U3013-A so as to eliminate possible squelch action on desired audio tones. The output of the HPF is routed to the noise detector and the squelch comparator. U3017-C is used to lower the hysteresis of the squelch comparator while on an 8.33kHz channel.

4.3.1.13 RF AGC and Carrier Squelch

The AM receiver IC, U3015, outputs an IF AGC voltage on pin 7. This voltage will be about 1 VDC with no input signal to the unit and rise to about 2 VDC with a strong input signal. U3018-D is used to monitor the IF AGC voltage, and when it reaches about 1.6 VDC, turns Q9 on, pulling the Com RF AGC voltage down below 8VDC. The reduced level of RF AGC voltage reduces the gain of RF amp Q10 to prevent the following stages from being overloaded.

As the IF AGC voltage out of U3015 increases above about 1.5V, the output of the carrier-squelch comparator U3013-B goes positive. This positive voltage is directed to the input of squelch comparator, U3013-C, to force the squelch to open on strong signals.

This carrier squelch (or backup squelch) is required when receiving signals that might contain a strong 8 kHz modulation component which would prevent the noise squelch circuitry from opening the squelch.

4.3.1.14 Com Synthesizer and TX Driver

Serial data from the microprocessor is sent to program the synthesizer IC, U3011. U3011 compares VCO output on pin 8 with the 20.95 reference oscillator signal on pin 1 and generates high or low pulses out of pin 5 to the active integrator, U3016-B. The combined action of U3016-B and the RC loop filter apply a DC tuning voltage to CR3014 in the VCO. The voltage will vary from about 2.5 V at 118 MHz transmit to about 8.4 V at 136.9 MHz receive.

Internal to U3011 are two dividers which divide the 20.95 reference frequency and the VCO frequency down to a lower reference frequency of 25 kHz. The divided reference pulses appear on

U3011 pin 13 and the divided VCO frequency pulses appear on pin 14; these pulses are only about 50 ns wide on pin 13 and 300 ns wide on pin 14 and will occur at a 25 kHz rate.

In the transmit mode, the VCO frequency is the same as the unit's operating frequency. In receive, the VCO frequency is 21.4 MHz higher than the operating frequency. U3012 buffers the VCO output directing the signal three places. The output of U3012 goes back to the synthesizer IC, U3011, to keep the loop locked. It also goes to the first mixer to serve as the first LO injection (Gate 2 of Q3011 in a unit without Mod 5 and to U3028 in units with Mod 5). In the transmit mode, U3012 also drives the TX Driver stage Q3015. Approximately +15 dBm of output power is available at J3005 when Q3012 is turned on in transmit providing power to Q3015. This unmodulated signal out of the TX driver stage is fed to the Transmitter board. In receive, when Q3012 is off, there is less than 0 dBm at J3005.

A pin diode switch consisting of CR3033, is placed between the output of U3012 and the base of Q3015 to remove the drive power to Q3015 in the receive mode.

In a normal synthesizer locked state, the LD output of U3011 (pin 7) will be high. Low going pulses will be seen at the LD output if the synthesizer is unlocked. These pulses are filtered by C3092 and applied to comparator U3016A. The output of U3016 and the Com Synth Lock line at P3001 pin 16 is low in a locked condition and high in an unlocked condition.

4.3.2 TRANSMITTER

4.3.2.1 RF PATH

The RECEIVER BOARD lineup of Q3020, U3012 and Q3015 produces an unmodulated RF drive level of 30 mW (+15 dBm) at J3005 on the desired frequency of operation in the COM BAND. The drive signal is conducted by 50 ohm transmission line and fed to the 2N4427 PREDRIVER, Q4004. This stage provides approximately 9 dB of gain, boosting the level of the signal to 250 mW (+24 dBm) for the JT2468 DRIVER, Q4005. Approximately 14 dB of gain is achieved in this stage, to a level of 6 watts for the MRF 173 FINAL, Q4006. The final stage produces 9 dB of gain, to a level of 50 watts peak power. There is a loss of about 1 dB in the HARMONIC FILTER which comprises the Low Pass Filter and Directional Coupler, so the peak output power at the COM ANT is 40 watts for full AM modulation of a 10 watt carrier.

4.3.2.2 AUDIO PATH

Audio input from the MIC input is processed by U1023-A which provides bias for carbon mic elements, and buffering to the digital pot, U1032-A, for mic gain adjustment. The circuitry of U1034-C, U1032-B, U1034-B, and Q1042 comprise the MIC COMPRESSOR to ensure modulation is maintained at the highest average level as possible without overmodulating the carrier on modulation peaks. The shape of the audio response in the BPF is determined in large part by U1035-C to provide a 6 dB bandwidth from 350 to 2500 Hz. The KX165A has an additional audio filter which is needed to meet the 8.33kHz channel spectral requirements. The KX165A TX Audio Adapter Board provides this additonal audio filtering. U1 and its surround
ing components form a switched capacitor filter having an elliptic response.

4.3.2.3 MODULATOR PATH

The audio signal from U1035-C TX Audio Adapter Board provides the reference to modulate the carrier by comparing detected RF, which is buffered by U1035-D, and provides the feedback in U1035-A, with the error amplified and applied to the transmitter final device's gate bias.

4.3.2.4 POWER CONTROL PATH

There are two control loops that monitor the modulator gate bias on TRANSMITTER BOARD Q1006. The main loop for power control detects output power (TRANSMITTER BOARD Directional Coupler & CR4004, U1035-D) and compares in U1035-A this sample against a reference for carrier power set, U1032-C buffered by U1035-C. This carrier power set reference is modulated by the processed audio from the MIC COMPRESSOR / BPF circuitry on the MAIN BOARD. The modulator gate bias is adjusted instantaneously to effect amplitude modulation of the carrier. RF drive to the gate is controlled by the second control loop. This loop which comprises U1034-D and Q1038 to drive Q4004, predistorts the signal fed to the final by accomplishing low level modulation of the predriver to a level of about 15% AM, allowing a very high degree of final modulation with low distortion.

4.3.2.5 THERMAL CUTBACK

The transmitter estimates ambient temperature by reading the internal thermistor, U1010, and applying offsets for unit specific operation (TOFF) and model specific operation (TAOS). TOFF is typically 0 because thermistor deviation is very small. TAOS is typically -7 for units with glideslope, and -4 for units without glideslope. The Transmitter will hold carrier power of 10 watts to +55C, and fall within the window of 2.5 to 6 watts at +70C.

4.3.2.6 TIMEOUT TIMER

The transmitter will allow continuous transmissions for durations of up to 30 seconds, after which the COMM frequency display will blink indicating timeout of the transmitter. This guarantees minimized interference from a stuck microphone condition which may not be noticed by the pilot.

4.3.3 NAV (VOR/LOC) RECEIVER

Refer to the Nav receiver schematic. Some Nav Audio receiver functions appear on the main board schematic.

4.3.3.1 Preselector and RF Amp

The front end of the Nav receiver employs a high-dynamic-range RF amplifier embedded in a 5-pole-band-switched preselector. Nav Signals at the Nav antenna connector are applied to the first two poles of preselector consisting of L3025, L3035 and associated circuitry. These two poles are band switched in two bands. When the operating frequency is below 113.6 MHz, the base of Q3029 is driven low by U3002 and U3001-F. This turns Q3029 on, turning on pin diodes CR3020, CR3022 and CR3026, lowering the response of the first two poles. At frequencies of 113.6 MHz or higher, these pin diodes are off, allowing the frequency of the preselector to rise. Q3028 is the RF amplifier operating in a lossless-feedback configuration. The gain of the RF amp is controlled by transformer T2 and Directional coupler T1 at about 15 dB. Q3027 is a constant current source for the RF amp, limiting the current through Q3028 to about 30 mA. Three additional poles of preselector filtering consist of L3023, L3027, L3036 and associated circuitry. When CR3021 and CR3027 have a positive voltage on their anodes, they turn on to provide RF AGC action.

4.3.3.2 First Mixer

FET mixer U3022 is a high-level-doubly-balanced mixer that converts the input received frequency on pins 12 and 14 down to a 20.5 MHz first IF Frequency on pins 5 and 10. The first local oscillator signal is applied to pins 1 and 3 at a frequency 20.5 MHz below the desired operating frequency.

4.3.3.3 First IF

The low output impedance of the mixer at the output of T3005 is impedance matched by L3033 and C3317 to the higher input impedance of the 20.5 MHz 8 pole crystal filter, FL11. The output of the filter is likewise matched to the low input impedance of IF amp Q3035 by L3034 and C3312. After being amplified by Q3035, the 20.5 MHz signal is passed to pin 18 of U3023, an AM receiver IC.

4.3.3.4 AM Receiver IC and Second IF

U3023, includes an additional gain controlled 20.5 MHz amplifier, a second mixer, amplification at 450 kHz, a detector and AGC circuitry. The 20.5 MHz signal applied to U3023 pin 18 is amplified then mixed down to 450 kHz, the second IF frequency. The 20.95 MHz reference oscillator is applied to U3023 pin 16 from the Q3023 buffer-amp to serve as the second LO.

The 450 kHz second IF signal output at pin 1 of U3023 is impedance matched by L3038 and C3314 to FL3008, a 450 kHz ceramic filter. The filtered signal is amplified by Q3034 and then returned to U3023 at pin 3. Within the receiver IC, the 450 kHz is further amplified and passed to an internal detector. C3285 and C3299 filter an internal reference voltage within U3023 and are important to maintaining accurate VOR bearing information. The gain of both the 20.5 MHz and 450 kHz amplifiers internal to U3023 is controlled by the AGC voltage on pin 7. AGC time constants are established by C3230, C3248, C3249, and C3286. The amplified 450 kHz signal is available at pin 12 of U3023 (TP3009) to allow easy viewing of the signal with an oscilloscope.

4.3.3.5 RF AGC

The AM receiver IC, U3023, outputs an IF AGC voltage on pin 7. This voltage will be about 1 VDC with no input signal to the unit and rise to about 2 VDC with a strong input signal. U3020-B is used to monitor the IF AGC voltage, and when it reaches about 1.7 VDC, the U3020 pin 7 voltage increases to a positive voltage, turning on pin attenuator diodes CR3021 and CR3027 in the preselector. As these diodes turn on, they attenuate the incoming signal to prevent the receiver from being overloaded on strong signals.

4.3.3.6 Nav Synthesizer and LO Amplifier

Serial data from the micro processor is sent to program the synthesizer IC, U3018. U3018 compares VCO output on pin 8 with the 20.95 MHz reference oscillator signal on pin 1 and generates high or low pulses out of pin 5 to the active integrator, 3019-A. The combined action of U3006-B and the RC loop filter apply a DC tuning voltage to CR3025 in the VCO. The voltage will vary from about 3.5 V at 108 MHz to about 7 V at 117.95 MHz .

Internal to U3018 are two dividers which divide the 20.95 MHz reference frequency and the VCO frequency down to a lower reference frequency of 50 kHz . The divided reference pulses appear on U3018 pin 13 and the divided VCO frequency pulses appear on pin 14; these pulses are only about 50 ns wide on pin 13 and 300 ns wide on pin 14 and will occur at 50 kHz rate. The VCO frequency is 20.5 MHz lower than the receiver's operating frequency. U21 buffers the VCO output and sends it back to the synthesizer IC, U3018, to keep the loop locked. The output of U3021 is also routed to Q3030, the Nav local oscillator amplifier. A lowpass filter on the output of Q3030 reduces the LO harmonics before T3003 transforms the low source impedance of Q3030 to a high impedance on the balanced input of the mixer at pins 1 and 3 of U3022.

4.3.3.7 Nav Audio

Nav audio is output from the receiver board on the nav composite line. The audio then is input to the main board's nav audio filter which is a 4 pole 350Hz-2500Hz bandpass filter composed of

U1017-A&B and associated circuitry. The output of the audio filter is then amplified by a gain of 1.6 by U1029-D before passing through the digital potentiometers U1016-B&D. After the potentiometers, the signal routes to unity gain amplifier U1029-C and then to audio power amplifier U1031-B which has a gain of about 35. T1002 transforms the signal in order to drive a 500 ohm load.

The ident filter, U1017-C&D and related components, form a 1020 Hz notch filter. When the notch is enabled (front panel ident knob in), the 1020 Hz identification signal is attenuated by more than 15dB. The ident filter is disabled when the front panel ident knob is pulled out enabling the 1020 Hz signal to pass to the audio amplifiers.

4.3.3.8 VOR Converter

The KX155A has an internal VOR converter that can convert the VOR receiver composite to bearing/radial information. The nav composite signal routes to a 9960Hz bandpass filter, U1015C. The signal is "squared up" and fed to a phase-lock loop, U1003. The PLL demodulates the 9960 Hz composite in order to extract the 30 Hz reference which is then directed to the microprocessor for signal processing.

The composite signal also routes to anti-aliasing filters (lowpass filters), U1004-C&D before it is fed to the microprocessor to be converted to bearing/radial information. The lowpass filters have a 3dB bandwidth of about 1kHz.

The composite signal also is fed to U1015-A where its level is adjusted so that it can be set to drive external converters.

Table 4-2 GS/LOC FREQUENCY PAIRS VS. GS VCO FREQUENCY

LOCALIZER FREQUENCY (MHz)	GLIDESLOPE FREQUENCY (MHz)
108.1	334.7
108.15	334.55
108.30	334.10
108.35	333.95
108.50	329.90
108.55	329.75
108.70	330.50
108.75	330.35
108.90	329.30
108.95	329.15
109.10	331.40
109.15	331.25
109.30	332.00
109.35	331.85
109.50	332.60
109.55	332.45
109.70	332.20
109.75	333.05
109.90	333.80
109.95	333.65
110.10	334.40
110.15	334.25
110.30	335.00
110.35	334.85
110.50	329.60
110.55	329.45
110.70	330.20
110.75	330.05
110.90	330.80
110.95	330.65
111.10	331.70

LOCALIZER FREQUENCY (MHz)	GLIDESLOPE FREQUENCY (MHz)
111.15	331.55
111.30	332.30
111.35	332.15
111.50	332.90
111.55	332.75
111.70	333.50
111.75	333.35
111.90	331.10
111.95	330.95

4.3.4 GLIDESLOPE RECEIVER

4.3.4.1 General

The Glideslope Board contains a receiver that may be tuned throughout the Glideslope frequency band of 329.15 to 335.00 MHz. The Glideslope operating frequency is paired with a selected Localizer frequency (Reference Table 4-2.). The radio selects the proper Glideslope frequency based upon the Localizer channel. Digital and analog I/O comes from the VHF Main board via a 12 pin ribbon cable. The RF input comes in externally through the antenna connection on the back of the radio. There is a rear edge card connector that is used to output analog converter signals necessary to drive an external indicator. The receiver gets its synthesizer tuning, and DC power from the VHF Main board.

4.3.4.2 Variable Gain RF Amplifier

Q6 is an N-channel depletion type dual gate MOS-FET that is the active component in the Variable Gain RF Amplifier. The RF AGC voltage is applied to one of its gates, and controls the amount of RF gain through the amplifier. The RF AGC voltage can vary from 0 to 8.5 V, resulting in a gain variation of +20 dB to -30 dB of gain. The full range of gain adjustment occurs as the input RF power varies from -90 dBm to -50dBm. A moderate amount of preselection filtering is accomplished in the tuned matching circuits of L1/C48/L5 and C49/L6/C7. C50 forms a 166MHz series resonant circuit with C48/L5. This series resonant circuit filters out the 1/2 channel frequency so that the out of band response is minimized.

4.3.4.3 13 dB Attenuator

The 13 dB RF Attenuator reduces the amount of RF power input to later stages. Reducing the signal level improves the crossmod performance of the MMIC RF Amplifier and the Mixer. Excess RF power exists because of the Mixer LO to Antenna Port reverse isolation requirement necessitating the use of the RF MMIC Amplifier.

4.3.4.4 RF MMIC Amplifier

This is a high reverse isolation silicon MMIC amplifier with a gain of 20 dB in the GS frequency band.

4.3.4.1.5 16 dB Attenuator

The 16 dB RF Attenuator reduces the amount of RF power input to the Mixer. Reducing the signal level improves the crossmod performance of the Mixer. Excess RF power exists because of the

Mixer LO to Antenna Port reverse isolation requirement necessitating the use of the RF MMIC Amplifier.

4.3.4.6 Mixer

Q7 is an N-channel depletion type dual gate MOS-FET that is the active component in the Mixer. The output from the synthesizer's VCO buffer amplifier is incident upon one of the gates and serves as the LO (Local Oscillator) for the Mixer. The GS signal is incident upon the other gate, and is the RF input to the Mixer. The LO is 30 kHz below the GS signal so that a 30 kHz IF (intermediate Frequency) is generated. Conversion loss from the input RF lever to the IF power level absorbed by the IF Amplifier #1 is 13 dB. This loss is do mainly to an impedance mismatch between the Mixer and the IF Amplifier #1 causing most of the Mixer's output power to be dissipated in R2.

4.3.4.7 IF Amplifier #1

Q5 is the active device in the IF Amplifier #2. Gain at the 30 kHz IF is 30 dB.

4.3.4.8 50 kHz Low Pass Filter

This 9 pole filter has a Chebyshev response and a -6dB pass band of 50 kHz minimum. Out of band rejection is typically 60 dB at 90 kHz. Ultimate refection is greater than 70 dB.

4.3.4.9 IF Amplifier #2

Q1 is the active device in the IF Amplifier #2. Gain at the 30 kHz IF is 30 dB. This is the power gain from the power absorbed by the Amplifier #2 input to the power delivered to R10.

4.3.4.10 IF Amplifier #3

U4 is an IF VGA (Variable Gain Amplifier). Its gain is adjusted by the IF AGC amplifier. The RF VGA has more effect on receiver gain over the power range of -90 dBm to -50 dBm than the IF VGA. From -105 to -90 dBm and -50 to -33 dBm the IF VGA has more effect on overall receiver gain than the RF VGA.

4.3.4.11 IF Amplifier #4

Q2 is the active device in the IF Amplifier #4. Gain at the 30 kHz IF is 25 dB. This is the power gain from the power absorbed by the Amplifier #4 input to the power delivered to the Detector.

4.3.4.12 Detector

Q4 is the active device in the 30 kHz IF detector. Q3 supplies a temperature compensated bias for Q4. C34 and R86 form an RC filter that filters off residual 30 kHz IF but does not filter any of the 90/150 Hz composite audio.

4.3.4.13 Composite Audio Buffer Amplifier

Op-Amp U3-A is used to amplify and DC level shift the 90/150 Hz audio before it goes to the main board. C106 and R36 introduce a low pass response to filter out some of the higher frequency noise.

4.3.4.14 IF AGC Amplifier

Op-Amp U3-B is configured as an integrator and is the IF AGC Amplifier. The DC level from the Detector is used by the AGC loop to maintain a constant carrier input power into the Detector. The output of this Amplifier is connected to the IF VGA, to adjust the IF gain, and is the input to the RF AGC Amplifier. The IF AGC voltage varies from 3.6 V with no RF input, to 6 V with -33 dBm RF input.

4.3.4.15 RF AGC Amplifier

Op-Amp U3-D is the RF AGC Amplifier with a gain of 16 and an adjustable DC offset. While the RF AGC is in its linear region, it varies 16 times faster than the IF AGC. That is why the RF AGC predominates while it is active. R25 is used to set the point at which the RF AGC becomes active. This point is factory set at -87 dBm. The RF AGC voltage varies from 7.5 V with no RF input, to 0.1 V with -33 dBm RF input.

4.3.4.16 20.95 MHz Crystal Oscillator

Q8 is the active device in this common collector Synthesizer Reference Crystal Oscillator. Y1 is an AT cut crystal that is the Oscillator's frequency determining device. C66 is a variable NPO capacitor that adjusts the operating frequency of the Crystal Oscillator. Q9 is used in a buffer amplifier that increases the level of the crystal oscillator to the level needed by the Synthesizer IC U6. The buffer amplifier also provides isolation to the Crystal Oscillator.

4.3.4.17 Synthesizer

Serial Data from the Main Board is sent to program the Synthesizer IC, U6. The synthesizer compares a divided down 20.95 MHz reference with a divided down sample of the VCO output. U6 divides the reference and VCO down to 10 kHz for phase/frequency comparison. U6 is a dual modulus synthesizer, so that the VCO can be tuned in 10 kHz steps throughout the GS band. Operation is limited to the GS channels less the 30 kHz IF offset (low side injection). The range of operation is therefore 329.12 MHz to 339.97 MHz. U6 pin 5 is the synthesizer charge pump output and is used as the input to the loop filter/integrator U5-A.

4.3.4.18 LO Frequency Dither

A sample of the 10 kHz comparison frequency is taken from U6-14 and divided by 16 in U8. the resulting 625 Hz square wave is used to dither (frequency modulate) the VCO. the 625 Hz square wave is present on U8 pin 11 and is changed into a ramp waveform by the RC combination of R89 and C83. It is this ramp that varies the VCO/LO frequency at a rate of 625 Hz and a deviation of 1 kHz. Dithering eliminates the possibility of zero beat problems in the IF. this would be the case of a receiver or ground station failure causing a receive or transmit frequency error that allows the LO and RF to be only 90 Hz or 150 Hz offset.

4.3.4.19 332 MHz VCO

Q10 is the active device in this common base VCO (Voltage Controlled Oscillator). C75 is a mechanical variable capacitor that is adjusted so that the electronic tuning range is centered in the GS frequency band. Electronic tuning is provided by varactor CR2. the tuning voltage typically ranges from 3.1 V to 4.8 V to cover the range of 329.12 MHz to 334.97 MHz. U7 is an MMIC buffer amp that increases the power level of the VCO enough to drive the synthesizer and Mixer LO.

4.3.4.20 Voltage Reference

U12 generates a stable +5 V reference voltage that is used by the converter circuitry. The Flag Driver and Indicator Driver use the +5 V reference directly. the GS Down voltage is derived from dividing the +5 V in half to +2.5 V, and is then buffered through U10. the +2.5 V is the 0 ddm reference voltage (GS Down). GS Up varies above and below this voltage to move the indicator up and down.

4.3.4.21 Flag Driver

The Main Board sends serial data to U11 to operate the flag. U11-B is in one of two states. The first state is with the flag in view, wiper connected to ground through pin 2. The second state is with flag pulled out of view, wiper connected to +5 V through pin 3.

4.3.4.22 Indicator Driver

U9, U11-D, and U11-C form the active portion of the Indicator Driver. Digital potentiometer U11-C adjusts the converter deviation. It allows the GS Up to be adjusted above or below GS Down's 2.5 V reference. the range of GS Up is 2.2 to 2.8 V (+/- 300 mV from GS Down). The 0 ddm centering voltage may be adjusted during Installation so that the Indicator's needle is centered for a received 0 ddm GS signal. Digital potentiometer U11-D adjusts the half scale deflection. the half scale deflection may be adjusted during Installation so that the indicator's needle reads half scale for a received .091 ddm GS signal.

4.3.5 AUDIO BOARD

The audio inputs from AUX_1_AUDIO_IN (J155A2-H), AUX_2_AUDIO_IN (J155A2-F), AUX_3_AUDIO_IN (J155A2-4), COM AUDIO IN (J155A2-J), and INTERCOM_MIC_IN (J155A2-8) are summed and inverted at U6002-C. U6003 generates the DC bias for the microphone input. R6024 is an external adjustment that allows the gain of the INTERCOM_MIC_IN to be varied. The output of the U6002-C summer is fed into inverting amplifier U6002-B which drives SUMMED AUDIO OLD OUT (J155A2-9). The output of the U6002-C summer is fed into inverting amplifier U6002-D which drives SUMMED AUDIO NEW OUT (J155A2-7). The output of U6002-D is also fed into amplifier U6004. The amplifier of U6004 drives transformer T6001. The output of T6001 is fed to 500 OHM AUDIO OUT (J155A2-D).

The speaker input amplifier U6002-A accepts an input from either COM AUDIO OLD IN (J155A2-2) or COM AUDIO NEW IN (J155A2-10) depending on the installation. The output of U6002-A is fed to Q6001. The gate of Q6001 is connected to COM MIC KEY (J155A2-C) through R6019 and CR6001. The gate of Q6001 is also connected to INTERCOM MIC KEY (J155A2-K) through R6019 and CR6007. If either COM MIC KEY or INTERCOM MIC KEY is externally grounded, Q6001 will not allow any signals to pass through. Q6001 is connected to the inverting input of amplifier U6001-A through R6046 and R6014. R6046 controls the gain of the speaker network. 4 OHM AUDIO BRIDGED is tied to the base of Q6005. When 4 OHM AUDIO BRIDGED is grounded, Q6005 turns off and Q6004 turns on which reduces the amount of signal reaching the inverting input of U6001-A by approximately half. The output of U6001-A drives 4 OHM AUDIO OUT (J155A2-1). The output of U6001-A is also divided down with R6005 and R6006 and fed into the

inverting input of U6001-B. The output of U6001-B drives 4 OHM AUDIO OUT 14V LO and is approximately the same level as 4 OHM AUDIO OUT but the polarity is reversed.

4.3.6 CPU FUNCTION

The CPU function consists of a microprocessor, RAM, ROM, an RS-232 asynchronous serial communication port, and various discrete inputs and outputs. A general serial control bus was created using CPU discrete I/Os to permit control of serial digital devices in the system; the integrity of this bus is not effected by interrupts. The QSM serial control bus was reserved for front panel control (display and front panel buttons/knobs) to simplify system software and minimize the overhead incurred by display control. Refer to the main board schematic .

4.3.6.1 CPU

The CPU is a Motorola 68HC16Z1 microprocessor, U1014, with several integrated functions. It has a CPU16 core with 1MB address space made up of sixteen 64kbyte banks, and a maximum clock speed of 16.78Mhz. A System Integration Module (SIM), provides address decoding, an interrupt controller and discrete I/Os. The Queued Serial Module (QSM) contains synchronous and asynchronous serial I/Os. A General Purpose Timer (GPT) module provides flexible timing functions and, finally, an 8 channel Analog to Digital Convertor module (ADC), U1021, provides analog inputs.

The clock provided to the processor is a crystal controlled 32.768 kHz, Y1001.

The CPU uses a 5.0 VDC precision reference, U1010, that supplies the CPU's ADC unit. There is also a 5V power monitor, U1011, which resets the system if the voltage falls below a 4.75VDC safety limit.

U1019, is a flash memory device that holds the software that controls the CPU. The flash memory allows the unit to be reprogrammed via the RS-232 port at the rear connector as software upgrades become available. U1002, U1006, U1008, and U1013 are RAM that interface to the CPU, and serve as temporary storage for the CPU operation.

4.3.6.2 Configuration EEPROM

Configuration EEPROM, U1001, contains information unique to each unit that is required for nav and com operation such as channeling, program memories, electronic tuning, and etc.

4.3.6.3 Digital Interfaces to Other Modules

There are digital logic interfaces to other assemblies of KX155A, including the com/nav receiver, com transmitter, VOR/LOC convertor, glideslope, and the front panel with the display and input devices. These lines are either discrete logic level controls or synchronous serial data lines.

Many I/O lines to these assemblies are filtered with a 330pF ceramic cap and in some cases ferrite beads (lossy inductor) or series resistors.

4.3.6.4 Discrete Interfaces

There are a few discrete logic level inputs to other instruments and equipment on the airplane. All these inputs are isolated with a 330pF ceramic capacitor, diode and PNP transistor. An optional Zener clamp can be used for lightning protection per DO-160C. This buffer should be sufficient in keeping spikes and other harmful transients from damaging digital ICs on board. An example of this type of interface can be seen at CR1021, R1249, C1223, CR1044, Q1012, R1102, R1406. These inputs go directly to microprocessor discrete inputs. Analog/power/non-TTL logic outputs are driven by transistors or FETs and are also optionally zener protected.

4.3.6.5 Analog Interfaces

The HC16 has an 8 channel ADC. However, there are 15 analog voltages to monitor. Therefore, an analog multiplexer, U1021, is used to select some of the low-speed signals (mostly voltage monitors).

Signals monitored by the CPU ADC include:

VOR 30Hz FM
FILTERED_NAV_COMPOSITE
FILTERED_GLIDESLOPE_COMPOSITE
VOR/LOC_FILTERED_STATOR_F
VOR/LOC_FILTERED_STATOR_D
COM_VOLUME
NAV_VOLUME
ANALOG_MUX_OUT which is one of the following
PHOTOCELLTEMPERATURE
+5V (through divider)
-200V (through divider)
-12V (through divider)
+9V (through divider)
FILTERED_11-33_VDC_POWER

Volume controls are done by applying a +5V reference across the Com and Nav volume potentiometers on the front panel then reading the wiper voltage with the ADC. The audio volume is then adjusted using digital potentiometers in the audio circuit controlled through the general serial bus.

Digital potentiometers U1016, U1028, and U1032 also adjust the level of sidetone, intercom, transmitter power, receiver noise squelch, RF AGC, and etc.

The 68HC16Z1 also has one RS232 port. This port is level-shifted to RS232 logic levels through a MAX202, U1022, converter and optionally protected by a bidirectional zener. This port can be used for the KX155A to communicate with other devices, and may be used to update software in the field.

The unit also makes available the aircraft power bus as an output that is controlled by the on/off switch. Q1044 is turned on when the Power ON* line goes low.

LOC ENERGIZE* goes low when Q1017-A is turned on; this is used to signal external equipment. Q1019 goes low in order to turn on the internal glideslope receiver.

Audio Alert* goes low in order to activate a sound device such as a sonalert or other audio annunciator.

4.3.7 POWER SUPPLY

A flyback power supply is used to supply all of the low level power requirements. It consists of a hash filter, flyback transformer, rectifier/filters, current mode controller and power switch, a post regulator for the display voltage and on-off switch circuitry.

Aircraft power is applied to the hash filter, C1208, C1209, C2140, C1266, C1282, C1288, CR1042, L1020 and L1021. These components attenuate noise coming in on the 11-33_VDC_POWER line and switching noise from the flyback regulator. CR1042 suppresses transients on the 11-33_VDC_POWER line.

The Flyback transformer consists of T1003. When Q1045 is turned on, energy is stored in the primary of T1003. This energy is dumped into the rectifier capacitors when Q1045 is turned off.

The Rectifiers/Filters consist of CR1048, C1210, C1311 and C1312 (-200V), CR1051 and C1226 (-12V), CR1059 and C1269 (+9V), and CR1058 and C1252 (+5V).

The Current Mode Controller and switch consists of U1036, Q1045 and associated components. The switching frequency of the supply is 125.0 kHz CR 130.124 kHz. In units without Mod 5, a 20.95 MHz signal is received from the receiver board, amplified by Q1026, and divided down to 131.124 kHz by U1024 and U1025. This 131.124 kHz signal determines the power supply operation frequency. In units with Mod 5, the power supply reference frequency is 125 kHz. This 125 kHz signal is derived from a 500 kHz ceramic oscillator, Y1002, and inverter U1024. U1026 divides the 500 kHz signal down by 4 before it is fed to inverter U1007-F and then to U1036 pin 4.

R1341 and C1280 are parts external to U1036 that set the frequency of oscillation until the supply has reached proper output voltage and synchronization is provided from the digital circuitry on the Main Board. The output of the +9V rectifier is feed back to U1036 via R1295, R311 and R1312. If this voltage is higher than the reference voltage (pin 8 of U1036) the peak current of the switch (Q1045) is reduced by reducing pulse width of the drive (U1036 pin 1) to the switch thereby lowering the output voltage of the +9V rectifier. U1036 senses the peak current through the switch by monitoring the voltage across R1319 and R1320. R1345 and C1290 attenuate high frequency noise that comes from the switch and CR1067 reduces the voltage needed across R1319 and R1320 in order to reach the level required by U1036. R1314, R1316 and CR1064 limits the maximum pulse width. A soft start feature is provided by C1264. R1312, R1313 and C1278 provide compensation for the power supply feedback loop.

The on-off switch circuitry consists of two current sources and a switch, all of which are turned on by the front panel on-off switch providing a short to ground. The current sources (Q1040 and Q1041 and associated components supply current to U36 until the soft start capacitor (C264) has charged to 1.95 volts. Above this voltage U1036 pin 13 sinks current to ground turning off Q1041. Q1040 supplies enough current to drive the Q1041 current source but not so much that U1036 pin 13 cannot turn off Q1041. If all is working normally, the voltage to U1036 pin 14 will be supplied by the +9V power supply output when the soft start is complete and U1036 pin 13 turns off Q1041. If the +9V output has not reached the required regulated voltage, the soft start will begin again. This cycle will be repeated until the +9V voltage reaches the required value. If the power supply is overloaded for any reason (any of the outputs drawing too much current) the supply will continually go through the soft start cycle until the overload is removed.

4.3.8 FRONT PANEL AND DISPLAY MODULE

The front panel board has two connectors. P2011 comes from the main board and J2012 goes to the display module. The display signals that control the anode driver are DOTCLOCK (P2011-29), COLDATA (P2011-27), and COLDATA (P2011-25). These signals are routed directly to the display connector (J2012). ROWDATA (P2011-22) and ROWCLOCK (P2011-20) are buffered by U2009-A and U2009-B respectively. The buffered signals are level shifted from 5V/GND to -178V/-190V by Q2002 and Q2003. The level shifted signals are buffered by U2003-A, U2003-B, and U2003-C. The buffered signals then go to the display connector J2012. DISPEN (P2011-23) is level shifted from 5V/GND to -178V/-190V by Q2004. The level shifted signal is then fed to the display connector. LUMCTRL (P2011-9) is a voltage level between 0.4VDC and 1.9VDC that is used in conjunction with the duty cycle of DISPEN to control the brightness of the display. LUMCTRL is fed through to the display connector (J2012-16).

-190VDC (P2011-1,3) is sent to the display connector and is used to generate two more voltage levels. -178V is generated using zener diode CR2001. The -190V is pre-regulated to approximately -95V by Q2005 and then the -95V is regulated to -80V by U2014. The -178V and the -80V are fed to the display connector J2012.

RBSCLK (P2011-21) and RSP3* (P2011-6) are used to clock U2011 and U2012. U2011 and U2012 are parallel to serial shift registers that are chained together. The inputs to U2011 and U2012 are tied to the pushbuttons, push-pull switches, and the optical INC/DEC switches. The state of the inputs are shifted to the main board via SDI (P2011-16). The photocell R2040 is fed to the main board via FOTOCELL (P2011-14). DS2001, DS2002, DS2003, DS2004, DS2005, and DS2006 are the bulbs used to backlight the front panel. LIGHT_GND (P2011-12,19) is always tied to ground in the lighting bus. 14V/LGND (P2011-8,11) is connected to the lighting bus if a 14V lighting bus is in use and is left open if using a 28V lighting bus. 28V/LGND (P2011-10,13) is tied to the lighting bus if a 28V lighting bus is being used and is tied to ground if a 14V lighting bus is used.

The power switch is connected to the front panel via E18 (PWRSW) and E17 (PSWLO). PWRSW is fed to the main board via P2011-7 and PSWLO is fed to the main board via P2011-15. The COM volume pot is connected to the front panel at E19 (COM HI), E20 (COM WIPER), and E5 (COM LO). The COM volume pot connections are fed to the main board connector P2011 and the setting is read by an A to D converter on the main board processor. The COM volume is then controlled by setting digital pots on the main board. The NAV volume pot is connected to the front panel at E12 (NAV HI), E13 (NAV WIPER), and E14 (NAV LO). The NAV volume pot connections are fed to the main board connector P2011 and the setting is read by an A to D converter on the main board processor. The NAV volume is then controlled by setting digital pots on the main board