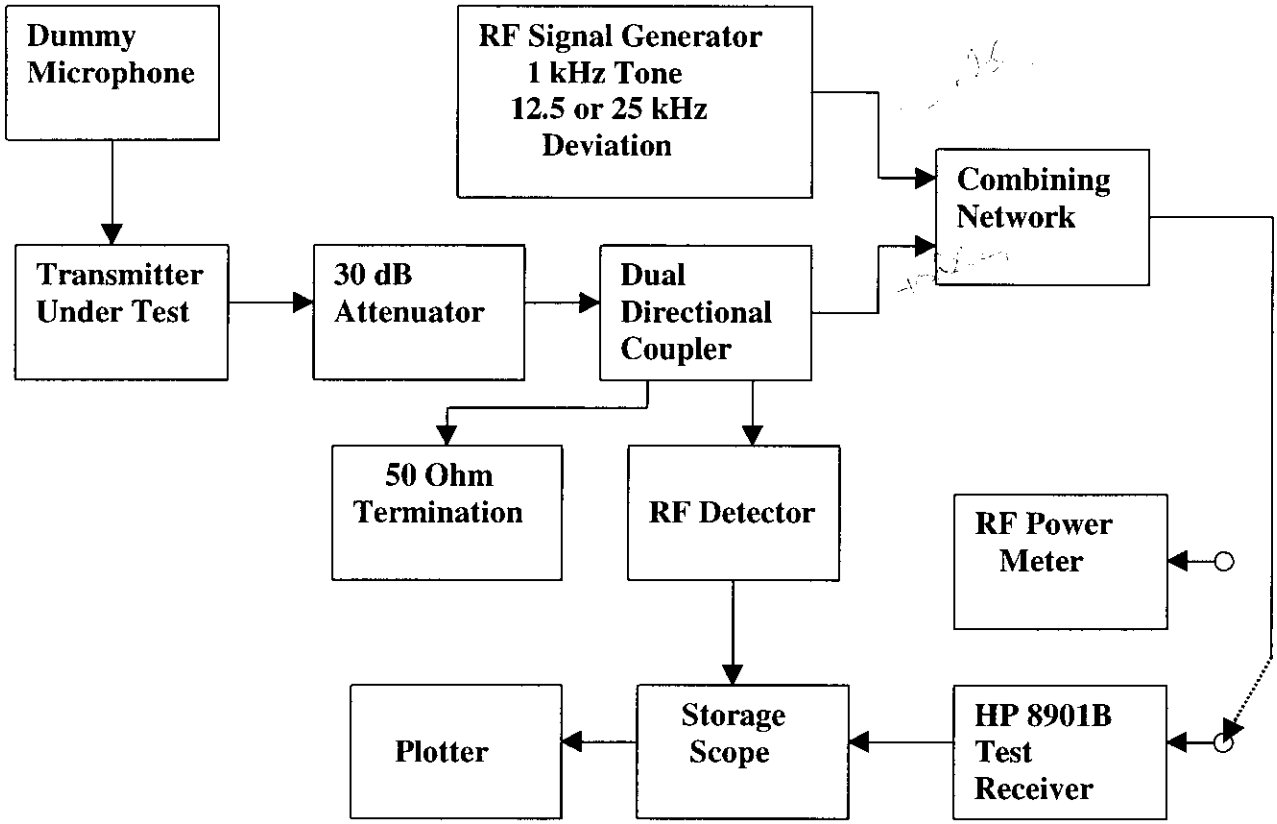
3. The transient frequency behavior test was performed according to TIA/EIA-603. The block diagram is shown below.



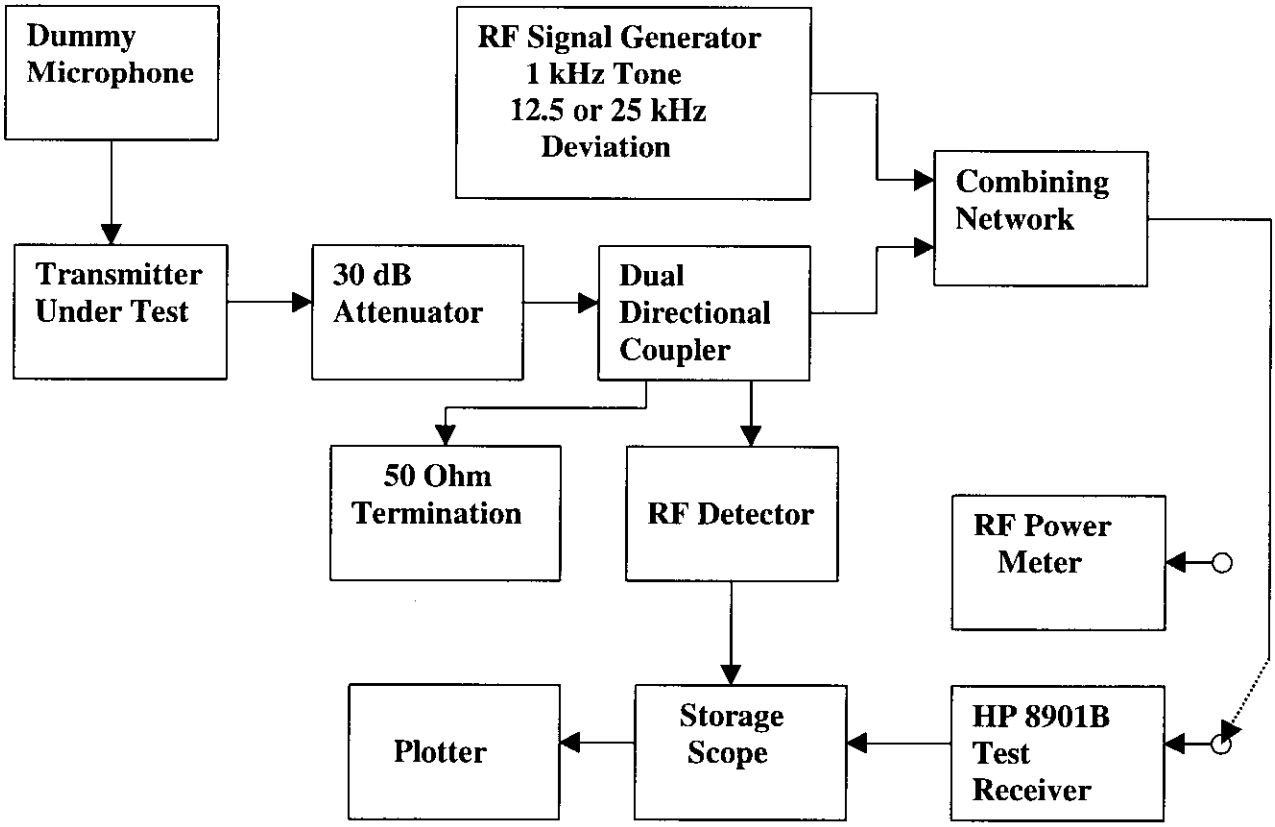
The level at the combining network input from the transmitter under test at the 50 watt level is about – 10 dBm. Additional attenuation was used in the 30 dB block that was not show. The RF signal generator was set at -30 dBm for the pictures sent which is per TIA/EIA-603 procedure. There is a degree of co-channel interference between the signal generator and the transmitter under test which accounts for the noise on the center line. We repeated the test with the signal generator set at –40 dBm. The characteristics are identical but the center line is now slightly less noisy.

4. The lower part of the original request contained a statement NOT to reply back but to just upload the data. We will send an email immediately after an upload from now on. Sorry for our confusion.

Thank you.

Engineering Manager

6. The transient frequency behavior test was performed according to TIA/EIA-603. The block diagram is shown below.



It should be noted that this equipment can have the transmitter PLL 'ON' continuously. The leakage is very low and the radiated tests were done with it powered and locked. As such, the transient lock for this equipment with the PLL 'ON' appears like nothing is happening. The unit was measured with PLL 'ON' and 'OFF' although it is recommended to the user the run the equipment with the PLL 'ON'

In the above block diagram, the RF signal generator is adjusted 20 dB below the signal from the Transmitter Under Test and the Test Receiver is fixed tuned to minimize any time delay in recovering the transient signal. This RF signal generator serves to provide a calibration to the transient display on the output of the test receiver. The use of a digital storage scope, however, causes aliasing to the calibration 1 kHz tone. Prior to plotting the screen, the scope was calibrated using the 1 kHz audio output of the test receiver (12.5 or 25 kHz deviation) for the full 8 cm display.

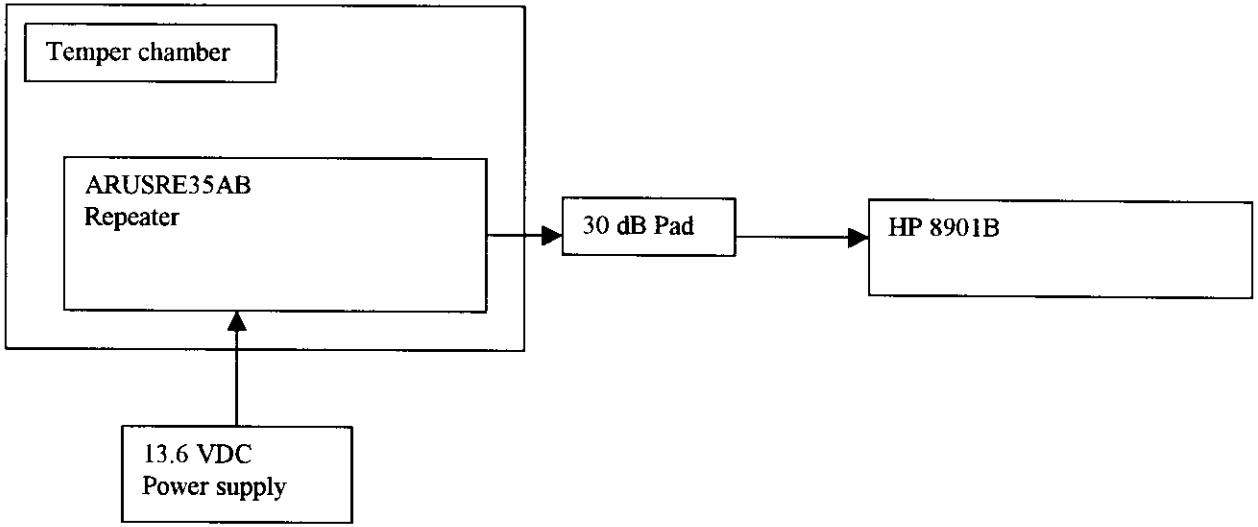
7. Data for item 90.214 for the narrow bandwidth channel is shown above in item four along with better labeled charts for the wide bandwidth channels.

8. Thank you.

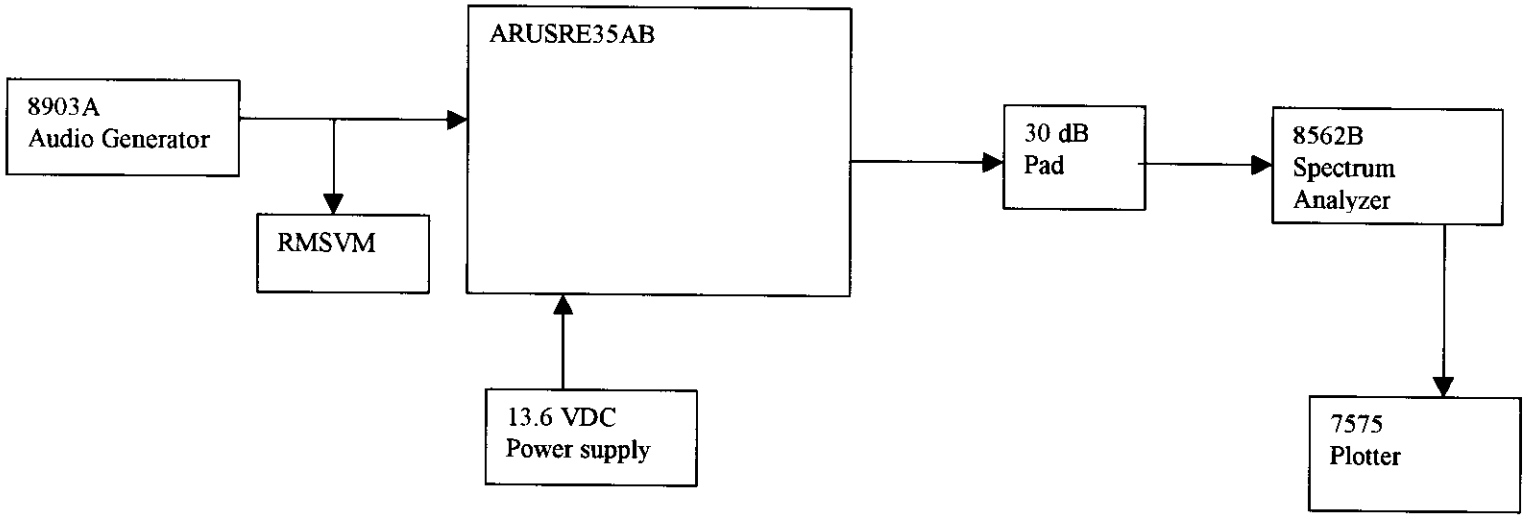
Engineering Manager

2.10 Figures

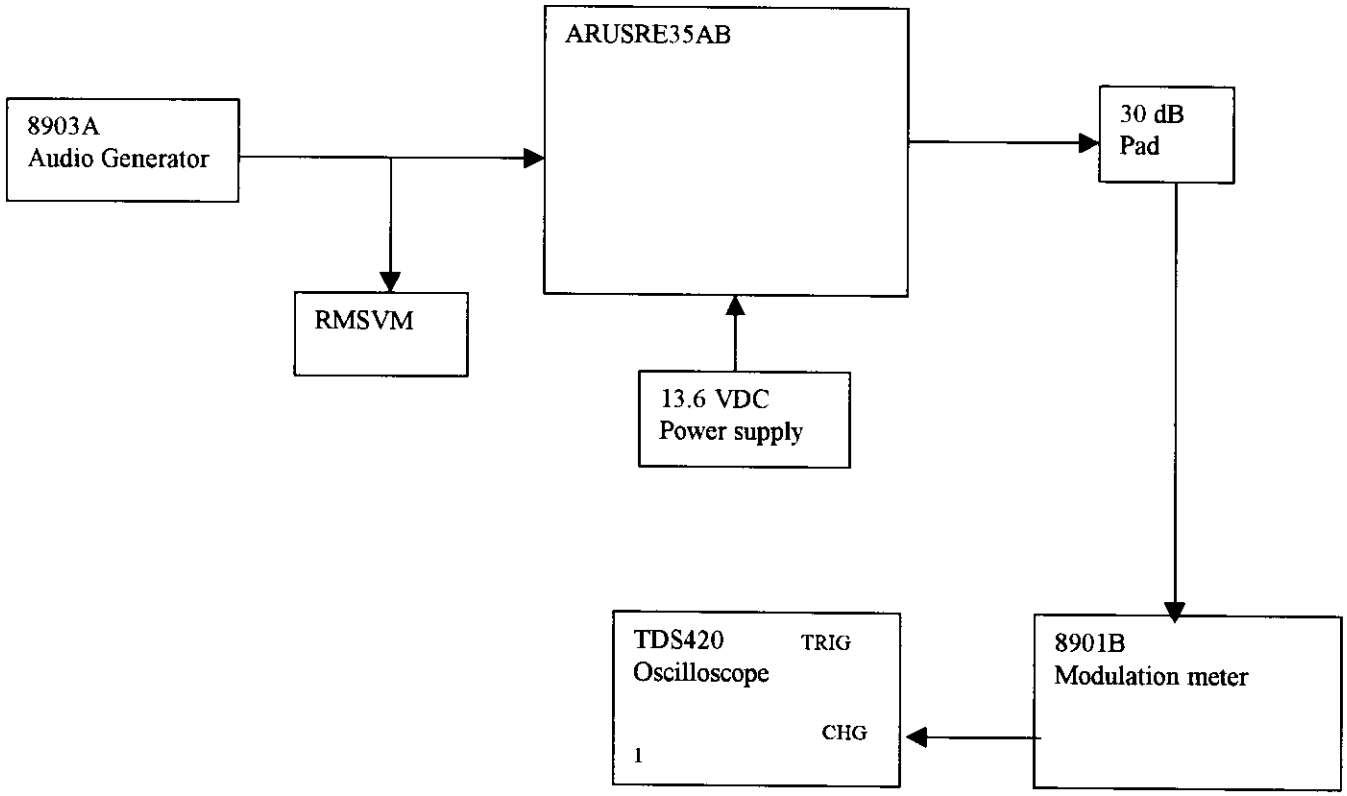
2.10.1 Figure 1. This test set up was used to test RF power output and Frequency Stability



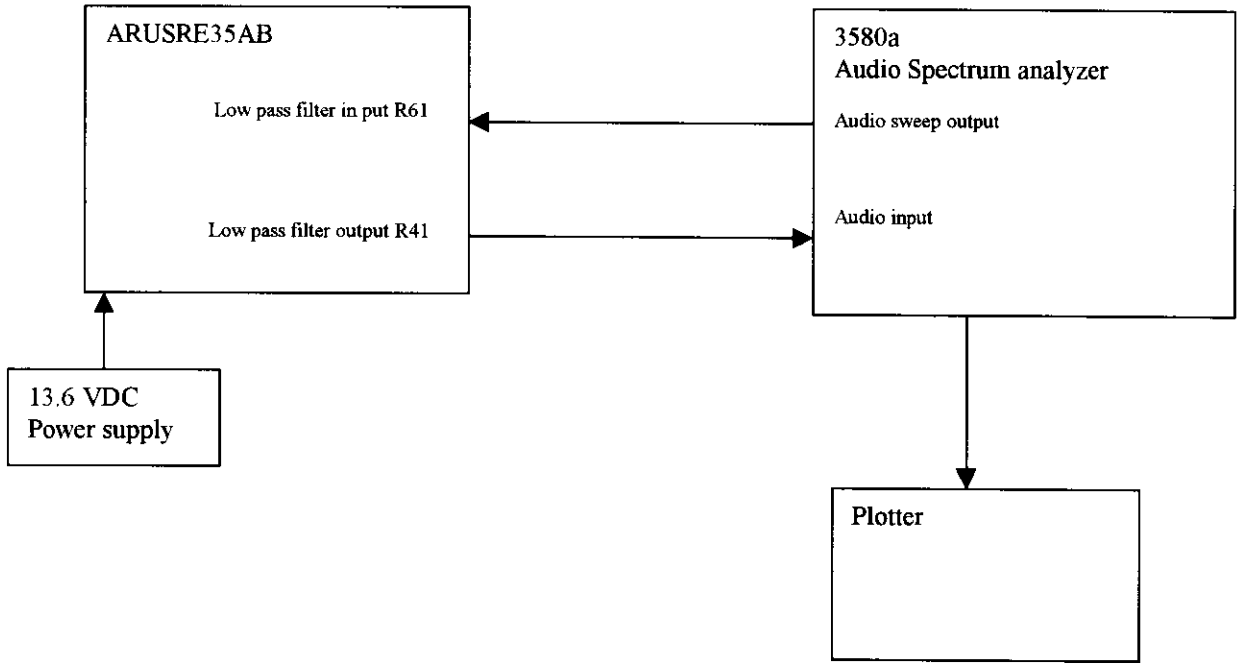
2.10.2 Figure 2. This test set up was used to do the Occupied Bandwidth Test



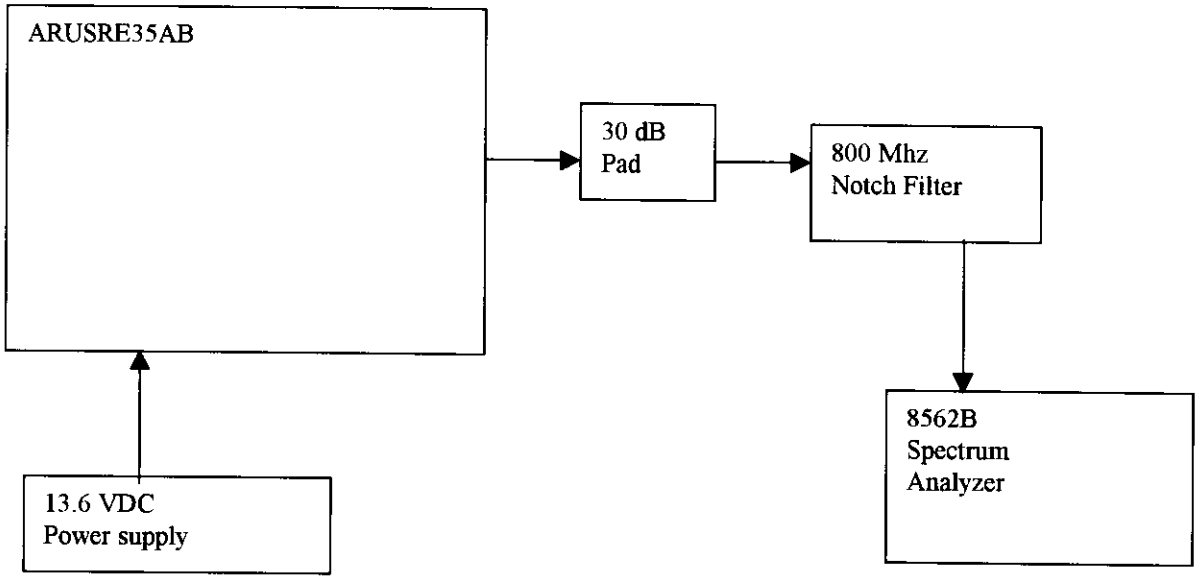
2.10.3 Figure 3. This test set up was used to do the Modulation Deviation Test and the Transmitter Audio Frequency Response Test



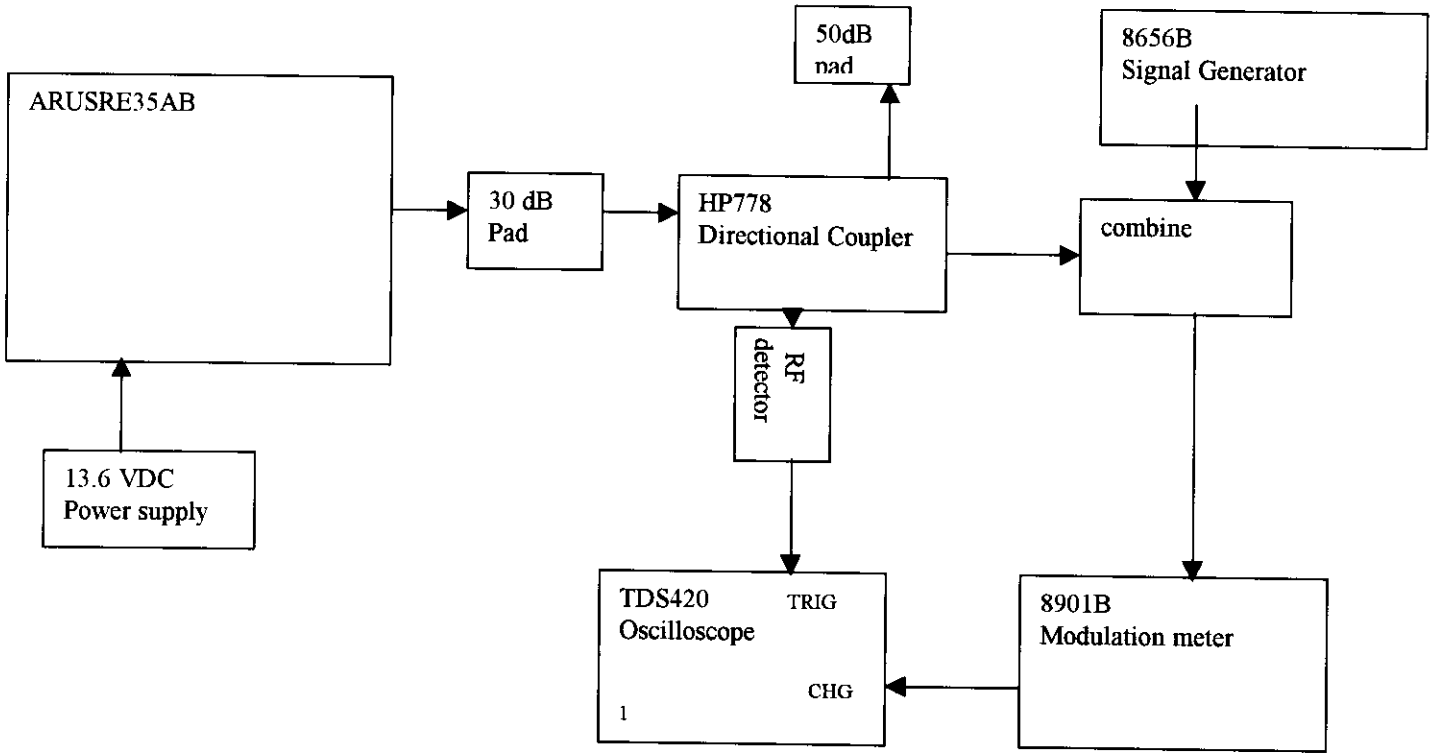
2.10.4 Figure 4 This test set up was used to do the Transmitter low pass filter Test

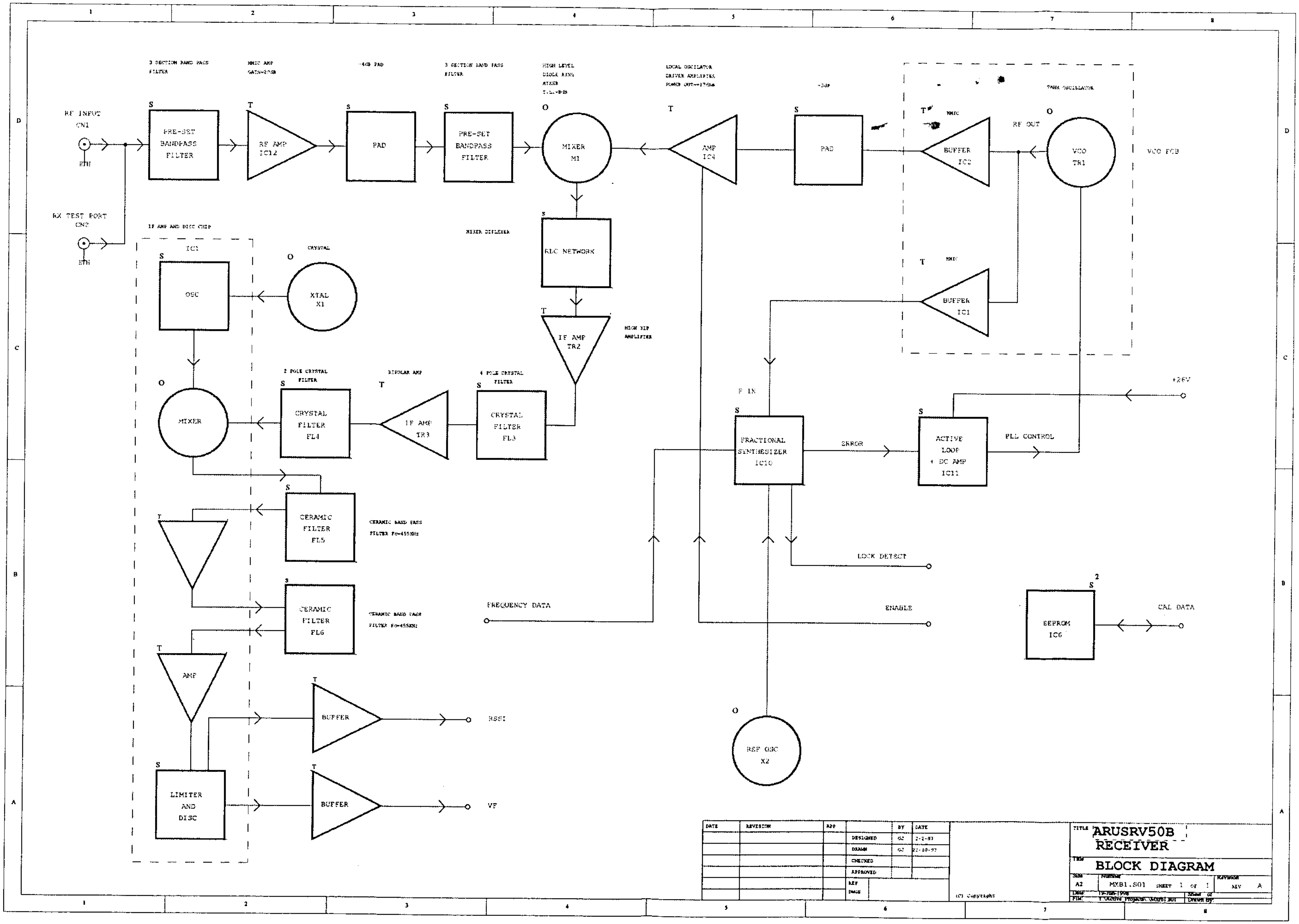


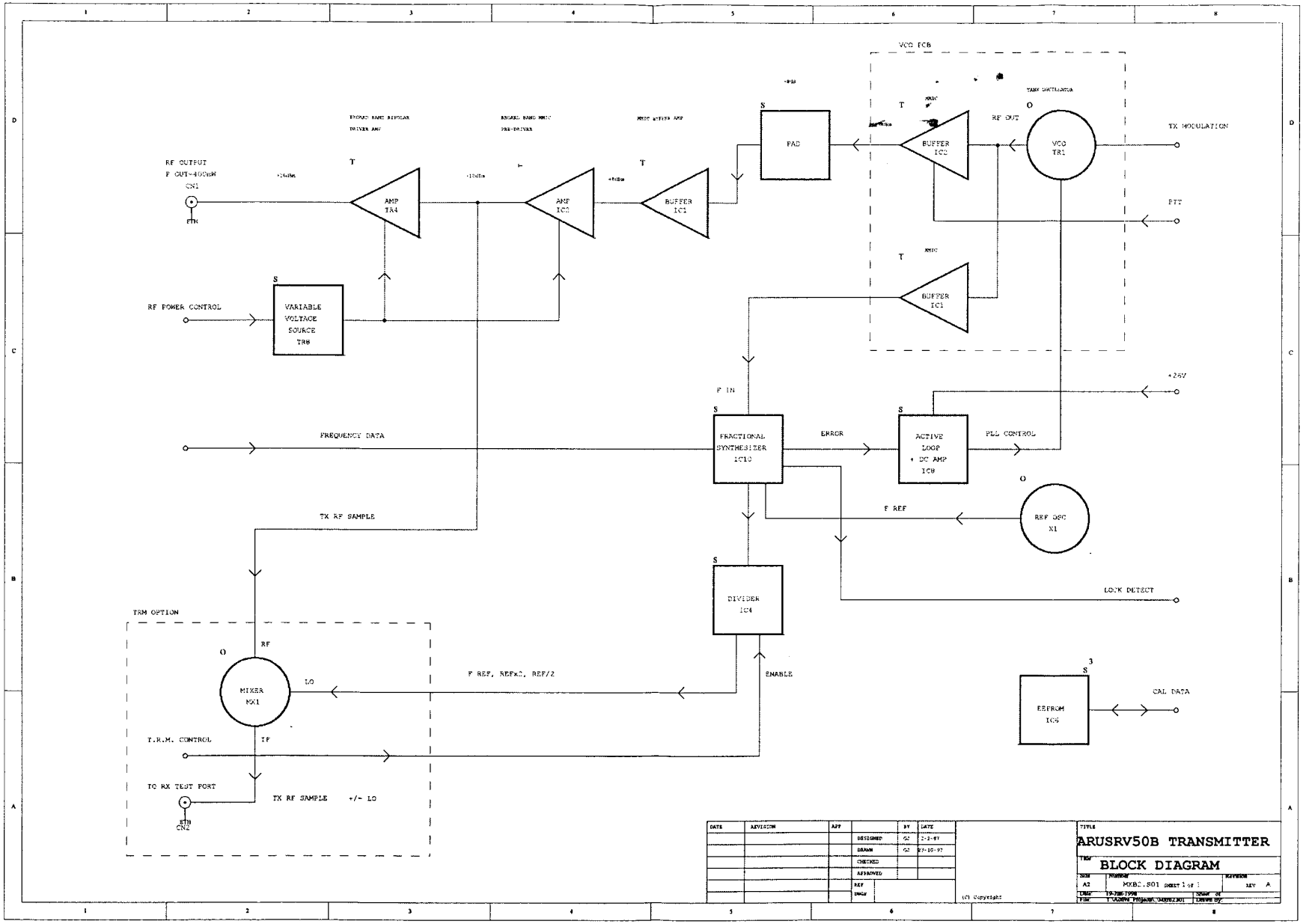
2.10.5 Figure 5. Conducted Emissions Test



2.10.6 Figure 6 This test set up was used to do the Transmitter Transient Behavior test




RF INPUT
CN1
RX TEST PORT
CN2
PRE-SET BANDPASS FILTER
RF AMP IC12
PAD
PRE-SET BANDPASS FILTER
MIXER M1
AMP IC4
PAD
BUFFER IC2
RF OUT
VCO TR1
VCO PCB
BUFFER IC1
RLC NETWORK
IF AMP TR2
IF AMP AND DISC CHIP
IC1
OSC
XTAL X1
MIXER
CRYSTAL FILTER FL4
IF AMP TR3
CRYSTAL FILTER FL3
CERAMIC FILTER FL5
CERAMIC FILTER FL6
AMP
LIMITER AND DISC
BUFFER
RSSI
BUFFER
VF
F IN
FRACTIONAL SYNTHESIZER IC10
ERROR
ACTIVE LOOP + DC AMP IC11
PLL CONTROL
+26V
LOCK DETECT
ENABLE
FREQUENCY DATA
EEPROM IC6
CAL DATA
REF OSC X2
ARUSRV50B RECEIVER
BLOCK DIAGRAM
MYB1.S01
(C) Copyright


VCO PCB
RF OUTPUT
F OUT=400MW
CN1
PTT
AMP
TR4
AMP
IC2
BUFFER
IC1
PAD
BUFFER
IC2
VCO
TR1
RF OUT
TX MODULATION
PTT
BUFFER
IC1
RF POWER CONTROL
VARIABLE
VOLTAGE
SOURCE
TR6
+24V
F IN
FREQUENCY DATA
FRACTIONAL
SYNTHESIZER
IC10
ERROR
ACTIVE
LOOP
+ DC AMP
IC8
PLL CONTROL
REF OSC
X1
F REF
TX RF SAMPLE
DIVIDER
IC4
LOCK DETECT
TRM OPTION
RF
MIXER
MX1
LO
F REF, REF*2, REF/2
ENABLE
EEPROM
IC5
CAL DATA
T.R.M. CONTROL
IF
TO RX TEST PORT
CN2
TX RF SAMPLE
+/- LO
(C) Copyright
ARUSRV50B TRANSMITTER
BLOCK DIAGRAM
DESIGNED
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CHECKED
APPROVED
MXBC.SCH SHEET 1 of 1
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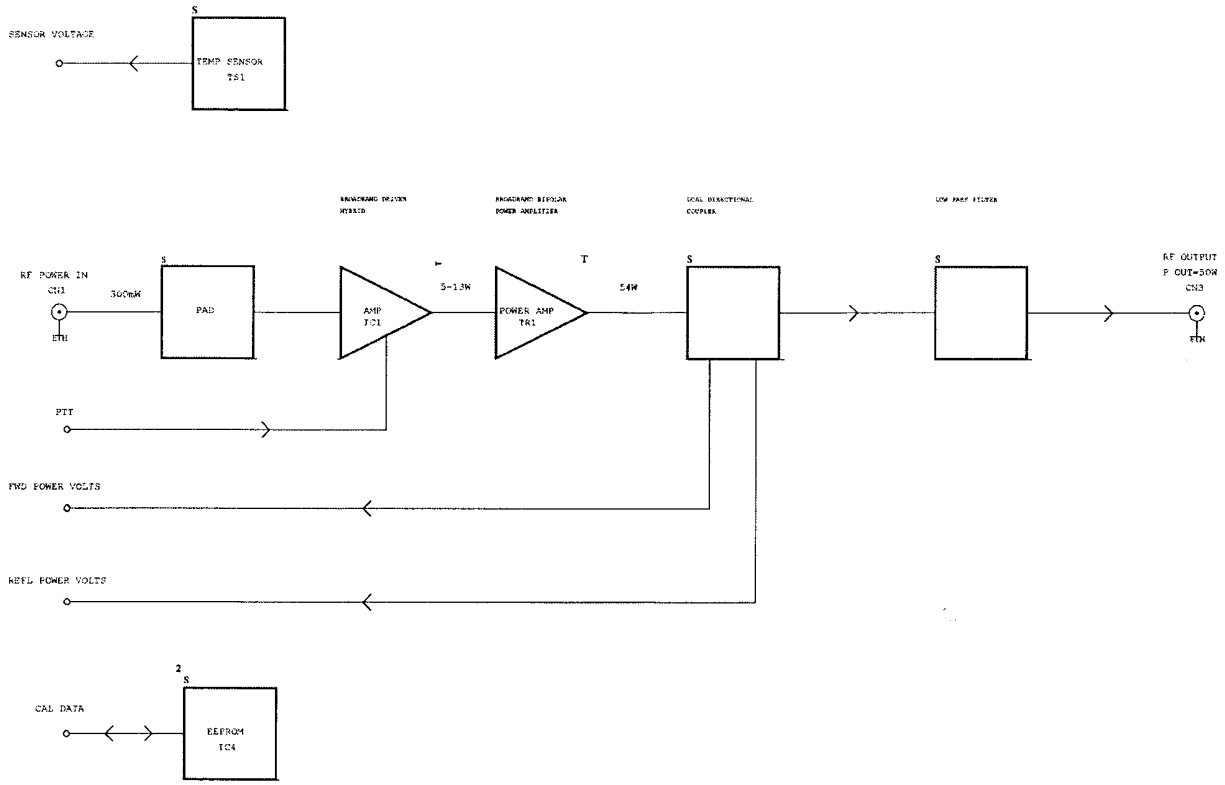

DATE	REVISION	APP		BY	DATE
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			DRAWN	GJ	23-10-97
			CHECKED		
			APPROVED		
			KEY DATE		

TITLE ARUSRV50B
POWER AMPLIFIER

TITLE BLOCK DIAGRAM

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