

# RPV599APlus Circuit Description

## 1. FREQUENCY CONFIGURATION

The receiver utilizes double conversion. The first IF is 45.05 MHz and the second IF is 455KHz. The first local oscillator signal comes from the PLL circuit.

The PLL circuit in the transmitter generates the necessary frequencies (See Fig.1).

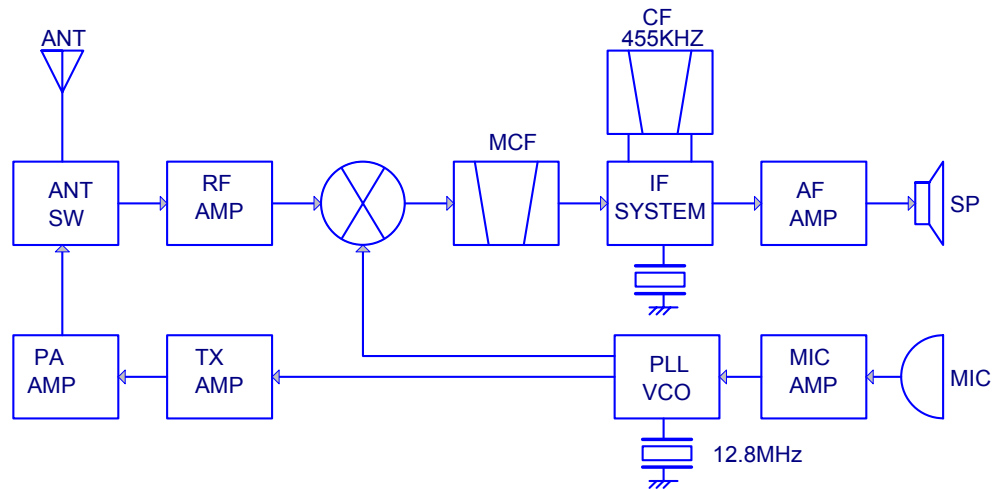


Fig.1

## 2. RECEIVER SYSTEM

The frequency configuration of the receiver is shown as following fig.2

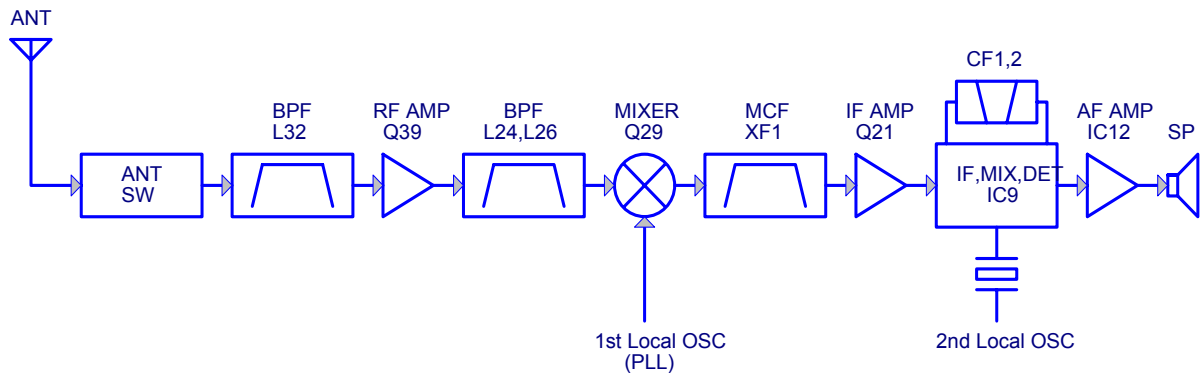


Fig.2

### 1) RF AMP

The signal coming from the antenna passes through the transmit/receive switching diode circuit, passes through a BPF [L32], and is amplified by the RF amplifier [Q39]. The resulting signal passes through a BPF [L26] and goes to the mixer.

### 2) First mixer

The signal from the front end is mixed with the first local oscillator signal generated in the PLL circuit by Q29 to produce a first IF frequency of 45.05 MHz.

The resulting signal passes through the XF1 MCF to cut the adjacent spurious and provide the optimum characteristics, such as adjacent frequency selectivity.

### 3) IF amplifier

The signal then passes through the first IF amplifier [Q21], and is amplified and goes to the IF IC (IC9). IC9 integrates the second OSC, second mixer, second IF amplifier, detector, noise amplifier, and noise detector.

The signal input to the IC is mixed with the RF signal of the second OSC to produce a 455KHz second IF signal. The signal is amplified by the IF amplifier. The signal is switched by Wide/Narrow switch diode and then passes through the ceramic filters (CF1 and CF2) to provide the necessary selectivity.

Finally, the signal is detected by the IC and output as an AF signal.

### 4) AF amplifier

The AF signal from the IF IC is amplified by IC8 (1/2) and passes through the high-pass filter (Q25 and Q28) to remove 300 Hz and lower frequencies to suppress the sub-audio signal.

The signal then passes through the de-emphasis circuit to restore the audio frequency characteristics. The signal passes through AF VOL and enters the IC12 audio power amplifier to drive the speaker. (See Fig.3)

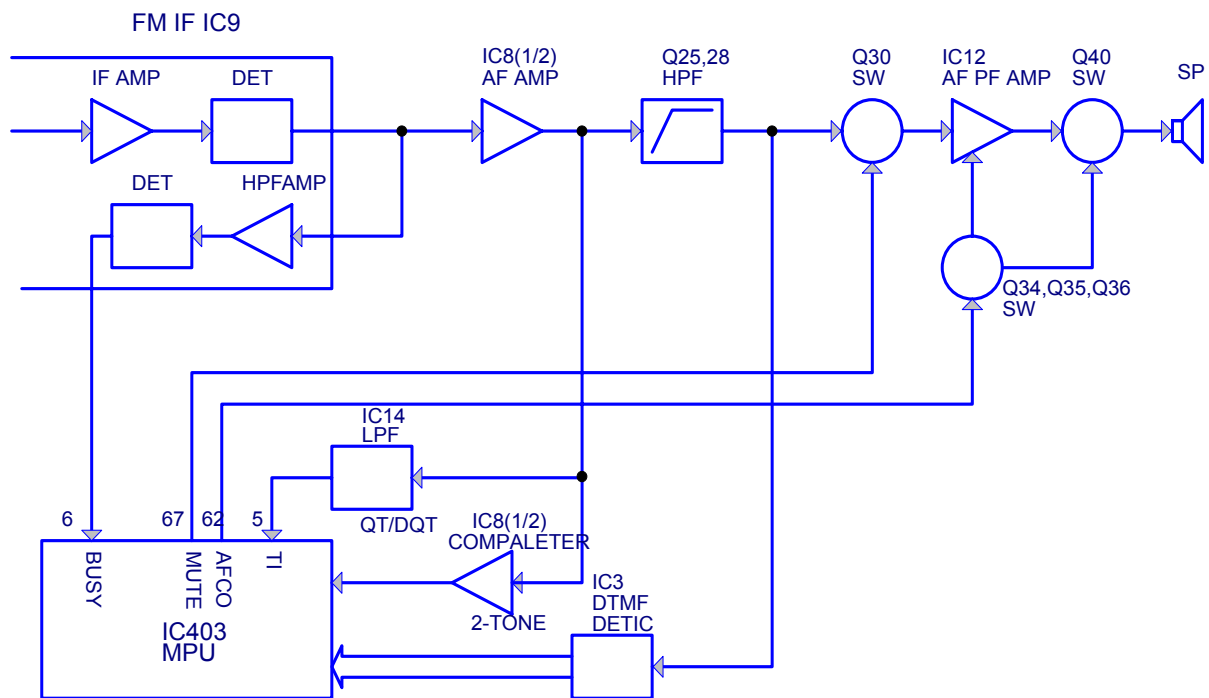


Fig.3

### 5) Squelch

Part of the AF signal from the IC enters the FM IC again, and the noise component is amplified and rectified by a filter and an amplifier to produce a DC voltage corresponding to the noise level.

The DC signal from the FM IC goes to the analog port of the microprocessor (IC1). IC1 determines whether to output sounds from the speaker by checking whether the input voltage is higher or lower than the preset value.

To output sounds from the speaker, IC1 sends a high level to the MUTE and AFCO lines and turns IC12 on through Q30, Q35, Q34, Q36 and Q40.

### 6) Receive signaling

#### (1) CTCSS

300Hz-and-higher audio frequencies of the signal output from IF IC are cut by a low-pass filter (IC14). The resulting signal enters the microprocessor (IC1). IC1 determines whether the CTCSS matches the preset value and controls the MUTE and AFCO and the speaker output sounds in line with the squelch results of that

content.

## (2) DTMF

The part of the received AF signal passes through a high-pass filter (Q25 and Q28) and goes to IC3.

IC3 detects a DTMF signal and sends received DTMF data to IC1. IC1 carries out various operations, such as sound output, according to the DTMF data. (See Fig.3)

## (3) 2-TONE

Part of the receive AF signal output from the AF amplifier (IC8 1/2) goes to the other IC8 (1/2), is compared, and goes to IC1. IC1 checks whether 2-TONE data is necessary. If it matches, IC1 carries out a specified operation, such as turning the speaker on.

## 3. PLL

The PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission.

### 1) PLL

The receiver has a VCO Q16, and the transmitter has another VCO (Q18).

The generated signal passes through the Q20 buffer and Q14 amplifier and enters the IC6 PLL IC. IC6 incorporates the reference oscillation divider and phase comparator functions. The input signal is divided into a 2.5 or 6.25KHz signal according to divide ratio data from the microcomputer (IC1). This signal and the 2.5 or 6.25KHz signal divided from the reference signal enter the phase comparator to produce a differential signal. The frequency control signal is output from the charge pump.

This signal passes through the passive LPF and goes to the varicap to control the VCO frequency (See Fig. 4).

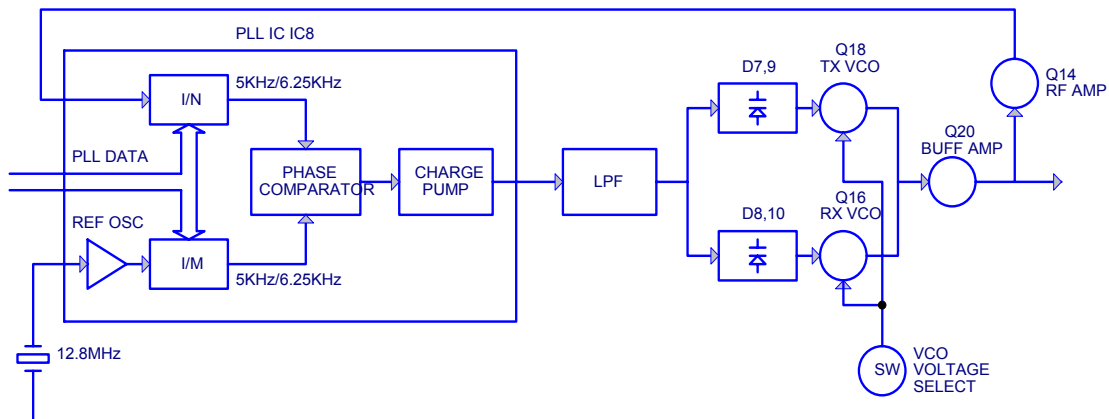


Fig.4

## 2) Reference Oscillator Circuit

The reference oscillator circuit in the PLL IC produces the 12.8MHz PLL reference frequency. To stabilize the frequency, the characteristics of the 12.8MHz crystal oscillator are controlled and the frequency is temperature-compensated.

It is compensated for by changing the DC voltage applied to D4. Changes in the ambient temperature are input to the analog port of IC1 using the TH3 thermistor. IC1 judges the temperature and outputs a voltage to the TC1, TC2, or TC3 port.

The temperature compensation value is corrected according to the differences in the characteristics of the thermistors in the TC1, TC2, and TC3 circuits. The temperature compensation is carried out when the temperature is -10°C or less. (See Fig.5)

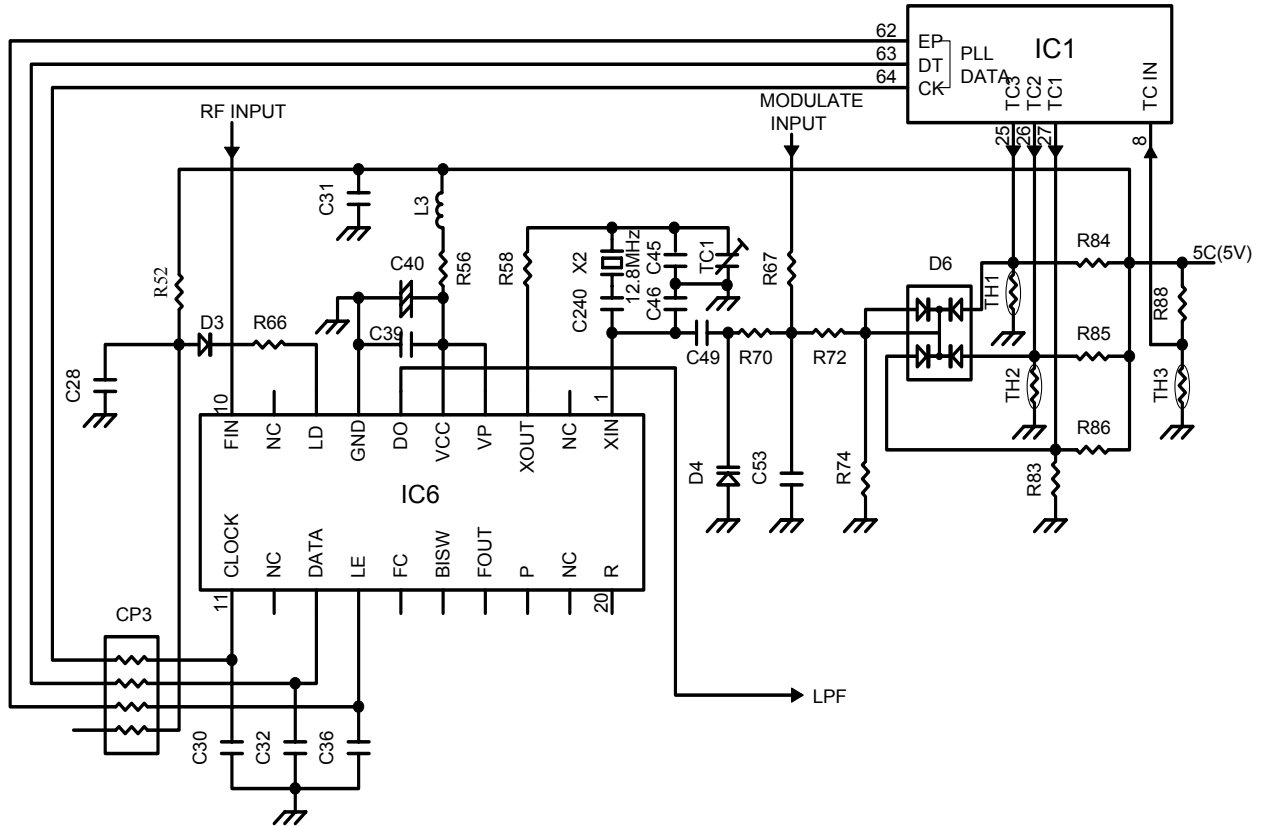


Fig.5

#### 4. TRANSMITTER

##### 1) Transmit audio

The modulation signal from the microphone is amplified by IC10 (1/2), passes through a pre-emphasis circuit, and is amplified by the other IC10 (1/2) to perform IDC operation.

The signal then passes through a low-pass filter (splatter filter) Q22 and Q17, and cuts 3 KHz and higher frequencies. The resulting signal goes to the VCO through the VCO modulation terminal for direct FM modulation.

##### 2) CTCSS encoder

A necessary signal for CTCSS encoding is generated by IC1 and is FM-modulated to the PLL reference signal. Since the reference OSC does not modulate the loop characteristic frequency or higher, modulation is performed at the VCO side by adjusting the balance.

##### 3) DTMF

The DTMF encode signal is also generated by IC1. This signal goes to IC10, and follows the same route as for ordinary modulation.

Q32 and Q37 mute the microphone line when sending the DTMF to prevent a malfunction resulting from audio signals (See Fig.6)

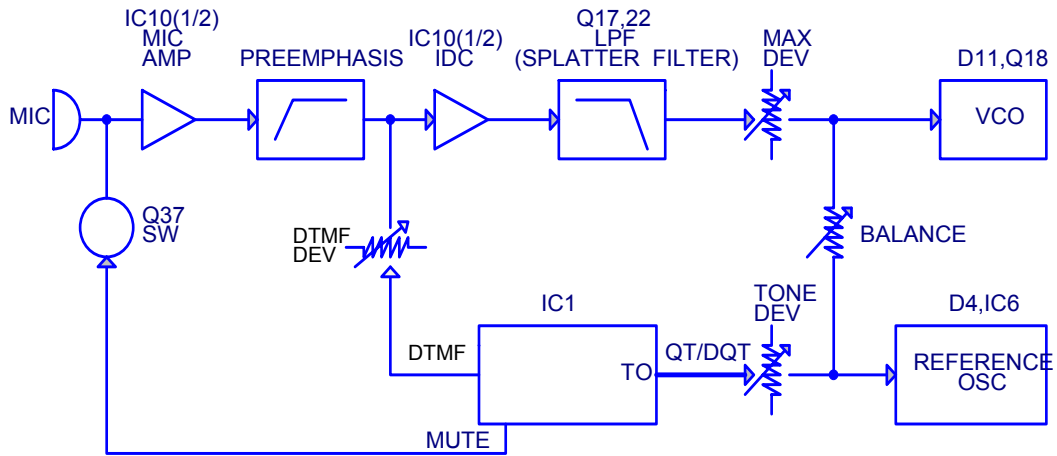


Fig.6

#### 4) VCO and RF amplifier

The modulation signal is modulated to VCO by D11. The RF signal from the PLL is amplified by Q26 and Q31 to the sufficient level to drive the power module.

#### 5) Final module

The MOS FET-type power module (IC11) is used to amplify the transmission power.

#### 6) ANT switch and LPF

The signal from the module passes through the D22 SW and L31 LPF and is output from the ANT terminal. D17 and D16 are used to switch between transmission and reception. The chip-type LPF is used to provide required attenuation.

#### 7) APC

The APC keeps the current constant to the final module. The current to the final module is output as a voltage by detecting the potential difference between R215, R217 and R218 by IC13 (1/2). IC13 (1/2) compares the signal with the APC voltage from IC1 and controls the voltage so that they have the same value. The output becomes the IC11 power control voltage, and the current is kept constant in this loop.

The APC voltage from IC1 has the preset high or low power level. (See Fig.7)

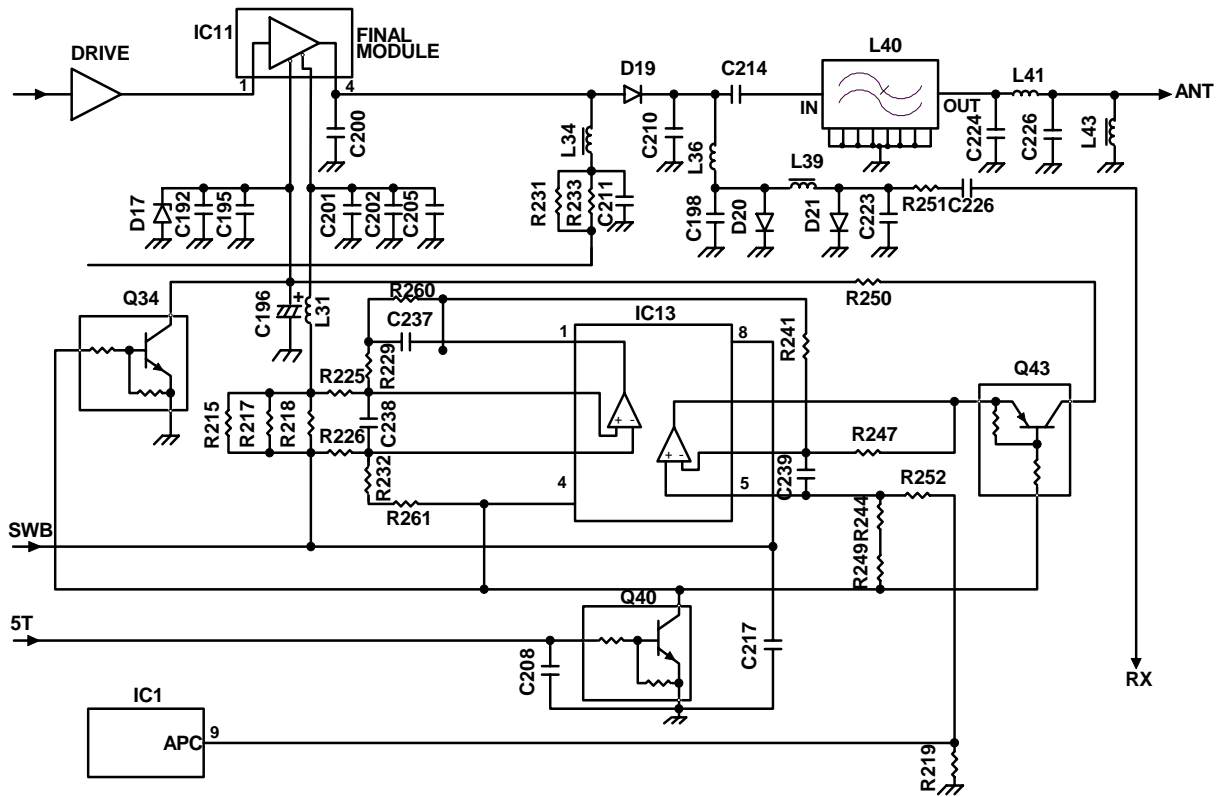


Fig. 7

## 5. POWER SUPPLY

There are four 5V power supplies for the microcomputer: 5V, 5C, 5R, and 5T. 5V for the microcomputer is always output while the power is on.

5C is common 5V and is output when SAVE is not set at OFF.

5R is 5V for reception and is output during reception.

5T is 5V for transmission and is output during transmission.

## 6. CONTROL SYSTEM

The IC1 CPU operates at 8.38-MHz clocks. This oscillator has a circuit that shifts the frequency according to EEPROM data.

IC1 controls the LCD driver and keys.

Key and rotary encoder circuit is shown as fig.8. The signal from keys and rotary encoder is input to microprocessor directly. (See Fig.8)

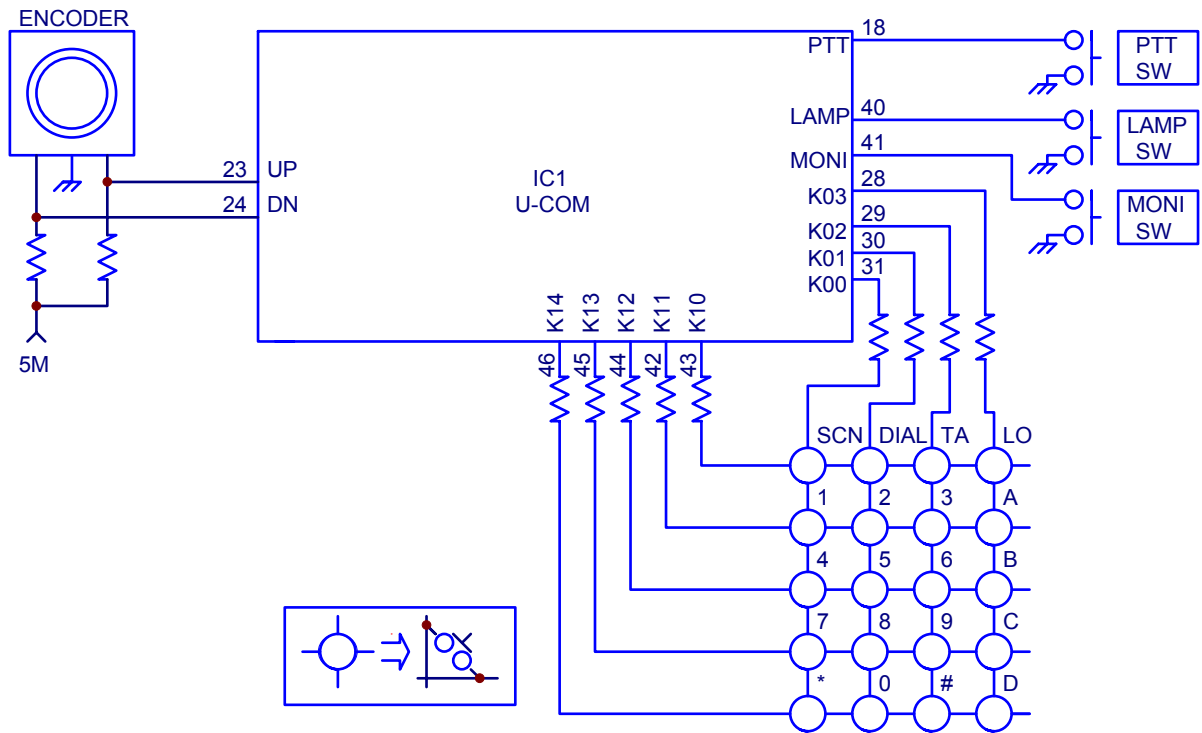


Fig. 8

# RPU499APlus Circuit Description

## 1. FREQUENCY CONFIGURATION

The receiver utilizes double conversion. The first IF is 45.05 MHz and the second IF is 455KHz. The first local oscillator signal comes from the PLL circuit.

The PLL circuit in the transmitter generates the necessary frequencies (See Fig.1).

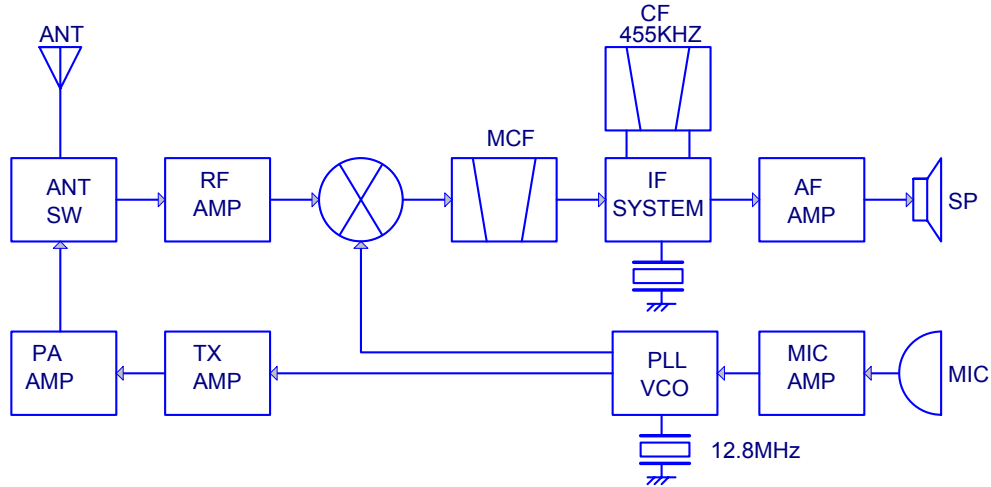


Fig.1

## 2. RECEIVER SYSTEM

The frequency configuration of the receiver is shown following fig.2

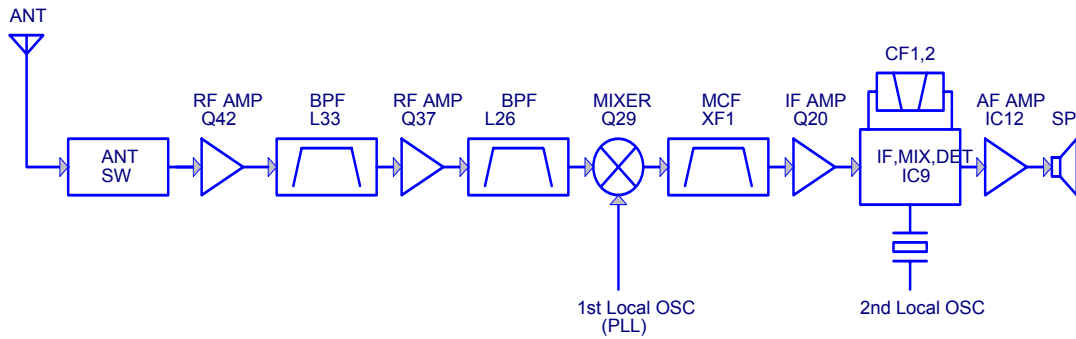


Fig.2

### 1) RF AMP

The signal coming from the antenna passes through the transmit/receive switching diode circuit, amplified by Q42 and then passes through a BPF [L33], and is amplified by the RF amplifier [Q37]. The resulting signal passes through a BPF [L26] and goes to the mixer.

### 2) First mixer

The signal from the front end is mixed with the first local oscillator signal generated in the PLL circuit by Q29 to produce a first IF frequency of 45.05 MHz.

The resulting signal passes through the XF1 MCF to cut the adjacent spurious and provide the optimum characteristics, such as adjacent frequency selectivity.



### 3) IF amplifier

The signal then passes through the first IF amplifier [Q20], and is amplified and goes to the IF IC (IC9). IC9 integrates the second OSC, second mixer, second IF amplifier, detector, noise amplifier, and noise detector.

The signal input to the IC is mixed with the RF signal of the second OSC to produce a 455KHz second IF signal. The signal is amplified by the IF amplifier. The signal is switched by Wide/Narrow switch diode and then passes through the ceramic filters (CF1 and CF2) to provide the necessary selectivity.

Finally, the signal is detected by the IC and output as an AF signal.

### 4) AF amplifier

The AF signal from the IF IC is amplified by IC8 (1/2) and passes through the high-pass filter (Q25 and Q28) to remove 300 Hz and lower frequencies to suppress the sub-audio signal.

The signal then passes through the de-emphasis circuit to restore the audio frequency characteristics. The signal passes through AF VOL and enters the IC12 audio power amplifier to drive the speaker. (See Fig.3)

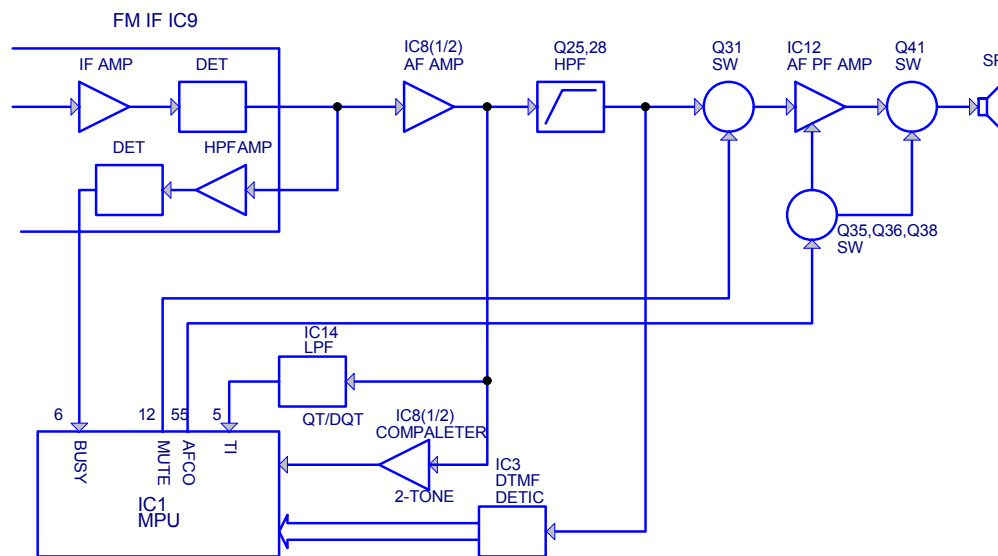


Fig.3

### 5) Squelch

Part of the AF signal from the IC enters the FM IC again, and the noise component is amplified and rectified by a filter and an amplifier to produce a DC voltage corresponding to the noise level.

The DC signal from the FM IC goes to the analog port of the microprocessor (IC1). IC1 determines whether to output sounds from the speaker by checking whether the input voltage is higher or lower than the preset value.

To output sounds from the speaker, IC1 sends a high level to the MUTE and AFCO lines and turns IC12 on through Q31, Q35, Q36, Q38 and Q41.

### 6) Receive signaling

#### (1) CTCSS

300Hz-and-higher audio frequencies of the signal output from IF IC are cut by a low-pass filter (IC14). The resulting signal enters the microprocessor (IC1). IC1 determines whether the CTCSS matches the preset value and controls the MUTE and AFCO and the speaker output sounds in line with the squelch results of that content.

#### (2) DTMF

The part of the received AF signal passes through a high-pass filter (Q25 and Q28) and goes to IC3.

IC3 detects a DTMF signal and sends received DTMF data to IC1. IC1 carries out various operations, such as sound output, according to the DTMF data. (See Fig.3)

**(3) 2-TONE**

Part of the receive AF signal output from the AF amplifier (IC8 1/2) goes to the other IC8 (1/2), is compared, and goes to IC1. IC1 checks whether 2-TONE data is necessary. If it matches, IC1 carries out a specified operation, such as turning the speaker on.

**3. PLL**

The PLL circuit generates the first local oscillator signal for reception and the RF signal for transmission.

**1) PLL**

The receiver has a VCO Q15, and the transmitter has another VCO (Q18).

The generated signal passes through the Q21 buffer and Q14 amplifier and enters the IC6 PLL IC. IC6 incorporates the reference oscillation divider and phase comparator functions. The input signal is divided into a 2.5 or 6.25KHz signal according to divide ratio data from the microcomputer (IC1). This signal and the 2.5 or 6.25KHz signal divided from the reference signal enter the phase comparator to produce a differential signal. The frequency control signal is output from the charge pump.

This signal passes through the passive LPF and goes to the varicap to control the VCO frequency (See Fig. 4).

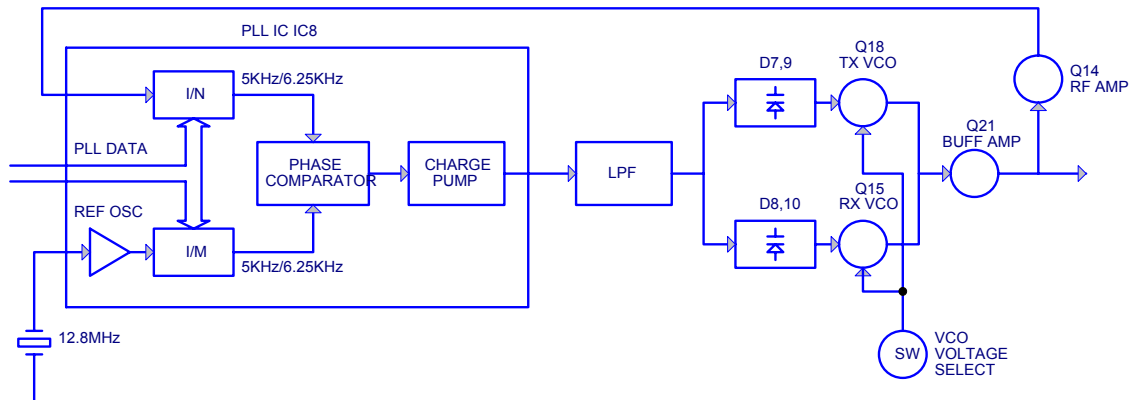


Fig.4

**2) Reference Oscillator Circuit**

The reference oscillator circuit in the PLL IC produces the 12.8MHz PLL reference frequency. To stabilize the frequency, the characteristics of the 12.8MHz crystal oscillator are controlled and the frequency is temperature-compensated.

It is compensated for by changing the DC voltage applied to D4. Changes in the ambient temperature are input to the analog port of IC1 using the TH3 thermistor. IC1 judges the temperature and outputs a voltage to the TC1, TC2, or TC3 port.

The temperature compensation value is corrected according to the differences in the characteristics of the thermistors in the TC1, TC2, and TC3 circuits. The temperature compensation is carried out when the temperature is  $-10^{\circ}\text{C}$  or less. (See Fig.5)

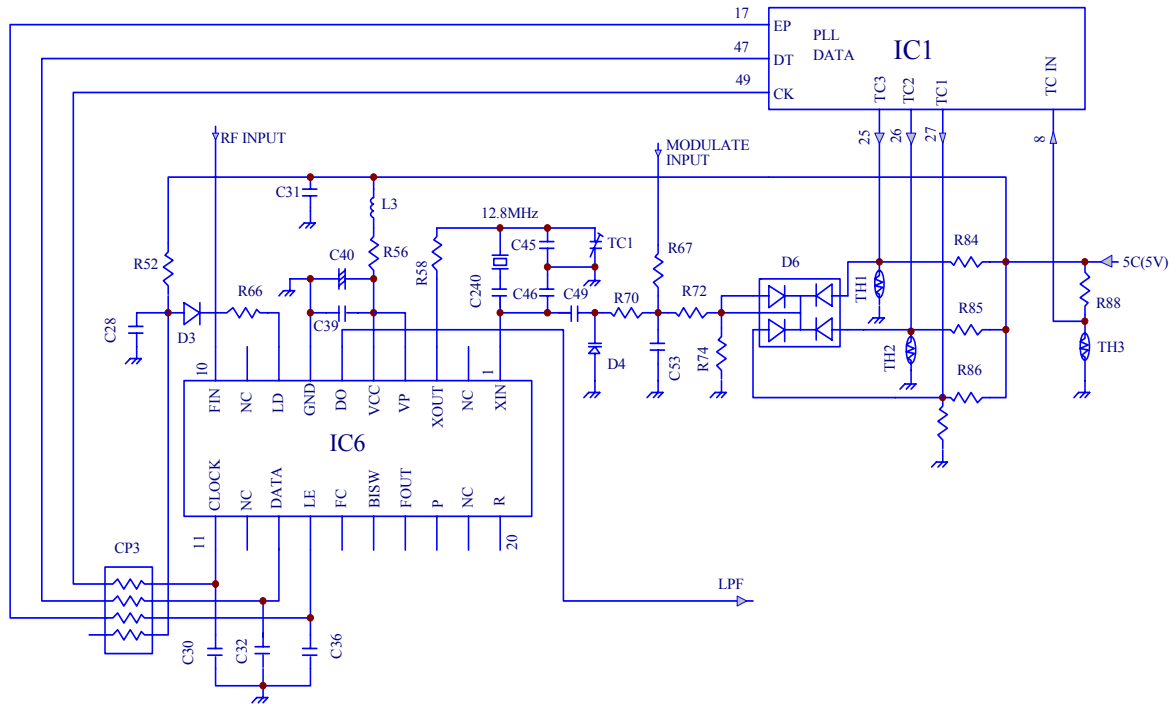


Fig.5

#### 4. TRANSMITTER

##### 1) Transmit audio

The modulation signal from the microphone is amplified by IC10 (1/2), passes through a pre-emphasis circuit, and is amplified by the other IC10 (1/2) to perform IDC operation.

The signal then passes through a low-pass filter (splatter filter) Q22 and Q16, and cuts 3 KHz and higher frequencies. The resulting signal goes to the VCO through the VCO modulation terminal for direct FM modulation.

##### 2) CTCSS encoder

A necessary signal for CTCSS encoding is generated by IC1 and is FM-modulated to the PLL reference signal. Since the reference OSC does not modulate the loop characteristic frequency or higher, modulation is performed at the VCO side by adjusting the balance.

##### 3) DTMF

The DTMF encode signal is also generated by IC1. This signal goes to IC10, and follows the same route as for ordinary modulation.

Q39 mutes the microphone line when sending the DTMF to prevent a malfunction resulting from audio signals. (See Fig.6)

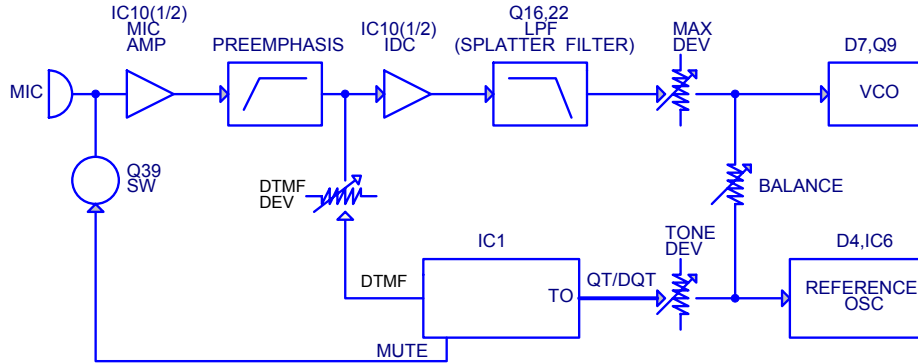


Fig.6

#### 4) VCO and RF amplifier

The modulation signal is modulated to VCO by D11. The RF signal from the PLL is amplified by Q30 and Q32 to the sufficient level to drive the power module.

#### 5) Final module

The MOS FET-type power module (IC11) is used to amplify the transmission power.

#### 6) ANT switch and LPF

The signal from the module passes through the D19 SW and L40 LPF and is output from the ANT terminal. D15 and D14 are used to switch between transmission and reception. The chip-type LPF is used to provide required attenuation.

#### 7) APC

The APC keeps the current constant to the final module. The current to the final module is output as a voltage by detecting the potential difference between R218, R220 and R223 by IC13 (1/2). IC13 (1/2) compares the signal with the APC voltage from IC1 and controls the voltage so that they have the same value. The output becomes the IC11 power control voltage, and the current is kept constant in this loop.

The APC voltage from IC1 has the preset high or low power level. (See Fig.7)

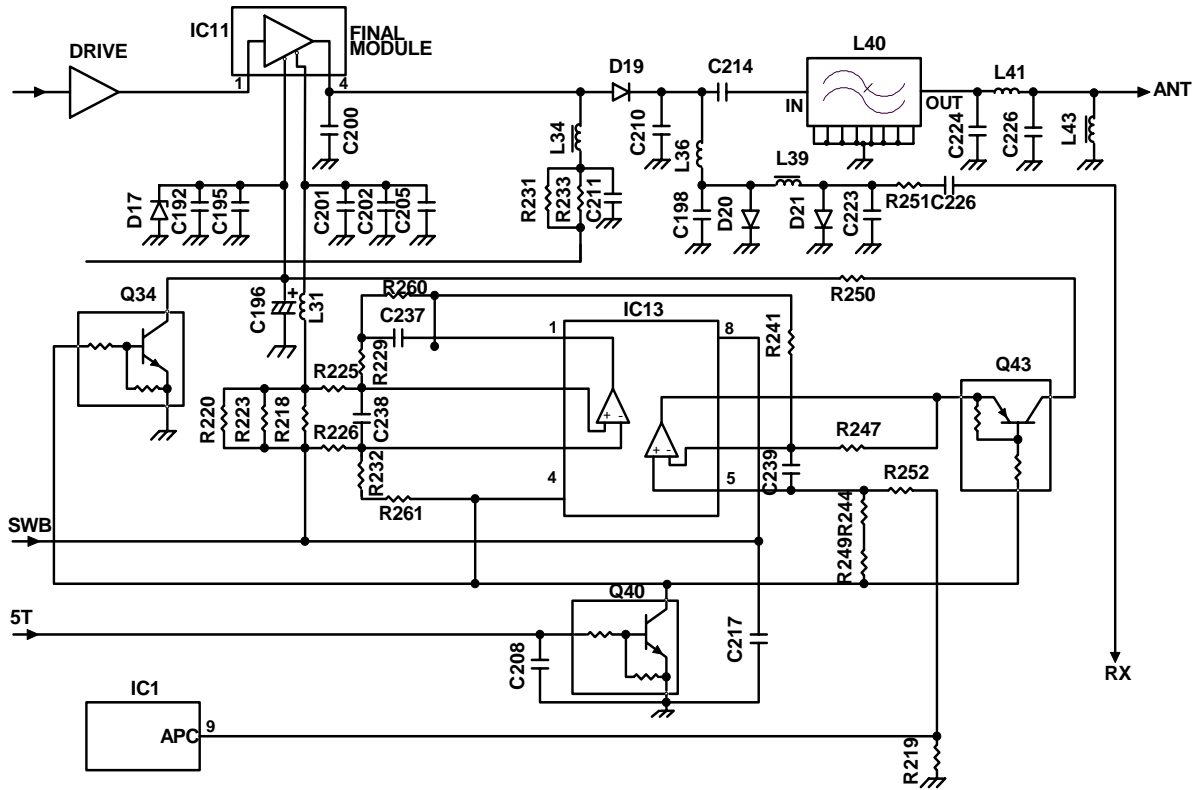


Fig. 7

## 5. POWER SUPPLY

There are four 5V power supplies for the microcomputer: 5V, 5C, 5R, and 5T. 5V for the microcomputer is always output while the power is on.

5C is common 5V and is output when SAVE is not set at OFF.

5R is 5V for reception and is output during reception.

5T is 5V for transmission and is output during transmission.

## 6. CONTROL SYSTEM

The IC1 CPU operates at 8.38MHz clocks. This oscillator has a circuit that shifts the frequency according to EEPROM data.

IC1 controls the LCD driver and keys.

Key and rotary encoder circuit is shown as fig. 8.

The signal from keys and rotary encoder is input to microprocessor directly. (See Fig.8)

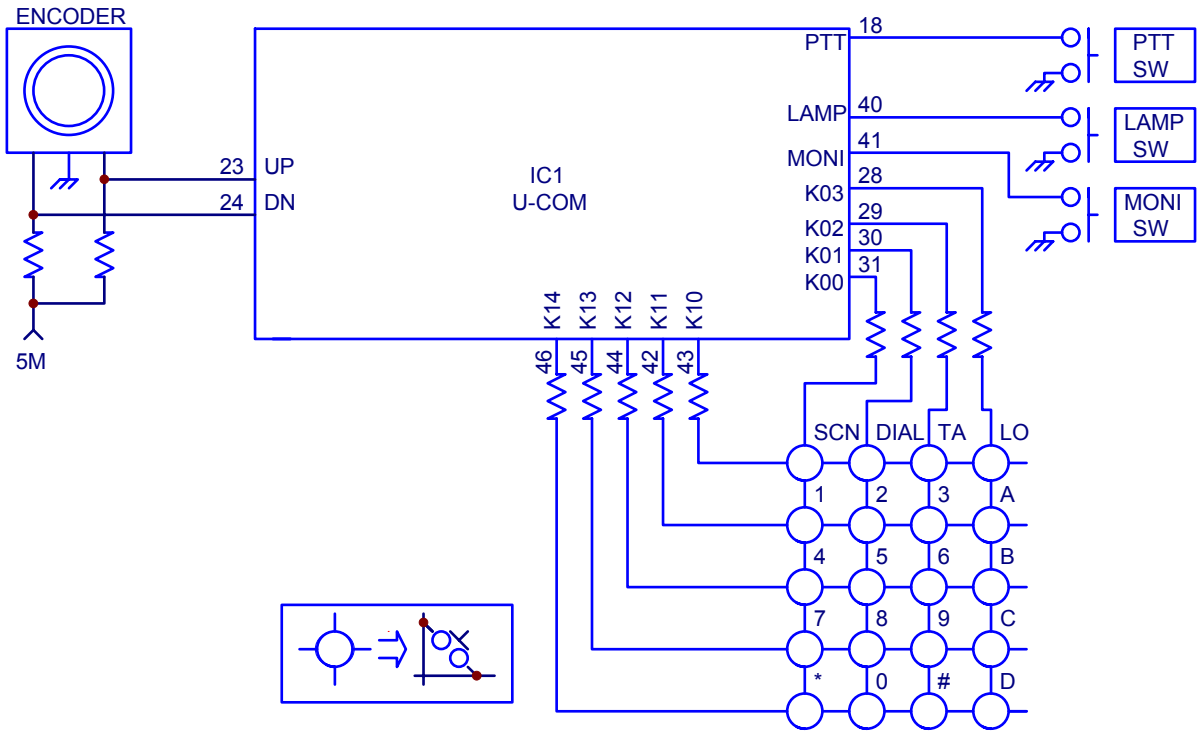


Fig. 8