

Legend Eagle 17" (gm2121) LCD CONTROLLER BOARD SCHEMATICS


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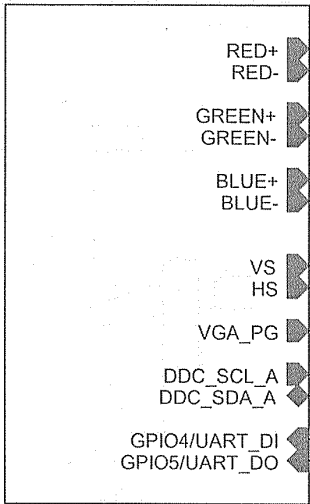
REVISION HISTORY

Date	Author	Ver	Comments
5/6/03	Rick	A	A. 依聯想要求, 修正Connector B. 由於有共用問題, 將另建料號
5/19/03	Rick	B	A. Inverter控制訊號反向 B. LED控制訊號反向

Approval	Organization	Signature	Date

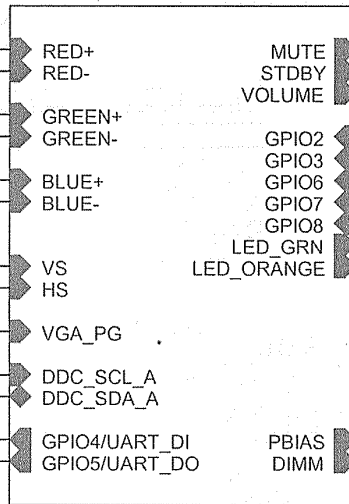
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	Size A	Document Number EAGLE17-715L1130-B-LEG.DSN
	Date: Monday, May 19, 2003	Rev B

SHEET 2



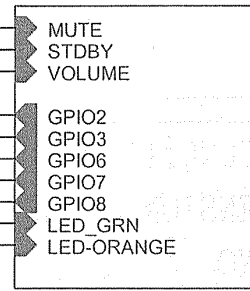
2.Signal Input

SHEET3



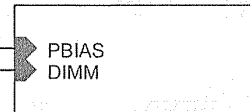
3.GM2121

SHEET 4



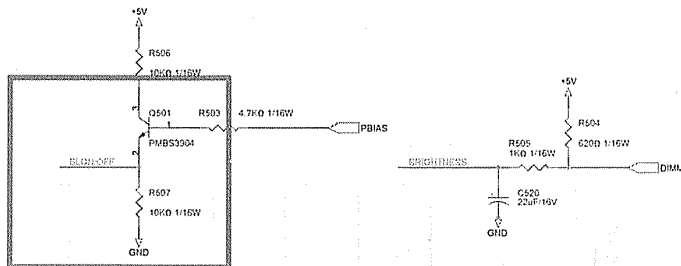
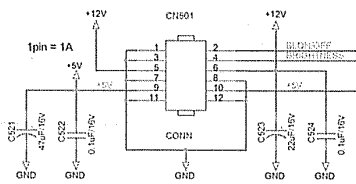
4.I/O Connectors

SHEET 5

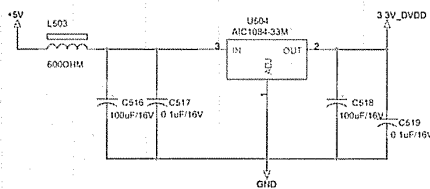
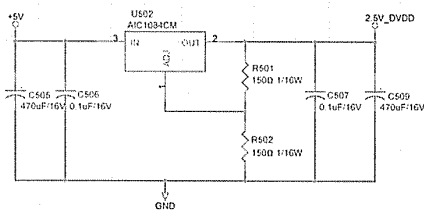
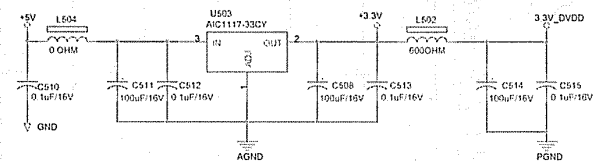
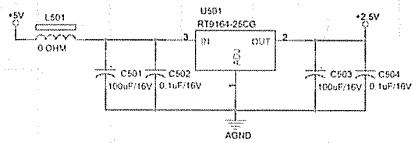


5.Power

	Title		1.Top Level	
	Size	Document Number		Rev
	Custom	EAGLE17-715L1130-B-LEG.DSN		B
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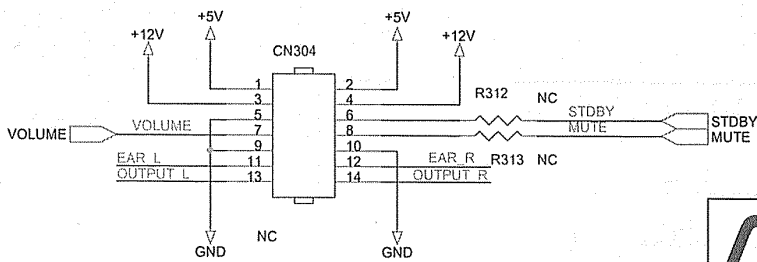
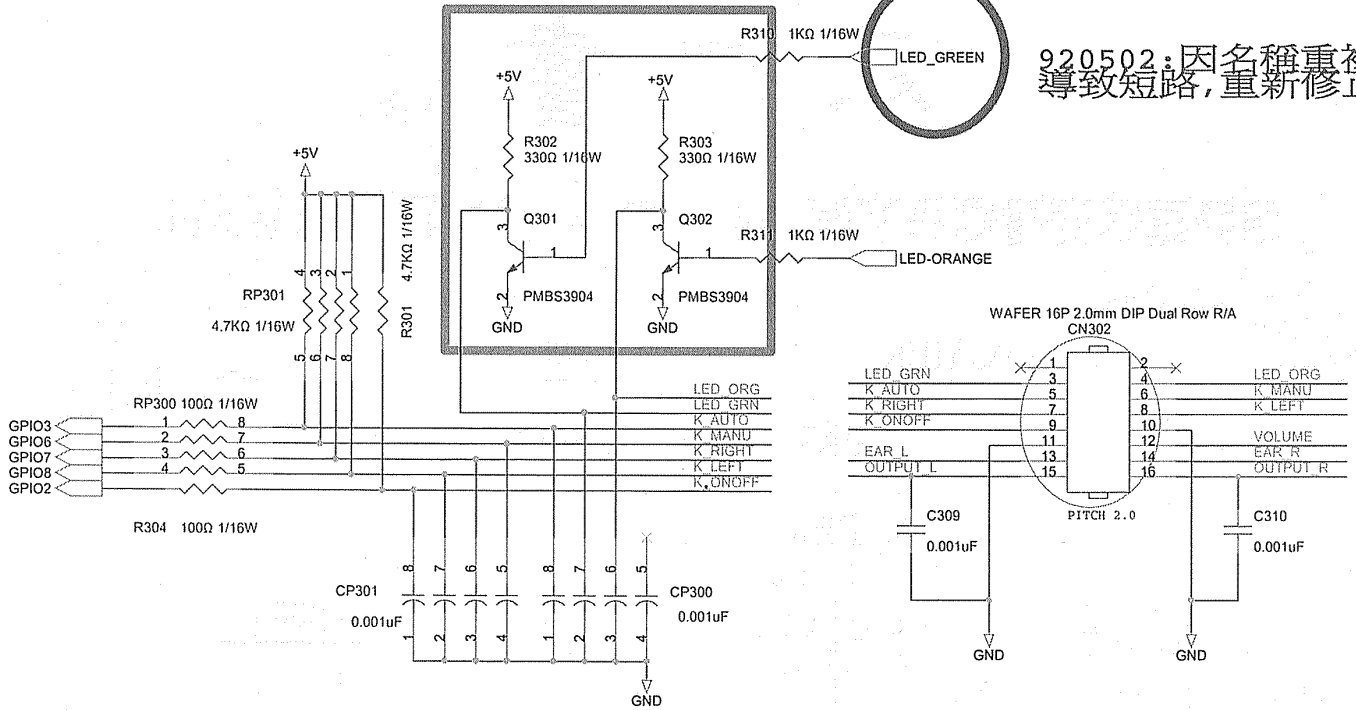
920519: Inverter 訊號腳反向



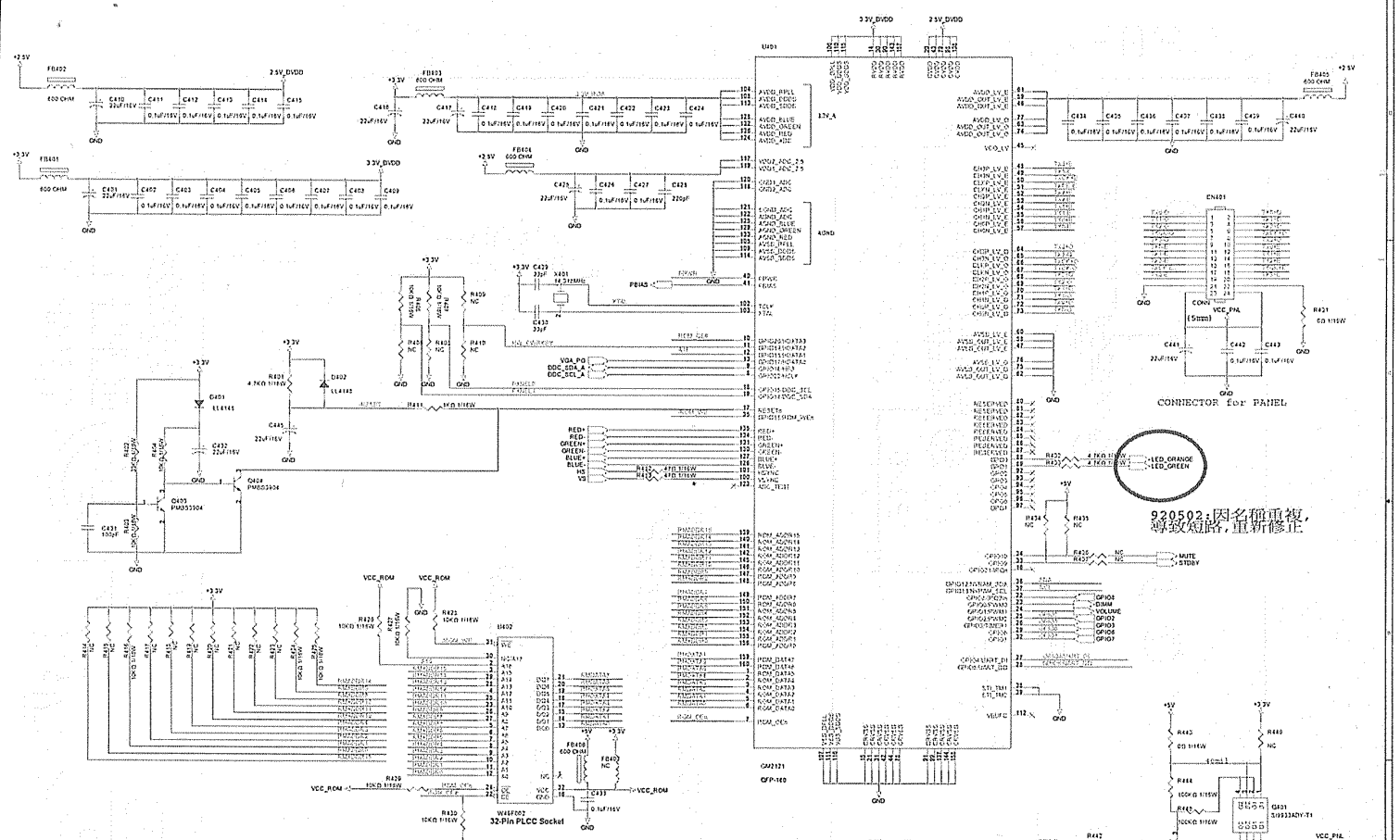
	Title	5.Power	Rev. 0
	Doc. No.	EAGLE17-71SL1130-B-LEG.DSN	
	Date	Monday, May 28, 2003	
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920519: LED訊號腳反向

920502: 因名稱重複, 導致短路, 重新修正



		Title: 4.I/O Connectors	
Size: A	Document Number: EAGLE17-715L1130-B-LEG.DSN		Rev: B
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BOOTSTRAP SIGNALS

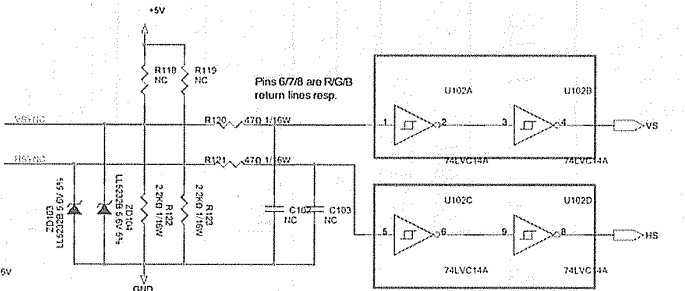
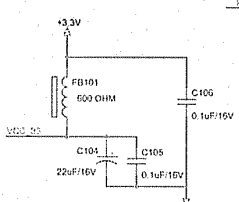
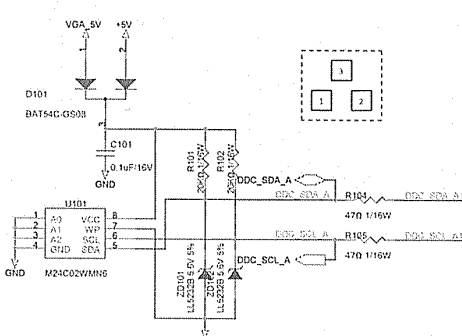
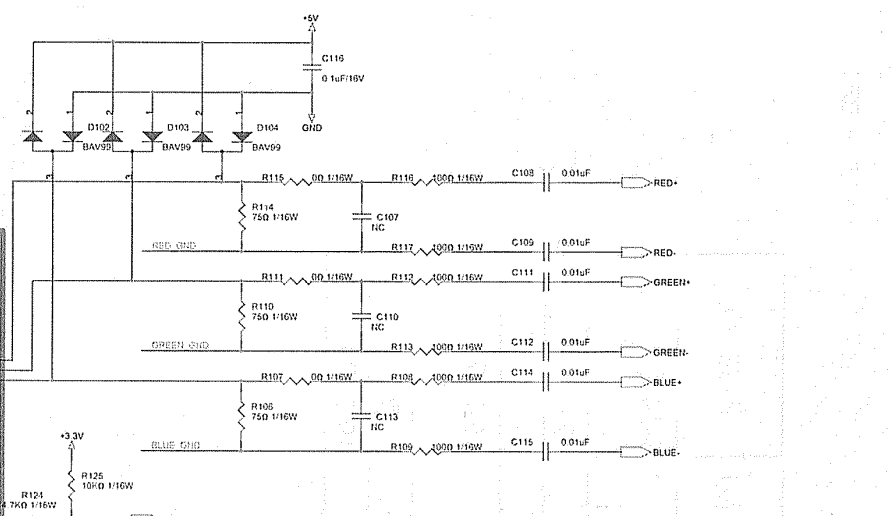
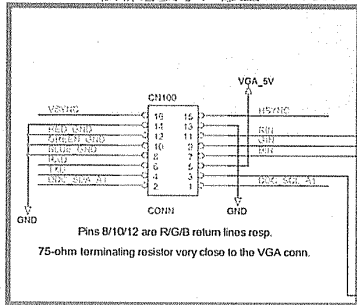
ADDRESS	NAME	SET	DESCRIPTION
ROM_ADDR(4)	USER_BIT(4)	X	Available for reading from status register
ROM_ADDR(5)	Reserved	X	If using 6-wire host protocol, program the bit to 1
ROM_ADDR(6)	SELROL	X	Diagnoses parity of HCLK supply
ROM_ADDR(7)	HOST_PROTOCOL	0	If using 6-wire host protocol, program this bit to 1
ROM_ADDR(8)	HOST_PORT_EN	1	GPIO(22) to 8 on "Host Port" pins
ROM_ADDR(9)	OCM_START	1	1 = OCM (OCM mode) active after OCM_CLK is stable
ROM_ADDR(12-13)	USER_BIT(2)	X	Available for reading from status register
ROM_ADDR(14)	OSC_SEL	0	0 = XTAL and TCLK pins are connected
ROM_ADDR(14)	OCM_ROM_Clock	1	1 = At 48KHz ROM is in memory ROM

920502:因名稱重複,
導致短路,重新修正

AOC 3.GM2121
 Eagle17-7151110-B-LEG.DSN
 Rev B

GPIO4UART_D0 R124 470 1/16W R219
 GPIO4UART_DI R103 470 1/16W R213

920507: 依聯想要求, 修正Connector



AOC EYE VALUE		File 2.Signal Input		Rev B
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