

Legend GM2115 LCD CONTROLLER BOARD SCHEMATICS


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REVISION HISTORY

Date	Author	Ver	Comments
5/13/03	Rick	A	
5/19/03	Rick	B	A. LED控制訊號反向 B. 7414 Power & Ground 未連線

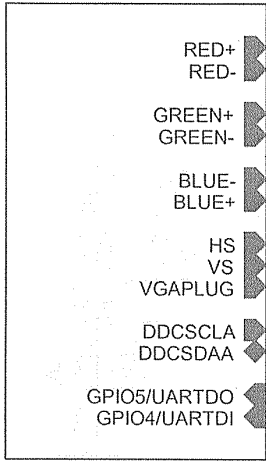
Approval	Organization	Signature	Date

	Title 01. Contents		
	Size A	Document Number 715L1129-B-LE2.DSN	Rev B
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SHEET 3

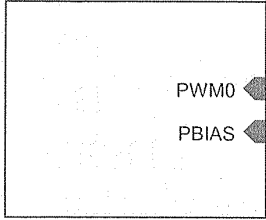
SHEET 4

SHEET 5

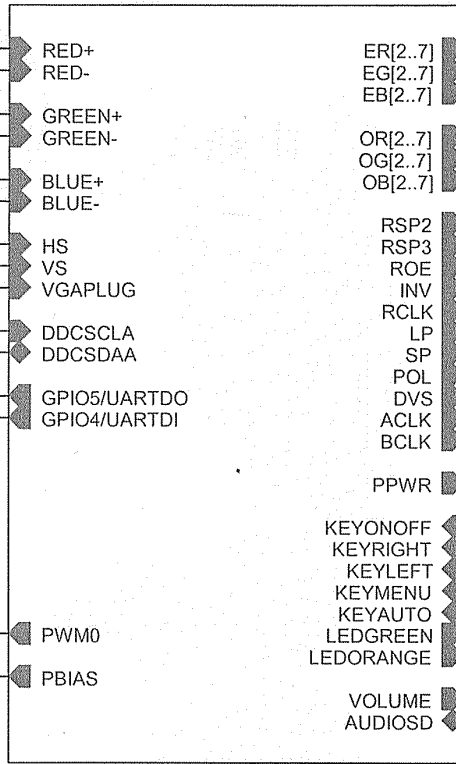


03. Analog Connectors

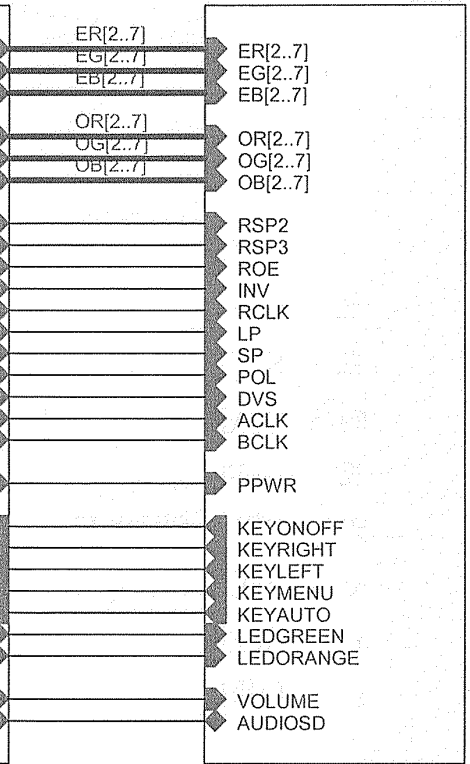
SHEET 6



06. Board Power Supply



04. Gm2115

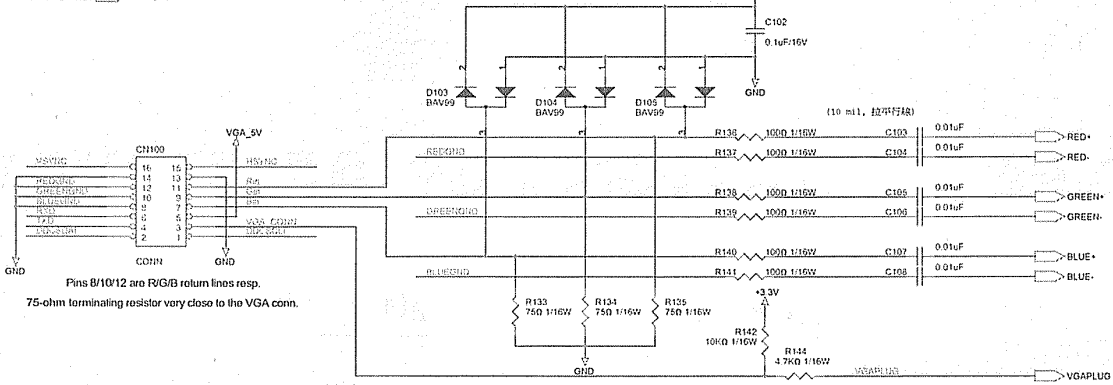


05. Display Interface

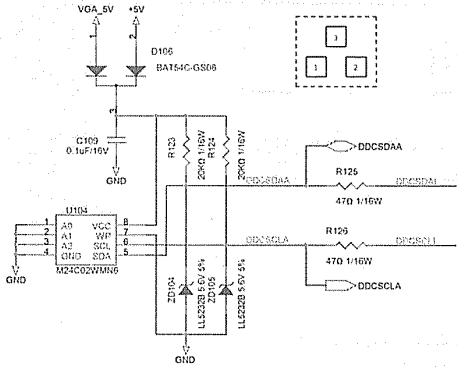


Title		02. Top Level	
Size	Document Number	Rev	
Custom	715L1129-B-LE2.DSN	B	
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GPIO4UARTD0 R104 470 1/16W 12D
 GPIO4UARTD1 R105 470 1/16W 12D

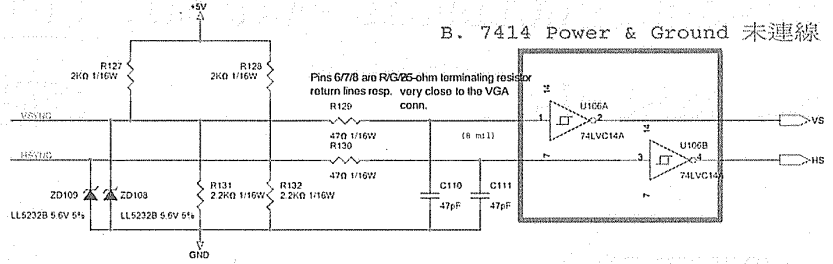


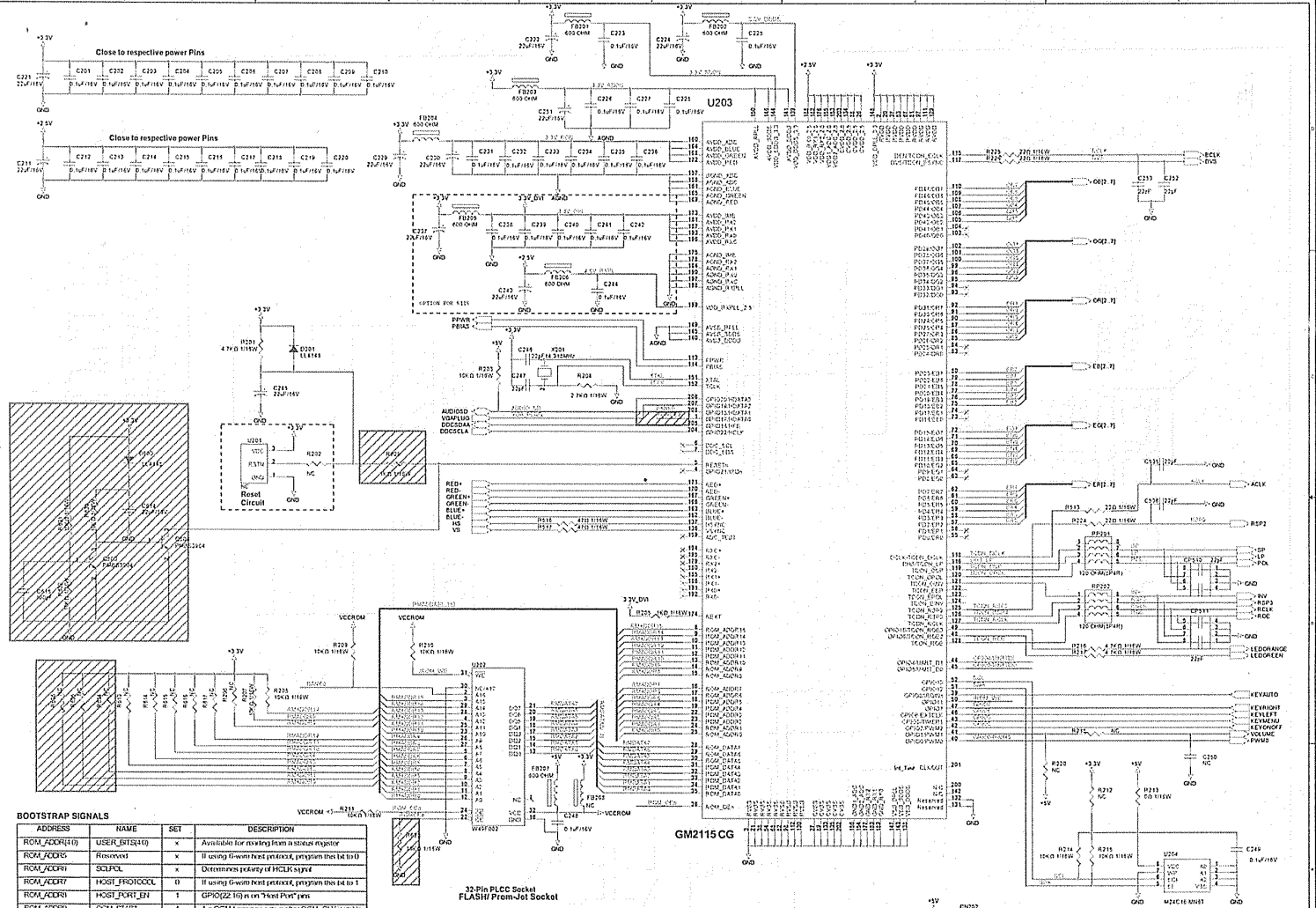
Pins 8/10/12 are R/G/B return lines resp.
 75-ohm terminating resistor very close to the VGA conn.



Pins 6/7/8 are R/G/B 75-ohm terminating resistor
 return lines resp. very close to the VGA
 conn.

B. 7414 Power & Ground 未連線

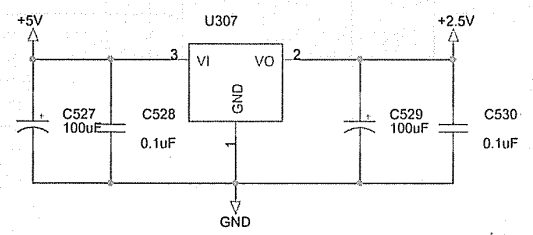
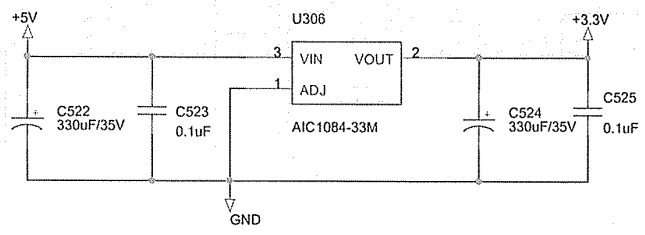
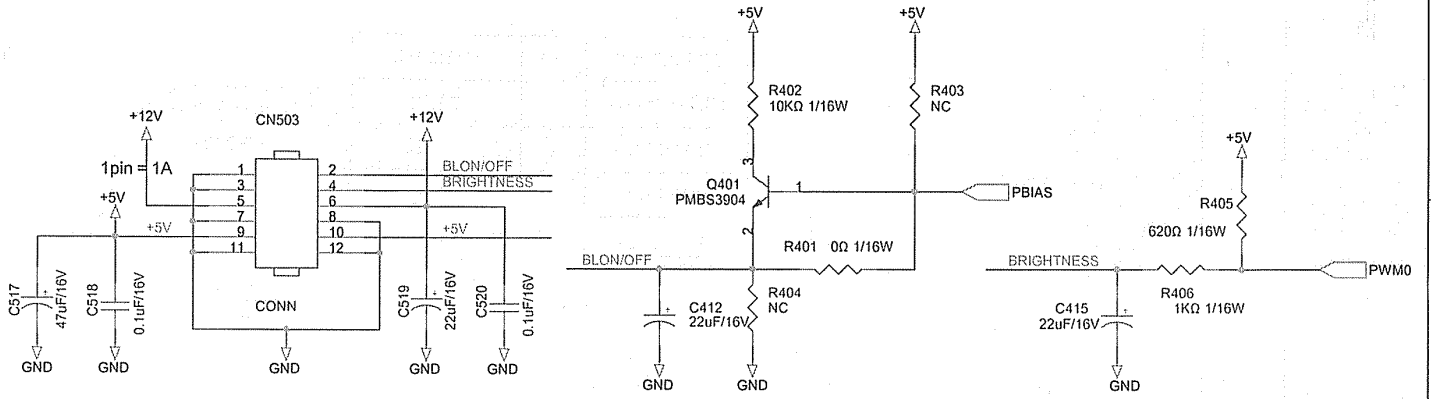




BOOTSTRAP SIGNALS

ADDRESS	NAME	SET	DESCRIPTION
ROM_ADDR(10)	USER_BITS(10)	x	Available for moving from a status register
ROM_ADDR(5)	Reserved	x	If using 64-word flash, pins 6-10 program lines (6-10)
ROM_ADDR(8)	SELPOL	x	Determines polarity of HCLK signal
ROM_ADDR(7)	H0ST_PORT00L	0	If using 64-word flash, pins 7-10 program lines (4-7)
ROM_ADDR(8)	H0ST_PORT_EN	1	GPIO(22) is an "Host Port" pin
ROM_ADDR(9)	OCM_START	1	1 = OCM becomes active after OCM_CLR is set(4)
ROM_ADDR(12-10)	USER_BITS(7-5)	x	Available for moving from a status register
ROM_ADDR(1)	OSSC_SEL	0	0 = XTAL and TCCLK pins are connected
ROM_ADDR(1)	OCM_ROM_LPC(1)	1	1 = All 48K of ROM is in external ROM

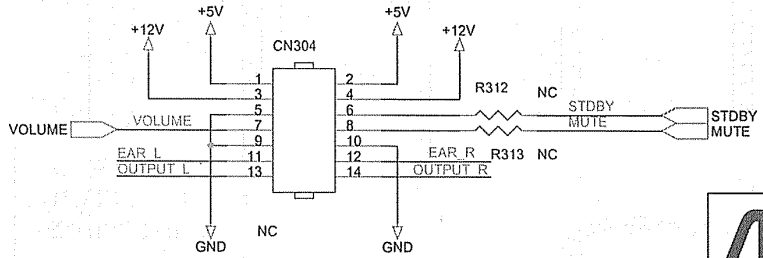
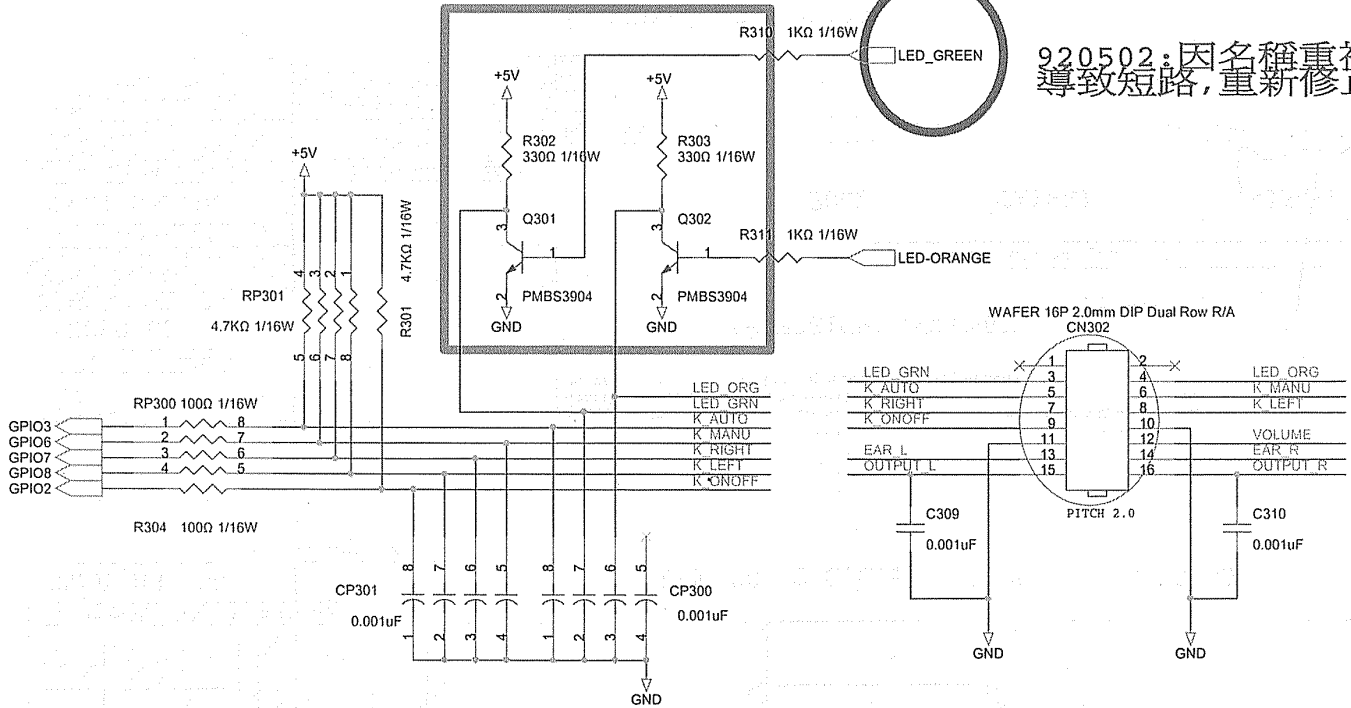
AOC 04. Gm2115
 715L1129-B-1-E.DSN
 Rev B
 Date: Entry, Dec 21, 1993



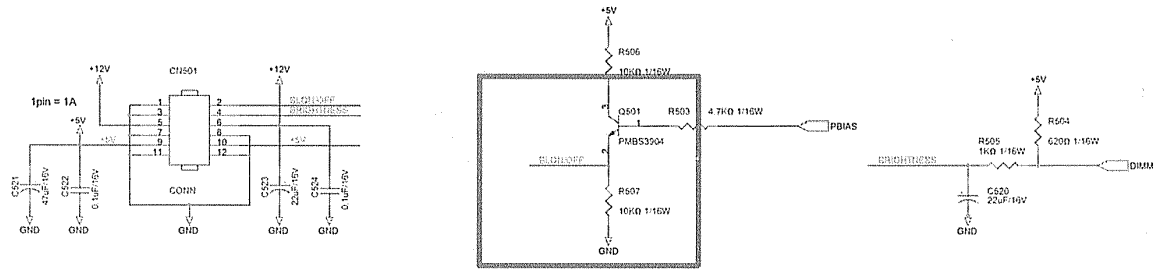
		Title 06. Board Power Supply	
		Size A	Document Number 715L1129-B-LE2.DSN
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920519: LED訊號腳反向

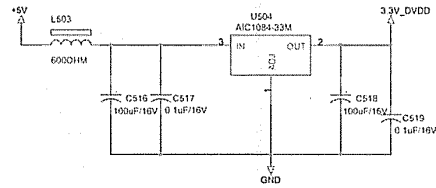
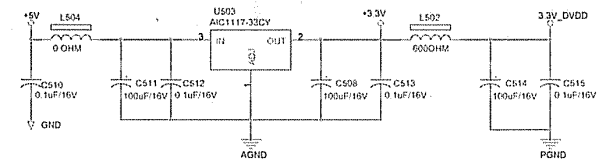
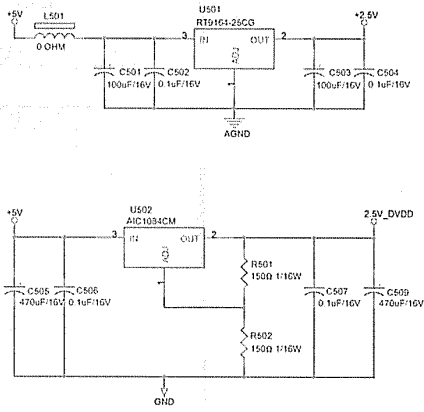
920502: 因名稱重複, 導致短路, 重新修正



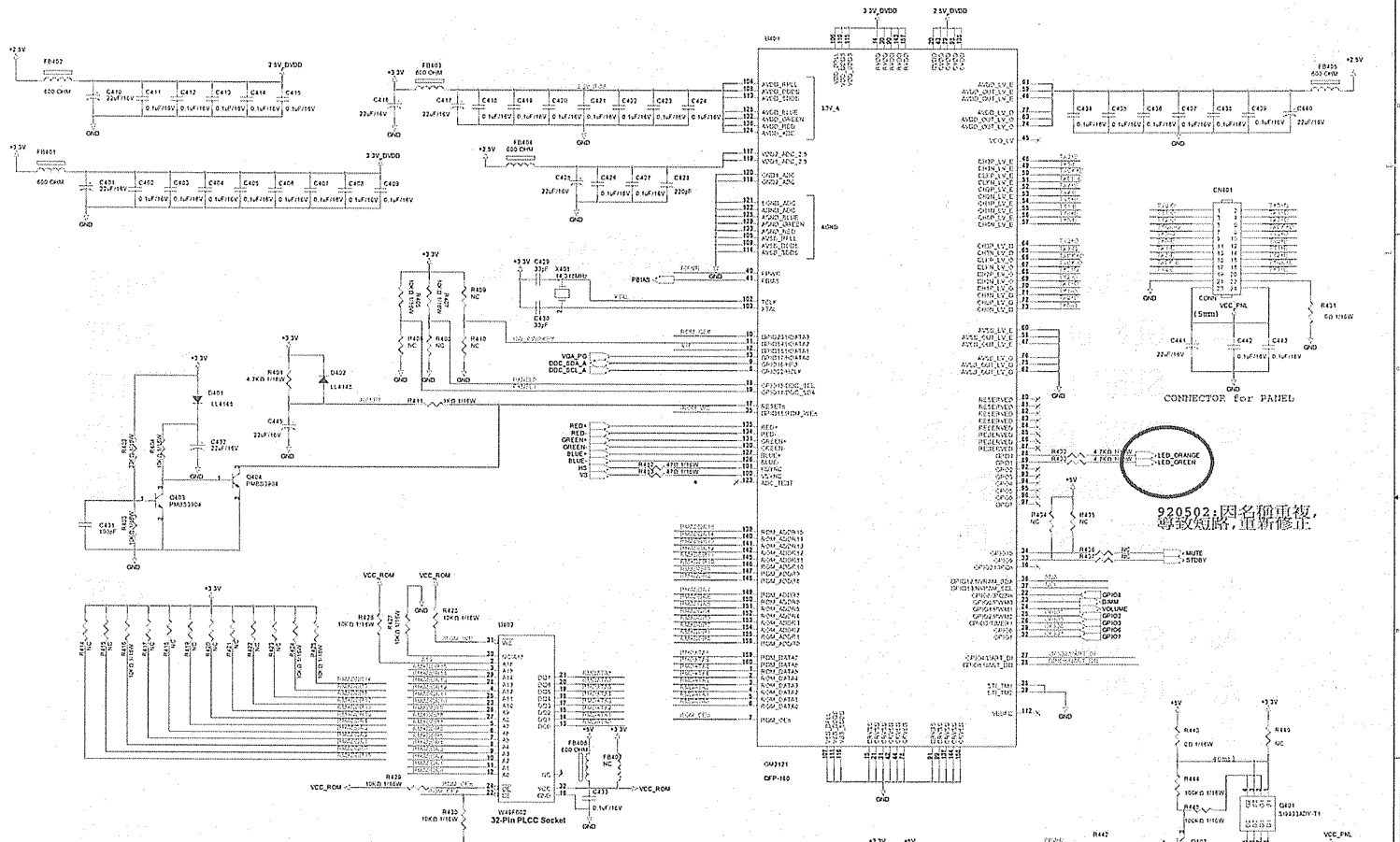
		Title	
		4.I/O Connectors	
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	EAGLE17-715L1130-B-LEG.DSN		
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920519: Inverter 訊號腳反向



	Info	5.Power	
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BOOTSTRAP SIGNALS

ADDRESS	NAME	SET	DESCRIPTION
ROM_ADDR(10)	USER_BTS(10)	x	Available for mixing from a status register
ROM_ADDR5	Reserve(1)	x	If using from boot period, program that bit 0
ROM_ADDR6	SCPFL	x	Determines polarity of HCLK output
ROM_ADDR7	HOST_PROTOCOL	0	If using from boot period, program that bit to 1
ROM_ADDR8	HOST_PORT_EN	1	GPIO(22-10) on "Host Port" pins
ROM_ADDR9	OCM_START	1	1 = OCM becomes active after OCM_CLK is active
ROM_ADDR(12-13)	USER_BTS(2)	x	Available for mixing from a status register
ROM_ADDR10	OCS_SEL	0	0 = XTAL and TCLK pins are connected
ROM_ADDR14	OCM_ROM_CFG(1)	1	1 = All bits of ROM are in system ROM

920502 因名稱重複，導致短路，重新修正。

AOC 3.2M2121
 EAGLE17-71SL1130-B-LEG.DSN
 DATE: 2007.03.23 11:00

GPIO4UART_DO R128 470 1/16W 100
 GPIO4UART_DI R103 470 1/16W 100

