



正基科技股份有限公司

SPECIFICATION

SPEC. NO. : _____ REV : 1.9

DATE : 07.20. 2012

PRODUCT NAME : WL-211

Only for TTV.

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				

AMPAK

WL-211 Wi-Fi SIP Module Spec Sheet



Revision History

Date	Revision Content	Revised By	Version
2011/08/22	-Initial released	Andy	1.0
2011/09/27	-Modify physical dimensions	Andy	1.1
2011/10/19	-Modify block diagram	Andy	1.2
2011/12/23	-Add Power Consumption	Andy	1.3
2012/01/12	-Modify dimension	Andy	1.4
2012/03/09	-Add packing information	Andy	1.5
2012/03/19	-More info to recommended footprint	Andy	1.6
2012/05/03	-Pin description revised	Bart	1.7
2012/05/18	-Modify Recommended Footprint -Modify Physical Dimensions	Bart	1.8
2012/07/20	-Modify Physical Dimensions	Bart	1.9

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1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the Wi-Fi functionalities. The highly integrated WL-211 module makes the possibilities of web browsing, VoIP, headsets and other applications. With seamless roaming capabilities and advanced security, WL-211 can also interact with different vendors' 802.11b/g/n Access Points in the wireless LAN.

This wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for Wi-Fi.

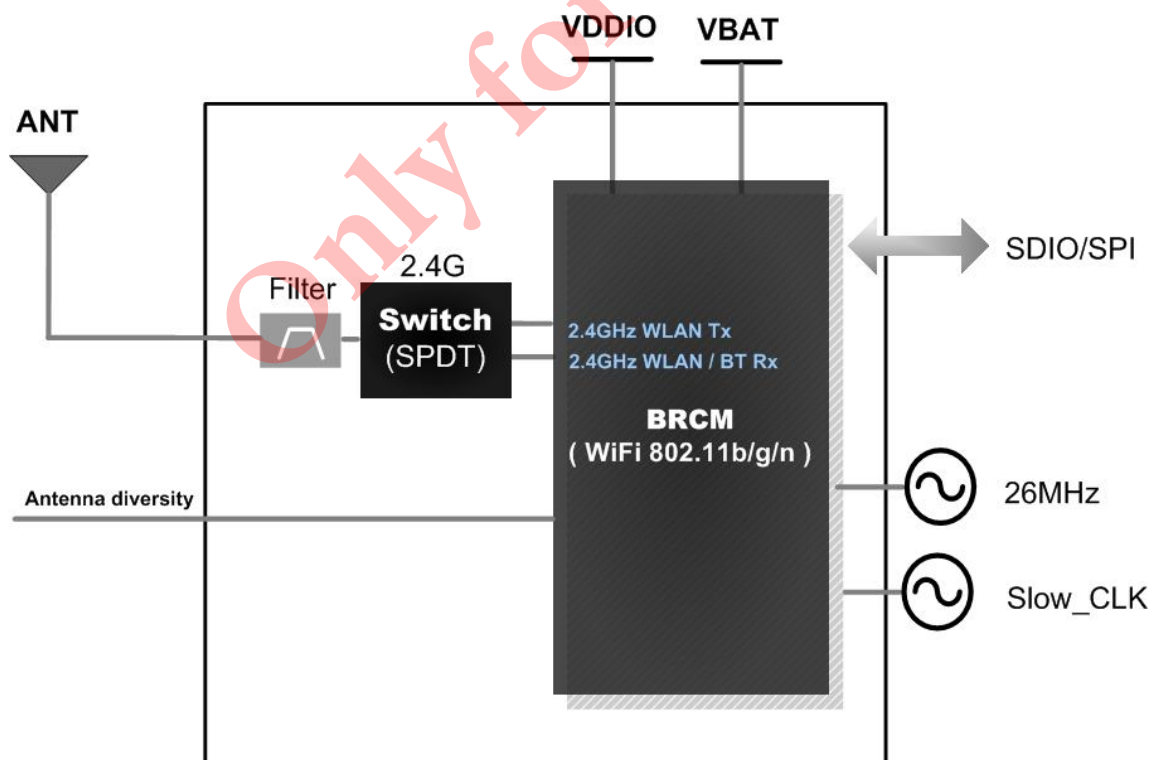
This compact module is a total solution for Wi-Fi technologies. The module is specifically developed for Smart phones and Portable devices.

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2. Features

- Single-band 2.4GHz IEEE 802.11b/g/n
- Supports standard interfaces SDIO v2.0(50MHz, 4-bit and 1-bit) and generic SPI(up to 50MHz)
- Integrated ARM Cortex-M3™ CPU with on-chip memory enables running IEEE802.11 firmware that can be field-upgraded with future features.
- Supports per packet Rx antenna diversity
- Security:
 - i. Hardware WAPI acceleration engine
 - ii. AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
 - iii. WPA™ – and WPA2™ - (Personal) support for powerful encryption and authentication

A simplified block diagram of the module is depicted in the figure below.



3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

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4. General Specification

4.1 Wi-Fi RF Specification

Conditions : VBAT=3.6V ; VDDIO=3.3V ; Temp:25°C

Feature	Description
Product Name	WL-211 Wi-Fi SIP Module
WLAN Standard	IEEE 802.11b/g/n, WiFi compliant
Host Interface	SDIO
Dimension	L x W x H: 9.5 x 9.5 x 1.5 (typical) mm
Frequency Range	2.412 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)
Number of Channels	11 for North America, 13 for Europe, and 14 for Japan
Modulation	802.11b : DQPSK, DBPSK, CCK 802.11g/n : OFDM /64-QAM, 16-QAM, QPSK, BPSK
Output Power	802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB
	802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB
	802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -28dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -85 ± 1dBm, typical
	- MCS=1 PER @ -84 ± 1dBm, typical
	- MCS=2 PER @ -82 ± 1dBm, typical
	- MCS=3 PER @ -80 ± 1dBm, typical
	- MCS=4 PER @ -77 ± 1dBm, typical
	- MCS=5 PER @ -73 ± 1dBm, typical
	- MCS=6 PER @ -71 ± 1dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -87 ± 1dBm, typical
	- 9Mbps PER @ -86 ± 1dBm, typical
	- 12Mbps PER @ -85 ± 1dBm, typical
	- 18Mbps PER @ -83 ± 1dBm, typical
	- 24Mbps PER @ -81 ± 1dBm, typical
	- 36Mbps PER @ -78 ± 1dBm, typical
	- 48Mbps PER @ -74 ± 1dBm, typical
	- 54Mbps PER @ -72 ± 1dBm, typical
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -90 ± 1dBm, typical
	- 2Mbps PER @ -89 ± 1dBm, typical
	- 5.5Mbps PER @ -87 ± 1dBm, typical
	- 11Mbps PER @ -84 ± 1dBm, typical

Data Rate	802.11b : 1, 2, 5.5, 11Mbps
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b : -10 dBm
	802.11g/n : -20 dBm
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	6.5	V
VDDIO	Digital/Bluetooth/SDIO/SPI I/O Voltage	-0.5	4.1	V

4.2.2 Recommended Operating Ratings

Test conditions: At room temperature 25°C				
Symbol	Min.	Typ.	Max.	Unit
VBAT	3.0	3.6	4.8	V
VDDIO	1.7	1.8	1.92	V
	2.97	3.3	3.6	V

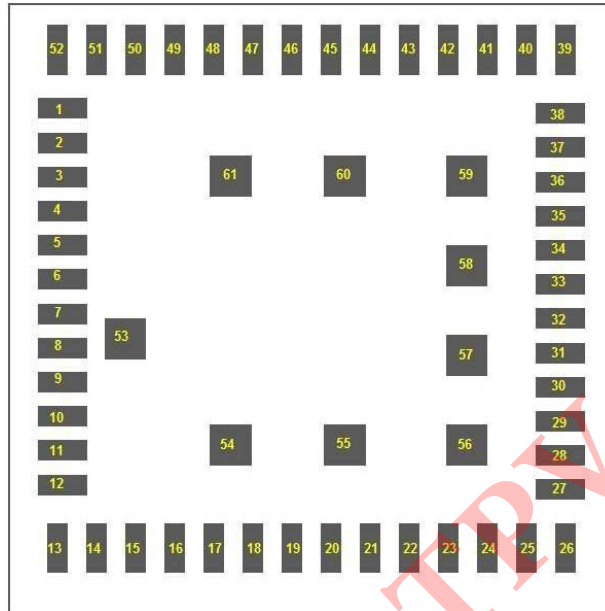
Note: The voltage of VDDIO is depended on system I/O voltage.

Test conditions: At operating temperature -10°C ~65°C				
Symbol	Min.	Typ.	Max.	Unit
VBAT	3.0	3.6	4.8	V
VDDIO	1.7	-	3.35	V

Note: VDDIO operating voltage range from 1.7V to 3.35V at operating temperature is guaranteed.

5. Pin Assignments

5.1 PCB Pin Outline



< TOP VIEW >

5.2 Pin Definition

NO	Name	Type	Description
1	WLAN_ANT	I/O	RF signal I/O port
2	GND	—	Ground
3	JTAG_TRST_L	I	JTAG interface, if JTAG not used unconnected (NC)
4	JTAG_TDO_UART_TX	O	JTAG interface, if JTAG not used unconnected (NC) this pin. This pin is also muxed with UART_TX, which can be enabled by software
5	JTAG_TDI_UART_RX	I	JTAG interface, if JTAG not used unconnected (NC) this pin. This pin is also muxed with UART_RX, which can be enabled by software
6	JTAG_TCK	I	JTAG interface, if JTAG not used unconnected (NC)
7	JTAG_TMS	I	JTAG interface, if JTAG not used unconnected (NC)
8	GND	—	Ground
9	OSC_IN	I	XTAL oscillator input
10	OSC_OUT	I/O	XTAL oscillator output
11	GND	—	Ground
12	RF_SW_CTRL0	—	Floating (Don't connected to ground)
13	RF_SW_CTRL3	—	Floating (Don't connected to ground)

14	GND	—	Ground
15	GND	—	Ground
16	GND	—	Ground
17	GND	—	Ground
18	VIO	I	Digital I/O Voltage input
19	CLK_32K	I	Sleep clock (32.768KHz) input
20	SDIO_DATA_2	I/O	SDIO data line 2
21	SDIO_DATA_0	I/O	SDIO data line 0
22	SDIO_CLK	I	SDIO clock
23	SDIO_CMD	I/O	SDIO command line
24	SDIO_DATA_1	I/O	SDIO data line 1
25	SDIO_DATA_3	I/O	SDIO data line 3
26	VIN_LDO	I	Internal DC-DC regulator input
27	GND	—	Ground
28	SR_VLX	O	Internal DC-DC regulator output
29	GND	—	Ground
30	VBAT	I	DC voltage input
31	WL_RST_N	I	Active low WLAN reset signal
32	GND	—	Ground
33	GND	—	Ground
34	GND	—	Ground
35	GND	—	Ground
36	XTAL_PU	O	Floating (Don't connected to ground)
37	GND	—	Ground
38	GND	—	Ground
39	GND	—	Ground
40	GND	—	Ground
41	GND	—	Ground
42	GND	—	Ground
43	VDD_TCXO	—	Floating (Don't connected to ground)
44	GND	—	Ground
45	TCXO_IN	—	Floating (Don't connected to ground)
46	GPIO_5	—	Floating (Don't connected to ground)
47	GPIO_4	—	Floating (Don't connected to ground)
48	GPIO_3	—	Floating (Don't connected to ground)
49	GPIO_1	O	WL_Host Wake,
50	GPIO_0	—	Mode selection, Low for SDIO, High for SPI mode
51	WRF_GPIO_OUT	—	Floating (Don't connected to ground)

52	GND	—	Ground
53	GND	—	Ground
54	GND	—	Ground
55	GND	—	Ground
56	GND	—	Ground
57	GND	—	Ground
58	GND	—	Ground
59	GND	—	Ground
60	GND	—	Ground
61	GND	—	Ground

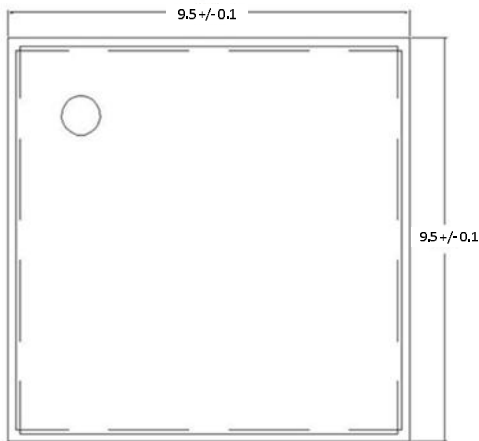
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6. Dimensions

6.1 Physical Dimensions

(Unit: mm)

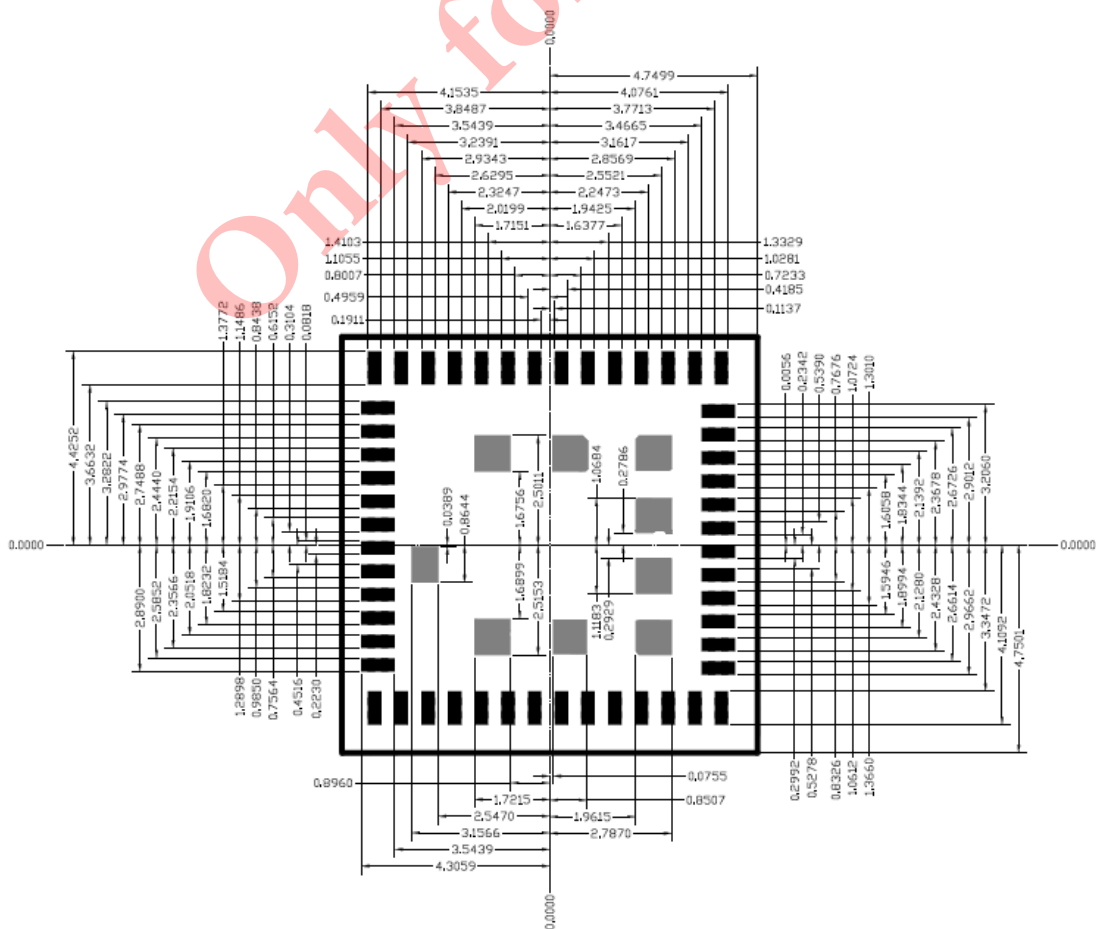
< TOP VIEW >



< Side View >



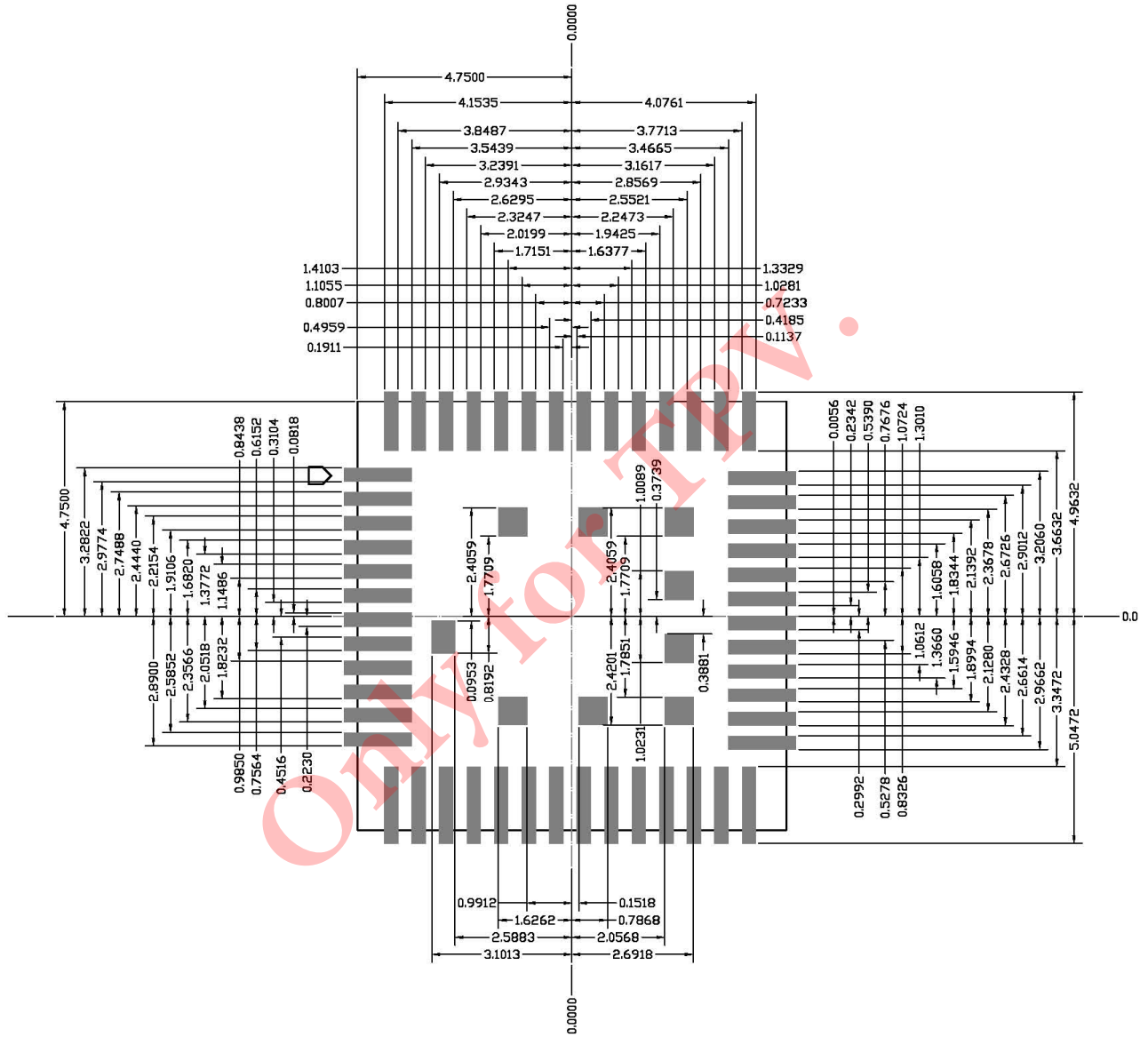
< TOP VIEW >



6.2 Recommended Footprint

(Unit: mm)

< TOP VIEW >



7. External clock reference

External LPO signal characteristics

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	± 30	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1600 to 3300	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz

7.1 SDIO Pin Description

The WL-211 supports SDIO version 1.2 for both 1-bit (25 Mbps), 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

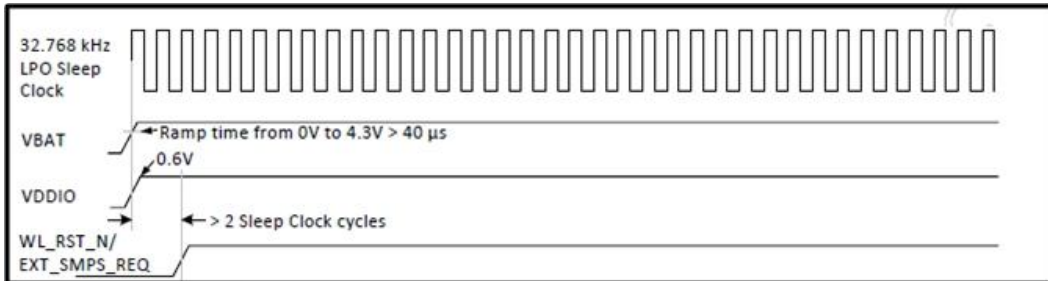
- ※ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ※ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ※ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize / ByteCount = 512B)

SDIO Pin Description

SD 4-Bit Mode		SD 1-Bit Mode		SPI Mode	
DATA0	Data Line 0	DATA	Data Line	DO	Data Output
DATA1	Data Line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data Line 2 or Read Wait	RW	Read Wait	NC	Not Used
DATA3	Data Line 3	NC	Not Used	CS	Card Select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command Line	CMD	Command Line	DI	Data Input

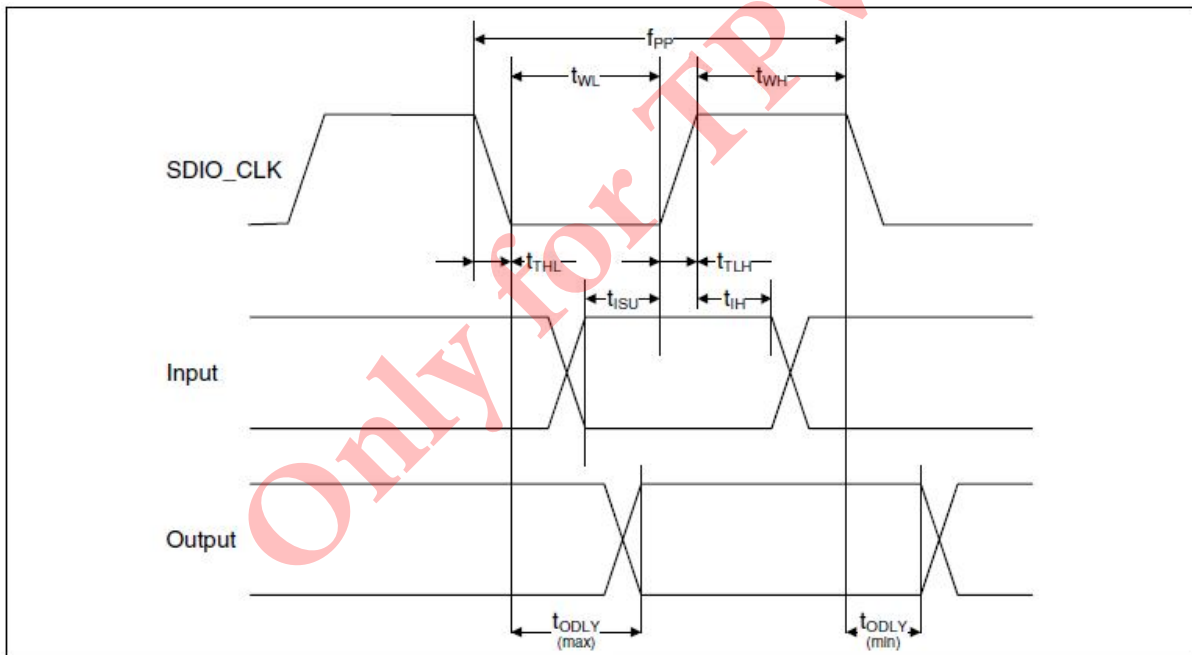
8. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram



- ※ WL_RST_N: Low asserting Reset for WLAN Core. This pin must be driven high or low (not left floating).

8.2 SDIO Default Mode Timing Diagram

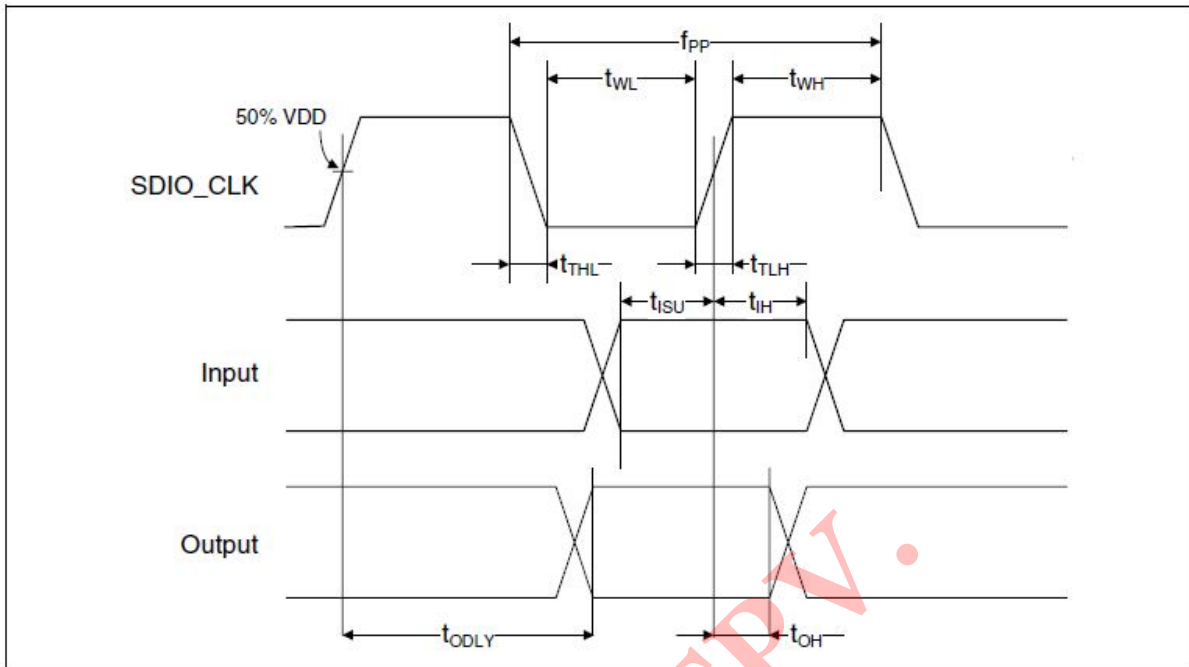


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL^b)					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time - Data Transfer mode	tODLY	0	-	14	ns
Output delay time - Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.

b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

8.3 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency-Data Transfer mode	f _{PP}	0	-	50	MHz
Frequency-Identification mode	f _{OD}	0	-	400	kHz
Clock low time	t _{WL}	7	-	-	ns
Clock high time	t _{WH}	7	-	-	ns
Clock rise time	t _{TLH}	-	-	3	ns
Clock low time	t _{THL}	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t _{ISU}	6	-	-	ns
Input hold time	t _{IH}	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time - Data Transfer mode	t _{ODLY}	-	-	14	ns
Output hold time	t _{OH}	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.

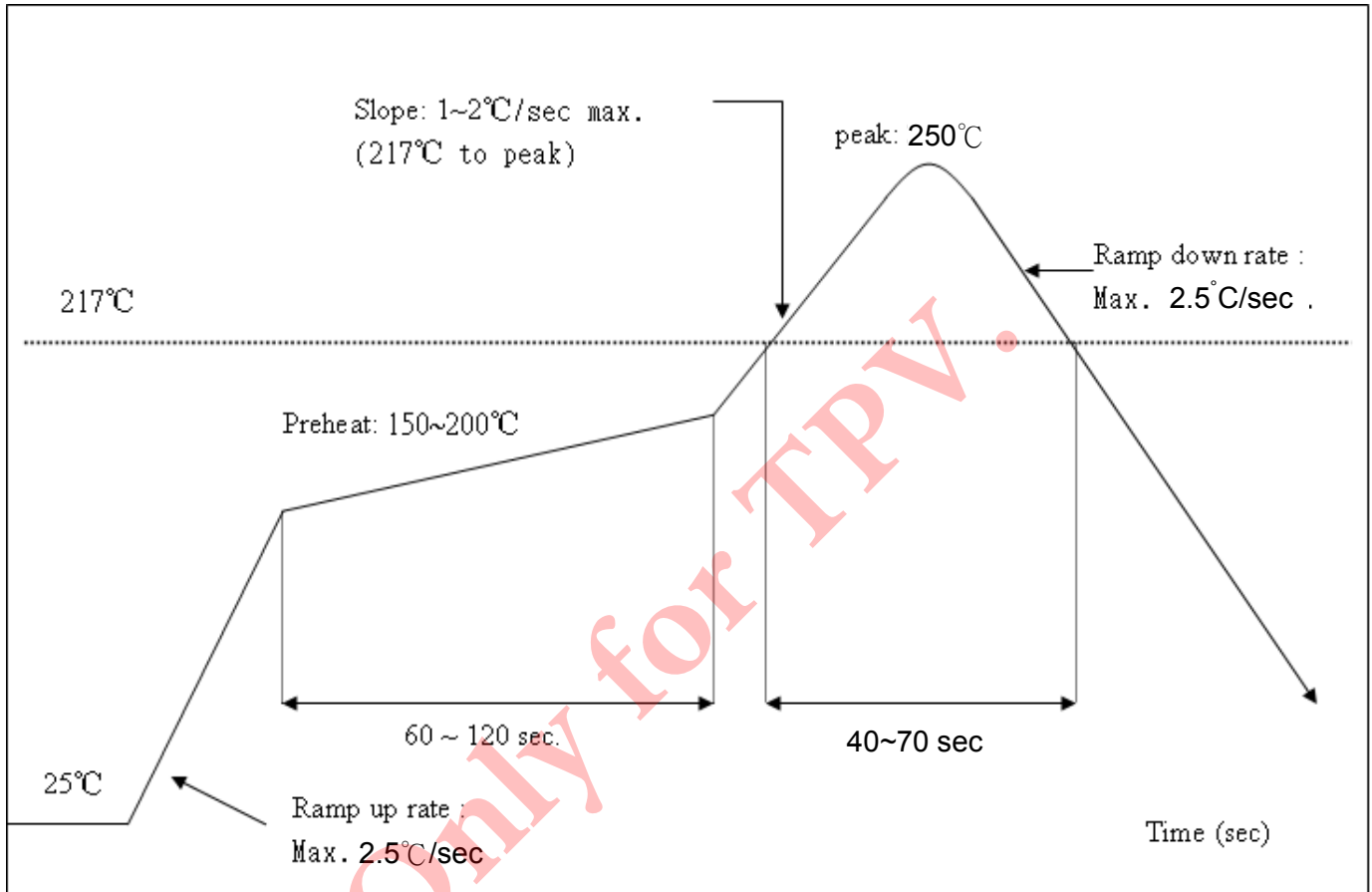
b. min(V_{Ih}) = 0.7 x VDDIO and max(V_{Il}) = 0.2 x VDDIO.

9. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : $<250^{\circ}\text{C}$

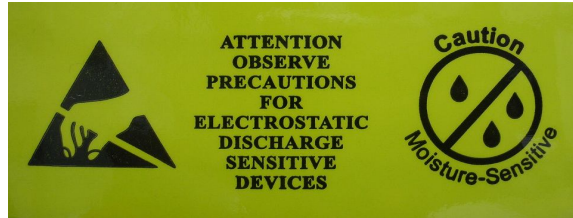
Number of Times : ≤ 2 times




10. Packing Information

10.1 Label





Label A → Anti-static and humidity notice








Label B → MSL caution / Storage Condition

	Caution	LEVEL
	This bag contains MOISTURE-SENSITIVE DEVICES	
1. Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)		
2. Peak package body temperature: _____ °C <small>If blank, see adjacent bar code label</small>		
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be		
a) Mounted within: _____ hours of factory conditions <small>If blank, see adjacent bar code label</small>		
b) Stored per J-STD-033		
4. Devices require bake, before mounting, if:		
a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 23 ± 5°C		
b) 3a or 3b are not met		
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure		
Bag Seal Date: _____ <small>If blank, see adjacent bar code label</small>		
<small>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</small>		

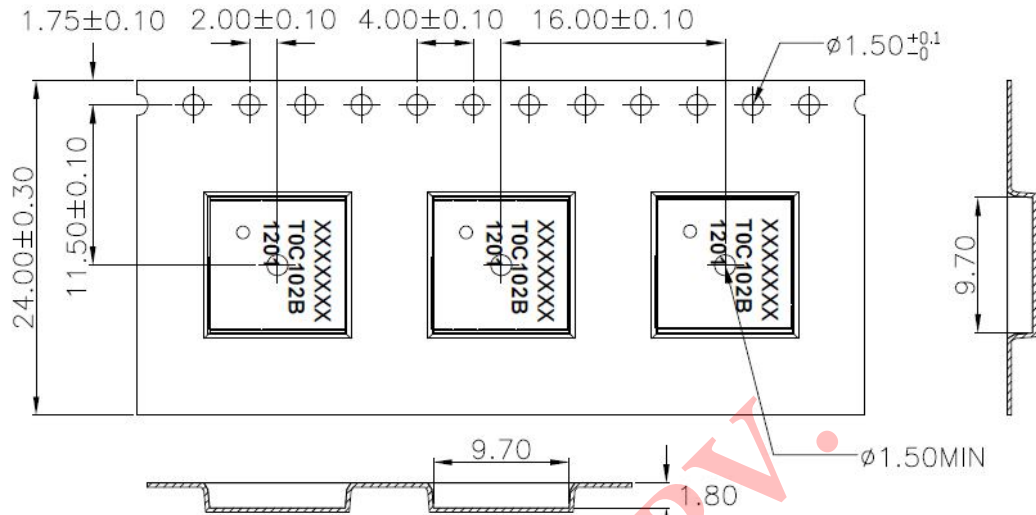
Label C → Inner box label .

PKG S/N :	
	9PKG12013100001
Model:	
	XXXXXXXX(HF)
P/N :	
	99P-W01-0042R
Qty :	
	1500
Date Code :	
	1205
Lot Code :	
	T0C102B

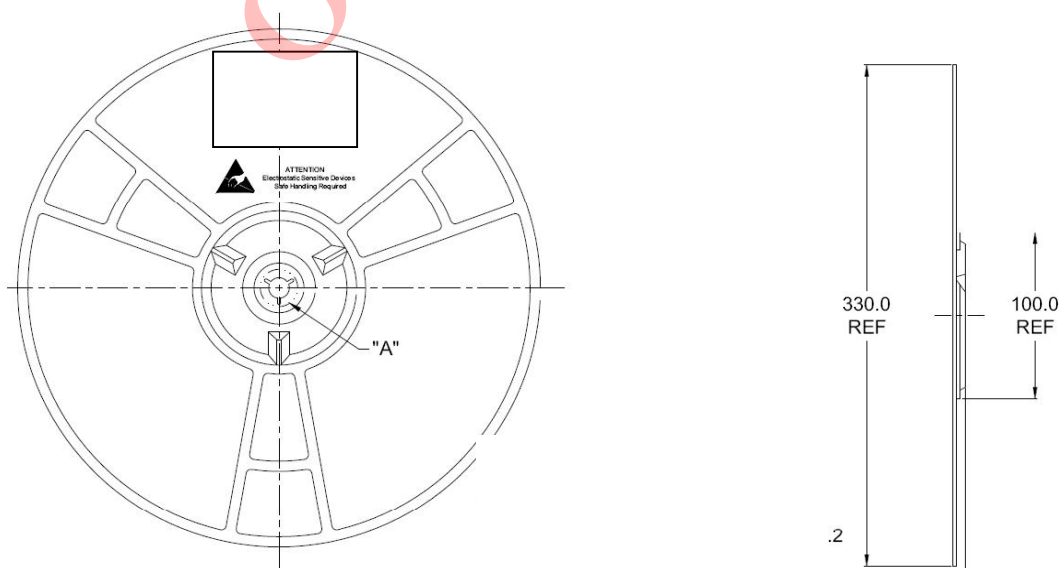
Label D → Carton box label .

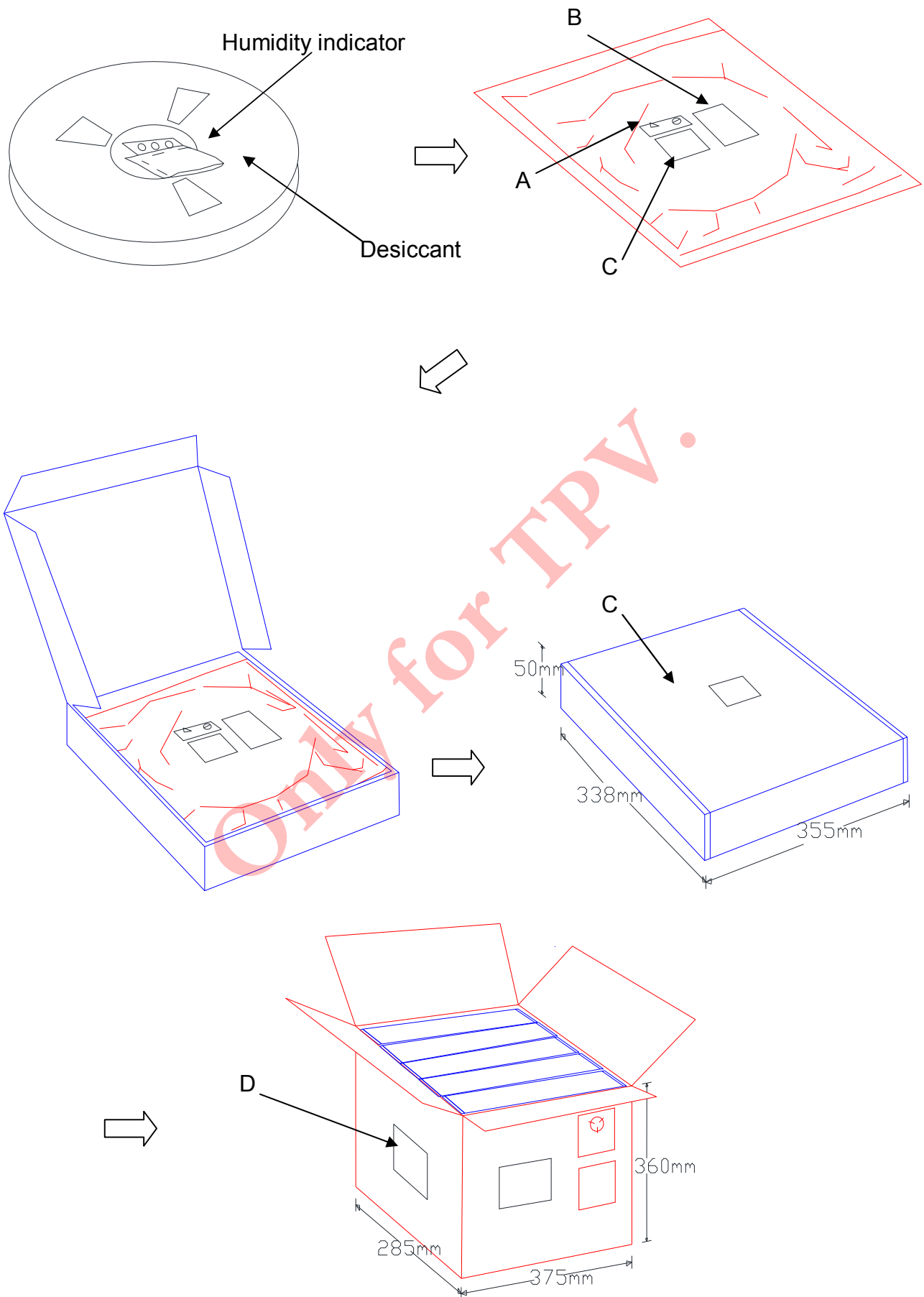
AMPAK Technology	
Model Name :	
	XXXXXXXX(HF)
Part No :	
	99P-W01-0042R
Quantity :	
	7500 ea
Lot D/C :	
	1205
Manufacture :	
	2012/02/22

10.2 Dimension




1. 10 sprocket hole pitch cumulative tolerance ± 0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30 ± 0.05 mm.
6. Packing length per 22" reel : 98.5 Meters.(1:3)
7. Component load per 13" reel : 1500 pcs.





10.3 MSL Level / Storage Condition

	<h2 style="margin: 0;">Caution</h2> <p style="margin: 0;">This bag contains MOISTURE-SENSITIVE DEVICES</p> <p style="margin: 0;">Do not open except under controlled conditions</p>	<table border="1" style="margin: 0 auto;"> <tr><td style="padding: 2px;">LEVEL</td></tr> <tr><td style="font-size: 2em; padding: 10px;">4</td></tr> </table>	LEVEL	4
LEVEL				
4				
<p>1. Calculated shelf life in sealed bag: 12 months at <math>< 40^{\circ}\text{C}</math> and <math>< 90\%</math> relative humidity(RH)</p>				
<p>2. Peak package body temperature: 225°C 240°C 250°C 260°C</p> <p style="text-align: center;"> <input type="checkbox"/> <input type="checkbox"/> <input checked="" type="checkbox"/> <input type="checkbox"/> </p>				
<p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must</p> <p style="margin-left: 20px;">a) Mounted within: 48 hours of factory conditions <math>< 30^{\circ}\text{C}/60\%</math> RH, OR</p> <p style="margin-left: 20px;">b) Stored at <math>< 10\%</math> RH</p>				
<p>4. Devices require bake, before mounting, if:</p> <p style="margin-left: 20px;">a) Humidity Indicator Card is >10% when read at <math>23 \pm 5^{\circ}\text{C}</math></p> <p style="margin-left: 20px;">b) 3a or 3b not met</p>				
<p>5. If baking is required, devices may be baked for 24 hours at <math>125 \pm 5^{\circ}\text{C}</math></p>				
<p>Note : If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure</p>				
<p>Bag Seal Date: <u> See-SEAL DATE LABEL </u></p>				
<p>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p>				

※NOTE : Accumulated baking time should not exceed 96hrs



Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.



This device is intended only for OEM integrators under the following conditions:

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

FOR MOBILE DEVICE USAGE (>20cm/low power)

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains FCC ID:ARS-WL211 ”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.