Attachment to FCC Form 731

FCC ID: AQZ-MX-9325

Exhibit 12

Operational Description

General Information

The MX-9325 Transceiver is designed to be a multiple-mode radio for use in ground-to-air data communications applications. The A2D emission mode supports the Aircraft Communications Addressing and Reporting System (ACARS) service. In the G1D and G7D modes the transceiver will support future use in Flight Information Service (FIS) systems. These FIS systems will be implemented using VDL Mode 2 (G1D) or Mode 3 (G7D).

The MX-9325 Transceiver employs digital microcontrollers that perform all control, modulation waveform synthesis and demodulation functions. The A2D emission consists of an amplitude modulated minimum-shift keying (AM-MSK) waveform which has a constant amplitude but a frequency that shifts between 1200 and 2400 Hz. The G1D and G7D emissions utilize a differentially encoded, 8 phase shift keying (D8PSK) modulated signal. The MX-9325 Transceiver is continuously adjustable over the range 5 watts to 25 watts. Closed loop power control is used to set and maintain the output power level.

The transceiver operating mode (i.e. ACARS, Mode 2 or Mode 3) is selected by issuing a software command via the front panel maintenance connector, then power cycling the transceiver.

The transceiver consists of several functional modules including receiver, exciter, power amplifier, low pass filter and power supply assemblies, which are contained within a single chassis. The transmit and receive circuits share common frequency control and reference oscillator circuits. For these reasons, the receiver part of the MX-9325 transceiver will be authorized under a grant of Verification pursuant to § 15.101(b), and the transceiver will have a single FCC identifier per § 2.925(b).

The MX-9325 Transceiver is powered from the AC mains and operates over the voltage range of 110 to 220 VAC.

2.1033 (c)(10) Description of all circuitry and devices provided for determining and stabilizing frequency, for suppression of spurious radiation, for limiting modulation, and for limiting power.

Frequency stabilization. The MX-9325 Transceiver uses a temperature compensated crystal oscillator (TCXO) to achieve the required frequency stability over its operating temperature range. The TCXO is located on the Digital Processor board and is used as a master reference oscillator for all transceiver circuits. The TCXO is purchased as a completed unit and consists of a Colpitts oscillator with varactor-thermistor temperature compensating networks. The

TCXO vendor tests and calibrates each unit before shipment to ensure that all specifications are met. The TCXO used in the MX-9325 has a frequency stability of 1 part per million (ppm) over the frequency range –30 to + 70 degrees Celsius. It also has a DC control pin which is used as a fine frequency adjust to set the oscillator precisely on frequency and correct for aging drift. Refer to Exhibit 5, Schematic Diagrams (filename digbd.PDF) for a schematic diagram of the circuit in which the TCXO is operated.

Suppression of spurious radiation. For conducted spurious emissions, the MX-9325 Transceiver employs a seventh order elliptic function low pass filter with a cutoff frequency of 155 MHz. This filter is physically located on the Directional Coupler/Low Pass filter board assembly. Electrically it is in the signal path between the power amplifier and the antenna connector in order to prevent conducted harmonic energy from reaching the antenna. For radiated emissions, the MX-9325 Transceiver is packaged inside a sheet metal enclosure. Top and bottom covers are equipped with RF gasketing material to prevent cabinet radiation from exceeding the limits specified in Part 15. Filtering is also used on all input/output connectors to further minimize radiation. Refer to Exhibit 5, Schematic Diagrams (filename: lpfdc.PDF) for the schematic diagram of the low pass filter and its associated circuits. Also please refer to Exhibit 9, Internal Photographs for pictures showing construction and mounting of the low pass filter.

Modulation limiting. The MX-9325 Transceiver employs a digital signal processor (DSP) integrated circuit which runs firmware signal processing algorithms to synthesize the AM-MSK or D8PSK modulation waveforms. The algorithms contain leveling loops to ensure that the modulating waveforms are of constant amplitude. Since this transceiver accepts only digital data input, and does not have the provision for an external audio input, the usual pre-emphasis/clipper/low pass filter stages are not needed, and are not provided.

Power limiting. The MX-9325 Transceiver has a closed-loop power control system that keeps the transmitter power constant over the frequency range and environmental conditions. The loop consists of a directional coupler at the output of the power amplifier; the digital signal processor; and a voltage variable attenuator (VVA) at the output of the exciter board. The directional coupler provides a dc output voltage proportional to the power output level; the digital signal processor compares this level to the power set point value and adjusts the VVA as required to maintain the desired power output.

2.1033 (c)(13) Detailed description of the digital modulation system to be used.

For all emission modes, the transceiver accepts digital data from external equipment via a RS-530 synchronous serial interface, and internally formats this data and synthesizes the correct waveforms through the use of a digital signal processor.

The A2D emission uses an amplitude modulated, minimum shift keying (AM-MSK) modulation scheme, which is a constant phase, frequency shift technique

using two tones. In this transceiver the tones are 1200 Hz and 2400 Hz sine waves. The presence of 1200 Hz indicates a bit change from the previous bit, while the presence of 2400 Hz indicates no bit change. The phase of these two tones is controlled by the DSP such that minimum phase discontinuity occurs at the interface with the preceding bit. Also, the DSP ensures that the amplitude of each tone is zero at the bit transition.

For both the G1D and G7D emissions, the data stream consists of a differentially encoded 8 phase shift keying signal which uses a raised cosine filter with α = 0.6. The raised cosine filter is implemented as a signal processing algorithm within the digital signal processor (DSP). The information to be transmitted is differentially encoded with 3 bits per symbol (baud) transmitted as changes in phase rather than absolute phase. The data stream to be transmitted is divided into groups of 3 consecutive data bits, least significant bit first. To aid clock recovery and to stabilize the shape of the transmitted spectrum, bit scrambling is applied. The pseudo noise (PN) sequence is a 15 - stage generator with the characteristic polynomial $X^{15} + X + 1$.

The DSP algorithm takes the resulting data stream and generates two analog signals I and Q which are separated in phase by 90 degrees, via a pair of digital-to-analog converter Ics. The I and Q signals contain amplitude and phase information which describes each bit transition. Both of these signals are filtered at baseband by means of a five section Bessel low-pass filter before they modulate the RF carrier. A plot of the response of this filter appears in the section titled “Modulation Characteristics” of the Test Report, which is contained in Exhibit 6 of this Attachment.

The transmitted signal is produced by means of a vector modulator, which consists of two balanced modulators, one each for the I and Q baseband signals. By means of the balanced modulators each baseband signal modulates an RF carrier, with the resulting modulated signals being combined to form the composite transmitted signal.

The G1D and G7D emissions differ only in the length and timing of the transmitted data burst. In VDL Mode 2 applications the data transceiver utilizes a carrier sense multiple access (CSMA) operating algorithm to transmit and receive packets of data as the radio channel becomes available. For this mode the G1D emission designator applies. The G7D designator applies for transceivers operating in VDL Mode 3 systems, which uses a time division multiple access (TDMA) data format. In this mode data is sent during well defined time intervals that are synchronized via a master clock. In this way, digital data may be sent in one time slot and digitally encoded analog signals may be sent in the next slot.