5 .Description of Circuitry or Theory or Operation

CONTENTS

FCC ID: APV0398
2.1033(b)(4) CIRCUIT DESC.

1. CONTROLS AND CONNECTIONS

① Antenna

② PTT (Push-To-Talk) switch
When pressed, switches the transceiver from receive to transmit.

③ FUNCTION key (LAMP key)
Used in combination with other keys to select other functions.
Press this key to turn the display lamp on for 5 seconds.

(Func + PTT/ Lamp Lock)
Hold down the FUNCTION key and press PTT key to turn the display lamp on continuously.

(Func + Down + Up/ Group mode On/Off)
Toggles between Basic mode and Group mode.
Hold down the FUNCTION key and Down key and Up key to display the Group Number.

④ MONITOR key
Press this key to open the squelch.

⑤ UP key
Press the up key to increase the channel number.

(Func + Up / Group Number +1)
If Group mode is enabled, Hold down the function key and press the up key to increase the group number.

⑥ DOWN key
Press the down key to decrease the channel number.

(Func + Down / Group Number -1)
If Group mode is enabled, Hold down the function key and press the down key to decrease the group number.

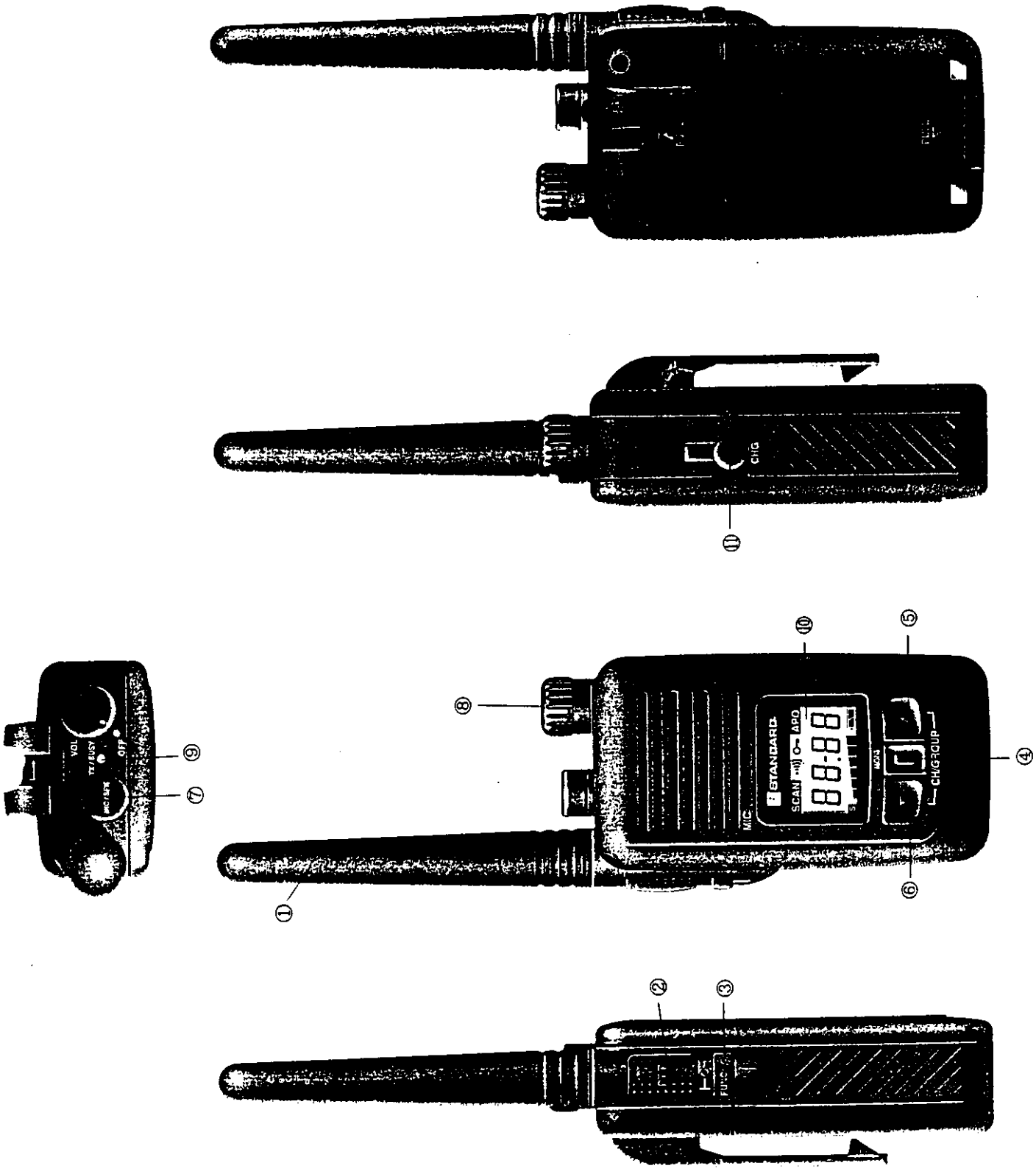
⑦ Microphone / Speaker Jack
External Microphone jack and speaker jack. To connect an optional microphone and speaker.

⑧ POWER / VOLUME knob
Turn this knob clockwise to turn the transceiver on, also turn this knob clockwise to increase the volume level.
Turn this knob counterclockwise to decrease the volume level, also turn this knob counterclockwise fully to turn the transceiver off.

⑨ TX / BUSY Indicator
Illuminates red during transmissions.
Illuminates green during reception or when the squelch is off (the monitor key is pressed).

⑩ LCD display

⑪ Charge Jack


⑪
⑩
⑤
⑧
④
⑥
①
⑨
⑦
②
③
STANDARD
APO
SCAN
MIC
CH/GROUP
VOL
OFF

2. THEORY OF OPERATION

2.1 PLL Synthesizer

PLL IC QP07, which is used in the PLL circuit, has a built-in programmable divider, phase comparator, prescaler, charge pump, and reference divider circuit. It controls the VCO.

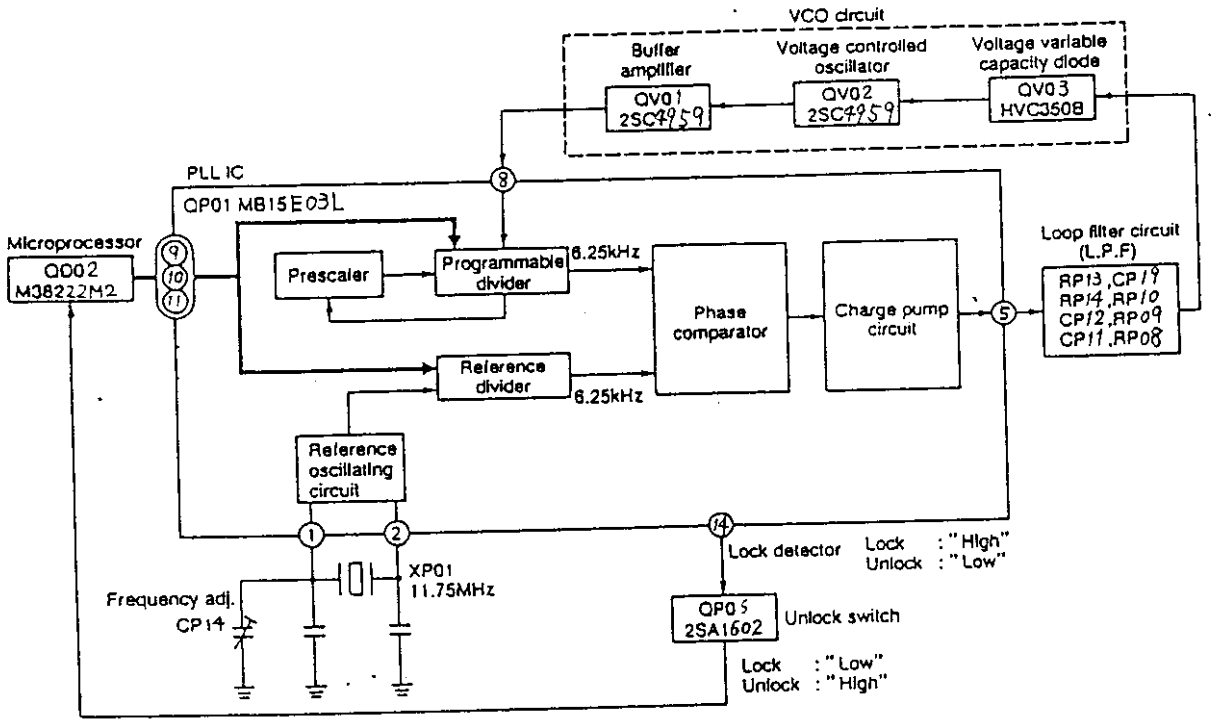


Figure 2-1

2.1.1 VCO Circuit

The VCO circuit comprises QV01, QV02, and QV03. The oscillator output is generated by QV02, which comprises a clamp circuit. The oscillation frequency passes from PLL IC QP07 through a loop filter circuit (low-pass filter) and is applied to the cathode of voltage variable capacity diode QV03, where it is changed by the voltage. Also, the modulation method used for the audio signal is reactance modulation in which the voltage of the anode side of QV03 is changed.

2.1.2 Reference Oscillating Circuit

The 11.75 MHz reference oscillation frequency for PLL IC QP07 is generated by crystal oscillator element XP01 and the oscillator built into PLL IC QP07.

2.1.3 PLL Circuit

The 11.75 MHz reference oscillation frequency generated by the PLL IC is frequency divided to 1/1,880 by the reference divider built into QP07, based on the dividing ratio data from microprocessor QD02.
After frequency division, the 6.25 kHz reference frequency is applied to a phase comparator built into QP07.
The oscillation output from the VCO is input to pin8 of QP07 and frequency divide to 6.25 kHz by the programmable divider, based on the dividing ratio data from QD02. The 6.25 kHz reference frequencies produced though frequency division by the two frequency dividers are then applied to the phase comparator.
If the phase does not match, the charge pump circuit outputs a high-level or a low-level pulse. The VCO charge pump pulse output from pin 5 of QP07 is converted to DC voltage by the loop filter circuit. Then it is applied to QV03.
In this way, the circuit's VCO oscillation frequency is controlled.

2.1.4 Unlock Control

If the PLL is locked, QP07 outputs a high-level signal from pin 14. A low-level signal is output if the PLL is unlocked.
The output from pin 14 of QP07 is logically inverted by unlock switch QP06 and then applied to pin 3 of microprocessor QD02.
This allows QD01 to determine if the PLL is locked or not.
If QP07 is unlocked, QD02 prohibits transmission to ensure that no unwanted radio signals are radiated.

2.2 Receiver Block

The receiver block comprises the RF amplifier circuit, the band-pass filter, the first mixer circuit, the first IF amplifier circuit, the second IF circuit and the audio power amplifier.

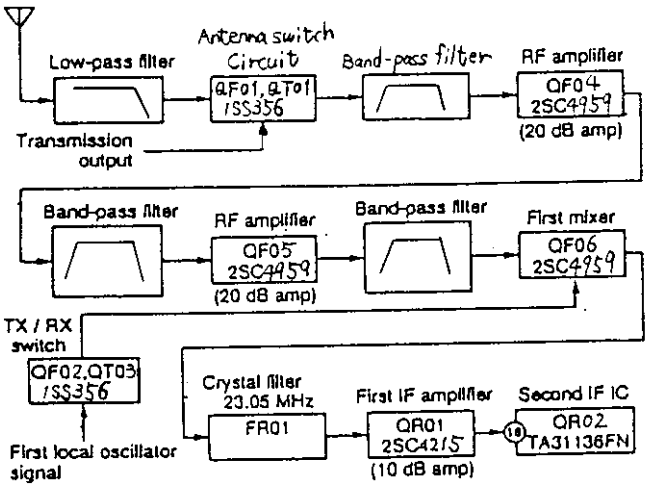


Figure 2-2

2.2.1 RF Amplifier Circuit

The reception signal passes from the antenna through low-pass and high-pass filters. After unwanted image signals and the like have been eliminated, the reception signal is applied to an antenna switch circuit consisting of QF01 and QT01. If the antenna switch circuit switches to the receive side, the reception signal is input to RF amplifier QF04, where it is amplified by approximately 20dB. After this, it passes though band-pass filter before being output.
After passing through band-pass filter, the reception signal is input to RF amplifier QF05, where it is amplified approximately 20dB. After this, it passes through band-pass filter and is output.

2.2.2 First Mixer Circuit

The reception signal amplified by the RF amplifier circuit and the first local oscillator signal are mixed by first mixer QF06, converting them to the 23.05 MHz first intermediate frequency.

Reception frequency = VCO frequency + 23.05 MHz

2.2.3 First IF Amplifier

After the reception side is selected by diode switch QF02, the first IF signal has unwanted adjacent signal elements eliminated by crystal filter FR01 and is amplified approximately 10 dB by first IF amplifier QR01.

2.2.4 Second Local Oscillator and Second Mixer Circuit

The amplified first IF signal is mixed with the 23.05 MHz second local oscillator frequency in the second mixer built into IF IC QR02. This converts it into the 450 kHz second Intermediate Frequency.

2.2.5 Second IF Filter, Second IF Amplifier, and Detector Circuit

After being converted to 450 kHz internally by QR02, the second IF signal passes from pin 3 of QR02 though ceramic filter FR03 (guaranteed attenuation of 6 dB bandwidth +-4.5 kHz or more: 35 dB) to obtain even better selectivity, then input to pin 5 of QR02. Then it is amplified internally by QR02 and, after limiting, undergoes wave detection (quadrature) by FR02. The result is then output from pin 9 of QR02 as the AF signal.

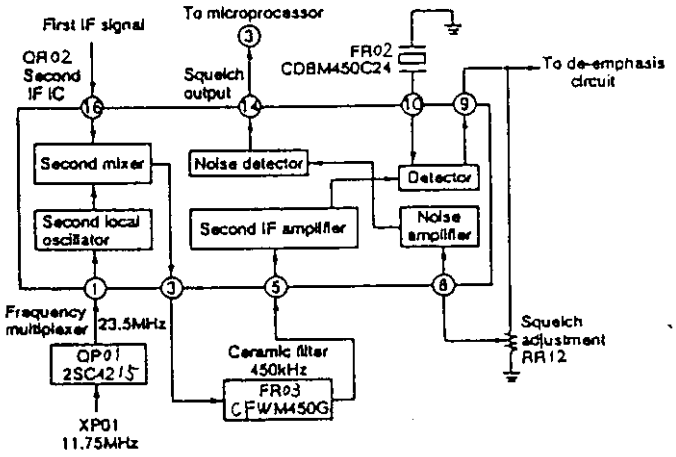


Figure 2-3

2.2.6 Audio Frequency Circuit

A portion of the audio signal output from pin 9 of second IF IC QR02 is input to a de-emhasis circuit consisting of RR14 and CR14. The de-emhasis circuit consisting of RR14 and CR14 (-6dB/oct.) performs frequency correction on the audio signal. After passing though the de-emhasis circuit, the audio signal is input to AF amplifier QR03. The audio signal input to AF amplifier QR03 is amplified approximately 6 dB there. After this, the amplified audio signal is input to AF switch QR04. AF switch QR04 is controlled by the output level of pin 13 of microprocessor QD02. When AF switch QR04 is on, the audio signal passing through QR04 is input to the volume adjustment resistance SD06 (a trimming potentiometer).

The input audio signal is level adjusted by the volume adjustment resistance SD06 and then input to pin 2 of AF power amplifier QR07.

The audio signal input to AF power amplifier QR07 is amplified to approximately 0.1W and then output from pin 6 of QR07. The audio signal output from pin 6 of AF power amplifier QR07 passes though external speaker jack JM01 and drives internal speaker ED01.

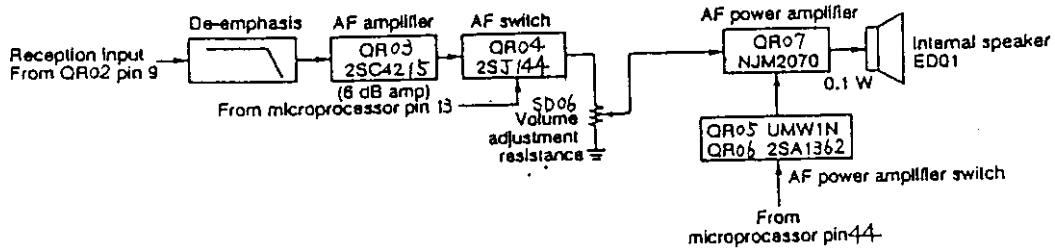


Figure 2-4

2.2.7 Squelch Circuit

When there is no signal (when no audio signal is being received), the white noise output from pin 9 of QR02 is level adjusted by squelch adjustment point RR12 (a trimming potentiometer). After being level adjusted, the white noise passes though a noise filter consisting of CR07, CR08, RR09 and RR10 before being applied to pin 8 of QR02. The white noise signal is applied to the noise amplifier built into QR02 and then converted into DC voltage by the noise detector circuit. The squelch signal output from pin 14 of QR02 is applied to pin 24 of microprocessor QD02. This allows QD02 to determine whether the transceiver is in reception status or no-signal status.

2.2.8 Muting Circuit

The squelch function operates by turning the power supply to power amplifier QR07 on and off using AF power amplifier switches QR05 and QR06. AF power amplifier switch QR05 is controlled by the signal from pin 44 of microprocessor QD02. At the same time, the control signal from pin 13 of microprocessor QD02 turns AF switch QR04 on and off.

2.2.9 Keypad Operation Tone Circuit

The keypad operation tones are output from pin 12 of microprocessor QD02.
The keypad operation tones from pin 12 of QD02 pass though a low-pass filter consisting of RR32 and CR28 before being applied to AF power amplifier QR07.

2.2.10 Tone Decoder Circuit for Group Mode

The detector's audio output also is fed to the tone low-pass filter QC01(4/4). Then the output of the low-pass filter is routed to the second stage filter QC01(3/4). The output of QC01(3/4) is applied to the squaring circuit QC01(2/4) and finally to the microprocessor QD02 pin 11 for decoding. At this point, the microprocessor determines whether the tone signal input to pin 11 of microprocessor QD02 matches the transceiver's tone signal setting.
If the tone signal matches, the output signals from pin 13 and 44 of microprocessor QD02 are applied to AF switch QR04 and AF power amplifier switch QR05.
AF switch QR04 turns on and AF power amplifier switch QR05 operates. If power is supplied to AF power amplifier QR07, the audio signal is output from internal speaker ED01.

2.3 Transmitter Block

The transmitter block comprises buffer amplifier QP02, TX/RX switch QT03, drive amplifier QT04, and power amplifier QT02.

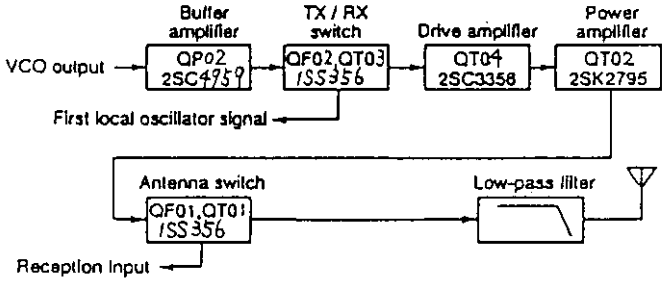


Figure 2-5

2.3.1 Microphone Amplifier

When the user presses the transceiver's PTT switch and speaks into the microphone, the resulting audio signal is applied to pre-emphasis network CM01/RM01 (6dB/oct. frequency characteristics) and is amplified by QM01(1/4). And it is input to pin 6 of microphone amplifier QM01(2/4), where it is amplified approximately 47 dB.
Microphone amplifier QM01(2/4), and it modulates the audio signal by boosting the high-frequency elements. Also, the audio signal has its bandwidth limited by low-pass filter QM01(3/4)/QM01(4/4), which has -18dB/oct. frequency characteristics.
After this, the audio signal is output from pin 14 of low-pass filter QM01(3/4)/QM01(4/4). After the deviation is level adjusted by deviation adjustment point RM19, the audio signal is applied to VCO variable capacity diode QV03, which performs frequency modulation on the radio-frequency signal.

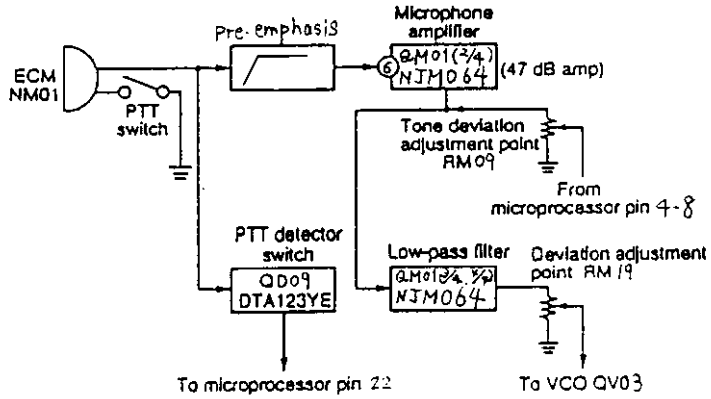


Figure 2-6

2.3.2 Power Amplifier Circuit

The RF signal output from the VCO is amplified approximately 8 dB by QP02. Then it passes through TX/RX switch QT03, is amplified approximately 20 dB by QT04, and is applied to QT02.
The RF signal power amplified by QT02 passes though antenna switch QT01 and, harmonics are eliminated by filter, is radiated by the antenna.

2.3.3 Tone Encoder Circuit for Group Mode

When the transceiver is group mode, the CTCSS signals is synthesized by microprocessor QD02 and applied as pulse waveform on I/O lines Pin4-8. The I/O lines are applied to a resistive digital-to-analog converter network (consisting of RD06-RD11) which produce a pseudo-sine wave for CTCSS at its output. The waveform is smoothed by low-pass filters QM01(3/4)/QM01(4/4) to produce an acceptable sine wave output. The CTCSS tone signal is adjust to the proper level by RM09. The tone signal output from low-pass filter QM01(3/4)/QM01(4/4) is applied to the same VCO variable capacity diode QV03 as the audio signal, which frequency modulates the radio-frequency signal.

2.4 Control Block

2.4.1 Microprocessor QD01 Control

- Reset Circuit –

The purpose of the reset circuit is to prevent the microprocessor QD02 from malfunctioning due to low voltage.
If the power supply voltage drops to approximately 2.7 V or lower, the output from the RESET IC becomes low level, causing the microprocessor QD02 to reset.
To ensure that stable memory write processing occurs when the microprocessor is reset, QD02 does not write data to the EEPROM QD03 if the power supply voltage is approximately 3V or lower.
When the power supply voltage is approximately 2.7 V – 3.0 V, transceiver setting are not backed up in memory.

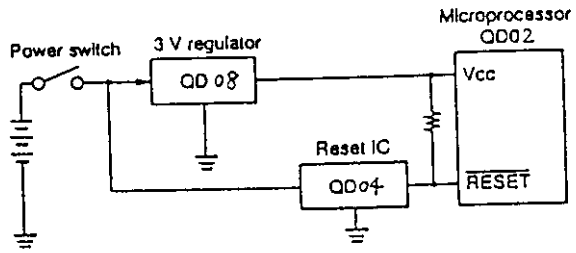


Figure 2-7

2.4.2 Microprocessor I/O Port Description

Table 2-1

Pin	Port Name	In/Out	Function
1	LOWBAT	A/D7	Terminal Voltage
2	SMETER	A/D6	S-METER detected
3	UNLOCK	In	Low:Unlock status
4	CTCD4	Out	CTCSS tone output terminal D4
5	CTCD3	Out	CTCSS tone output terminal D3
6	CTCD2	Out	CTCSS tone output terminal D2
7	CTCD1	Out	CTCSS tone output terminal D1
8	CTCD0	Out	CTCSS tone output terminal D0
9	/EEPSW	In	EEPROM data enable SW
10	TXBON	Out	High:RF transmitter power supply on status
11	TONEDET	In	CTCSS Tone receiver circuit on status
12	BEEP	Out	Beep output terminal
13	SQLMUTE	Out	High:Squelch on
14	FSKOUT	Out	FSK signal output status
15	RXBON	Out	Low:RF receiver power suplly on status
16	EEPDAT	In/Out	EEPROM serial data
17	DIODD1	In	Type data D1
18	DIODD0	In	Type data D0
19	TXDATA	Out	Program data Tx status
20	RXDATA	In	Program data Rx status
21	POWSAV	Out	High:RF receiver saver status
22	PTTSW	In	High:PTT input
23	/TESTMD	In	Low:test mode
24	/SQIN	In	Low:Busy signal status
25	RESET	In	Reset input
26	Xcin	-	Not connected
27	Xcout	-	Not connected
28	Xin	In	System clock(4.194MHz)input
29	Xout	Out	System clock(4.194MHz)Output
30	Vss	-	Ground potential
31	/TXLED	Out	Low:Tx LED lit
32	/TXLED	Out	Low:Tx LED lit
33	/BUSYLED	Out	Low:Busy LED lit
34	/BUSYLED	Out	Low:Busy LED lit
35	/MONISW	In	Low:Monitor key on status
36	/DOWNSW	In	Low:▲key on status
37	/UPSW	In	Low:▼key on status
38	/FUNCSW	In	Low:Function key on status
39	LCDLAMP	Out	High:Lamp lit
40	MICMUT	Out	High:MIC Mute on status
41	PLLCLK	Out	PLL clock output
42	PLLDAT	Out	PLL data output
43	PLLCS	Out	PLL data latch
44	AUDIOB	Out	High:AF amplifier
45	P11	Out	PLL PS output
46	P10	Out	Not connected
47	SEG23	Out	LCD segment signal output
48	SEG22	Out	LCD segment signal output
49	SEG21	Out	LCD segment signal output
50	SEG20	Out	LCD segment signal output

Table 2-1

Pin	Port Name	In/Out	Function
50	SEG20	Out	LCD segment signal output
51	SEG19	Out	LCD segment signal output
52	SEG18	Out	LCD segment signal output
53	SEG17	Out	LCD segment signal output
54	SEG16	Out	LCD segment signal output
55	SEG15	Out	LCD segment signal output
56	SEG14	Out	LCD segment signal output
57	SEG13	Out	LCD segment signal output
58	SEG12	Out	LCD segment signal output
59	SEG11	Out	LCD segment signal output
60	SEG10	Out	LCD segment signal output
61	SEG9	Out	LCD segment signal output
62	SEG8	Out	LCD segment signal output
63	SEG7	Out	LCD segment signal output
64	SEG6	Out	LCD segment signal output
65	SEG5	Out	LCD segment signal output
66	SEG4	Out	LCD segment signal output
67	SEG3	Out	LCD segment signal output
68	SEG2	Out	LCD segment signal output
69	SEG1	Out	LCD segment signal output
70	SEG0	Out	LCD segment signal output
71	Vcc	In	Positive power suplly terminal
72	Vref	In	A/D converter reference voltage input terminal
73	AVss	In	A/D converter reference ground potentail input terminal
74	COM3	Out	Not connected
75	COM2	Out	Not connected
76	COM1	Out	LCD common signal output
77	COM0	Out	LCD common signal output
78	VL3	Out	LCD drive power suplly terminal
79	VL2	Out	LCD drive power suplly terminal
80	VL1	Out	LCD drive power suplly terminal

Display indications