uniden®
SRC

PC Card System Design Document

Document #6410-0003

Revision History

Revision	Issue Date	Originator	Description
1.1	4/30/97	R. Kumar	First open project-wide release. - compiled from individual chapter documents provided by Jonathon, Rich, David Crandall, W. Rou, H. Eassie, N. Nguyen, K. Luu, Tri Le
1.2	5/7/97	R. Kumar	Updated RF chapter to include discrete external-to-asic DACs
1.3	TBD	R. Kumar	Release for SRC inspection process

Uniden San Diego Research and Development Center
San Diego, California 92121

1. Introduction

1 Purpose

This document describes the design approach of the Uniden CDPD PCMCIA Type II device design considerations code named PC-card. The Uniden CDPD PC-card shall comply with the CDPD (Cellular Digital Packet Data) Specification Release 1.1, 19th January 1995.

PC-card is intended to be a consumer product to allow an add-on wireless communication capability for laptop PC or PDA users.

For this design to be suitably used with a portable computer, it is necessary to satisfy the PCMCIA type II mechanical form factor, and the low power consumption requirements. To facilitate the host computer control interface, it is also necessary for this device to satisfy the portable PC operating system (OS) environment, which is currently assumed to be Microsoft Windows PCMCIA interface data services. This design is based on the CDPD full duplex mode operation.

Operationally, this product shall comply with CDPD system specifications mentioned above with all the advanced features such as Sleep Mode, Broadcast, Multicast and ZAP.

2 Scope

This document is divided into 7 chapters.

Chapter 1	This introductory chapter.
Chapter 2	This chapter provides the system design and partitioning of the hardware components of the product.
Chapter 3	This chapter explains the system design and partitioning of the software components of the product.
Chapter 4	This chapter focuses on the mechanical system design of the product.
Chapter 5	This chapter provides a narrative description of operational states and detailed analysis of issues such as power consumption.
Chapter 6	This chapter describes the service and maintenance methodology designed into the product, both for production and field service.

3 Applicable Documents

1. Product XYZ Requirements Document, V1.0, 25-December, 1995
2. Product XYZ Design Specifications, V1.0, 26-Decemnber,1995
3. EIA 123 Interface Specifications

4 Open Issues Log

<< Any open issues in the system design are mentioned here..>>

2. Overview of the System

1 Functional Overviews

.1 Hardware functional overview

The physical dimensions and the power consumption requirements drive the system design concept into adopting a single MAC layer ASIC partitioned in such as a way that all non MAC protocol decision related processes are done in ASIC hardware. The main intent of the ASIC partition is to eliminate any computation intensive elements of the system from the MCU so that no DSP class processing power is needed. Furthermore, as power consumption is function of the system clock speed, an overall system clock speed of in the order of 2 Mhz is desirable. A dedicated PCMCIA controller will be used to interface with the host computer. A full duplex cellular transceiver will provided for the airlink interface.

Figure 1.1 shows the overall block diagram of the design.

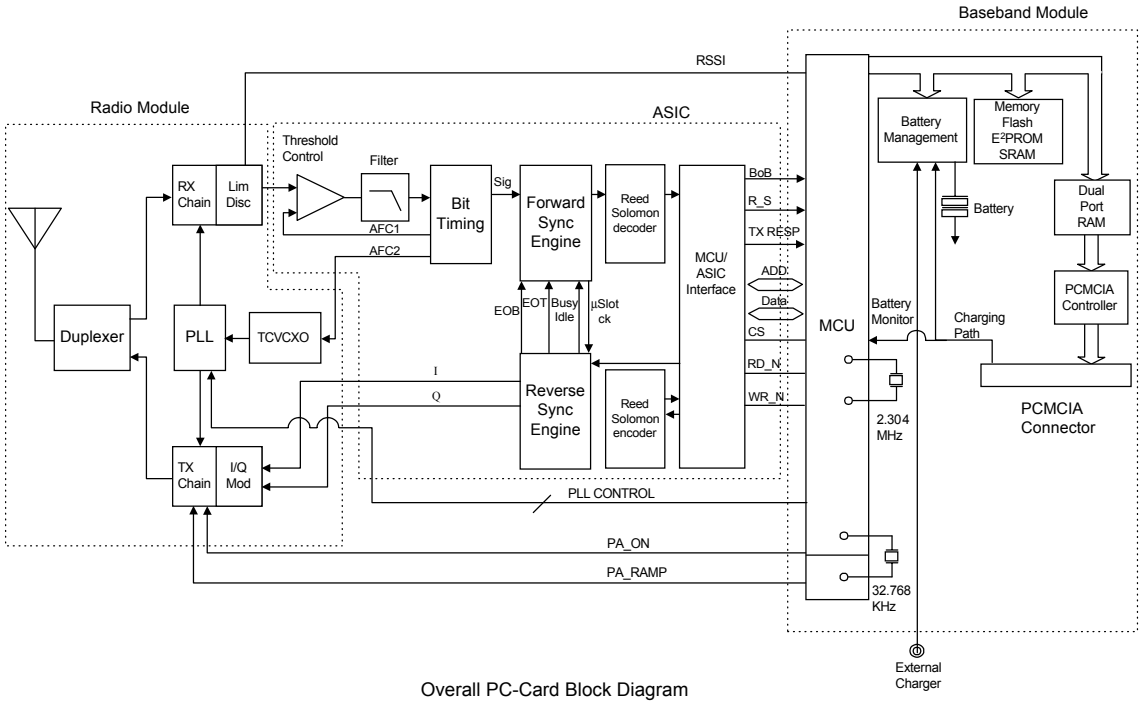


Figure 1.1 Overall hardware functional block diagram

Thus, in the CDPD forward channel, the Channel Interface ASIC will accept raw limiter discriminator output from the transceiver receiver chain and perform low pass filtering and bit recovery. It will also synchronize with the forward channel in minimum time of less than 2 microslots. ASIC is responsible for performing Reed Solomon decoding and it passes the recovered data block to the MCU. In the reverse channel, the Channel Interface ASIC accepts pre-formatted data blocks from the MCU. It appends a 38 bit dotting sequence and negotiates the reverse airlink in accordance to DSMA procedure. A stand alone Reed Solomon encoder is made available to the MCU so that the 16 parity symbols are provided when a raw data block is presented to the encoder.

As it can be seen from Figure 1, the Channel Interface ASIC provides other support functions. It provides AFC control signal and hard limiter threshold level for the forward channel operation. It also provides the power output step size and power output ramp-up ramp-down controls.

The MCU is responsible for interfacing with the Channel Interface ASIC to obtain the incoming data blocks in the forward channel. It executes all layers of the CDPD protocols. The forward channel engine provides the MCU with the status of synchronization by summarizing the majority vote of each of the synchronization flags, the Reed Solomon error correction counts and the decode flags. From these information MCU determines the status of the forward engine synchronization, and it can reset the forward engine operation

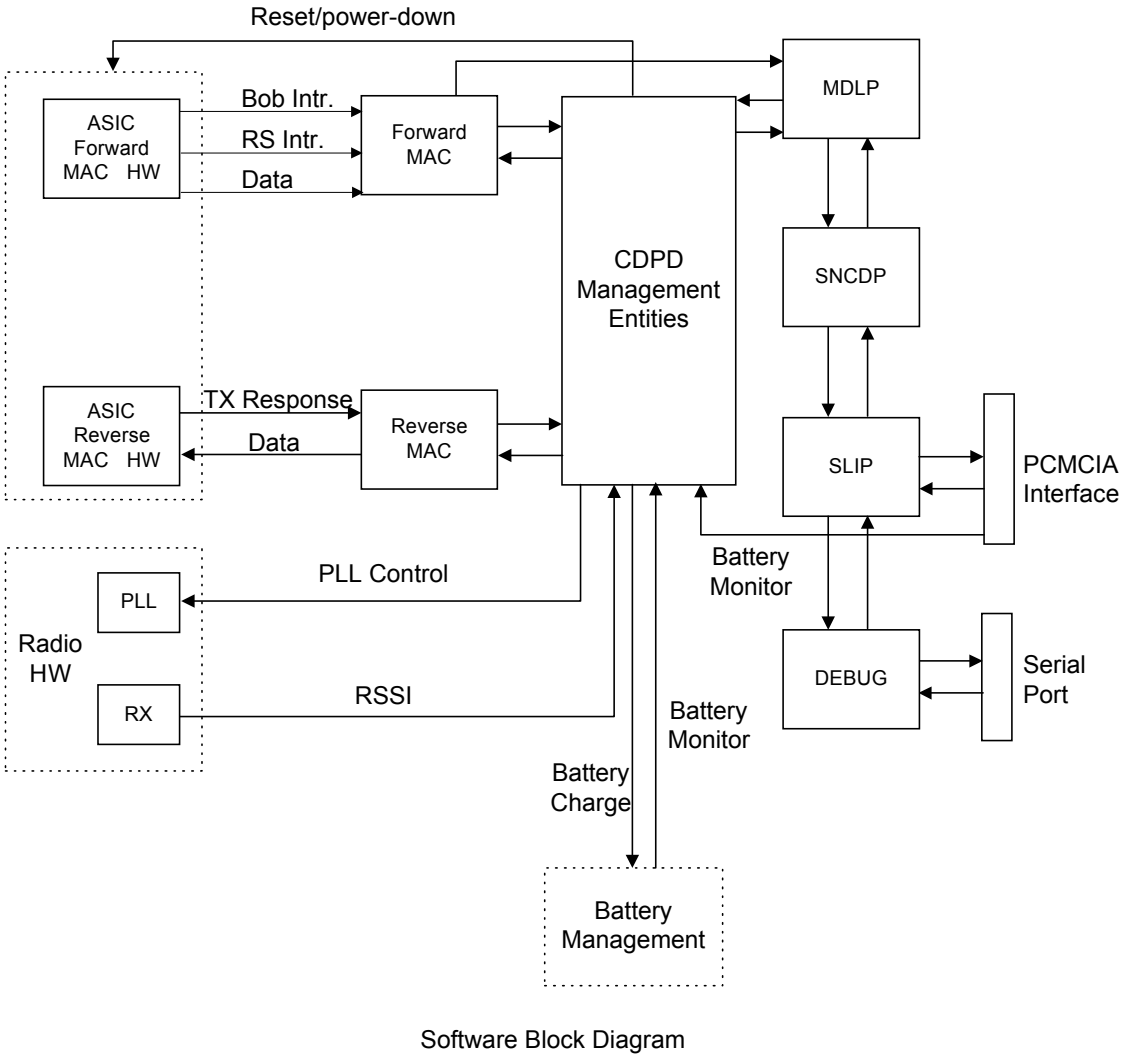
In the reverse channel, MCU dictates all access protocol action by constructing respective data blocks. All formatting of the reverse channel data block such as convolution encoding, interleaving, bit stuffing and continuity flag insertion is completed before the MCU delivers the formatted data block for transmission by the Channel Interface ASIC. MCU controls the state of the reverse channel engine DSMA BACK-OFF and the DEFER states by setting the BACK-OFF/DEFER status bit. Since MCU does not have the microslot timing, the reverse engine will monitor the forward channel BUSY/IDLE flag status and abort a transmission if an IDLE state in the forward channel is detected.

MCU is also responsible for the standby mode time keeping. The only real time reference made available to the MCU is the real time data block time tick generated by the Channel Interface ASIC. As the real time data block time tick is not always available, the MCU must extrapolate the real data block time so that it can keeps time-out periods for MAC operations. This is because the forward channel may not always in synchronization. For two obvious conditions, one is when the forward channel airlink condition is not ideal. The second is when the sleep mode is enforced. During the sleep mode period, MCU is to be powered down by running the slowest clock possible. It keeps the wake-up time. The standby routine must be adaptive to adjust to error conditions and be able to recover from errors in time keeping.

MCU shall maintain the current handling capacity of the built-in re-chargeable battery. The re-chargeable battery will obtain charging power from the PC when the PC is on charge, otherwise, the re-chargeable battery is the primary power source. The PC configuration shall provide a TSR capable of informing the PCMCIA port of the power charging state.

.2 Software functional overview

All CDPD control protocols are maintained by the PC-card software suite, such that the PCMCIA card appears like a standard wireline modem to the host computer. Figure 2 shows the high level software block diagrams.



Software Block Diagram

Figure 1.2 Software functional block diagram

In Figure 1.2, all unlabelled arrows represent the CDPD primitives defined in the CDPD specifications. All hardware interfaces which are localized to the PC-card, are labelled accordingly.

The forward MAC engine hardware is directly interfaced with the software forward MAC module through two interrupt lines:

- Begin of Block (Bob)
- Forward_MAC_status (previously known as RS)

Begin_of_Block interrupt occurs at the rising edge of every new forward data block. This interrupt is asserted at real time, when the hardware forward sync engine receives the block. This is the only real time, time reference the software has other than its local systems clock generated by a 20 ppm crystal. Software will periodically measure this duration between two Bob interrupts to calibrate its data_block_time. In this way, time_out and sleep time can be measured using data_block_time as the time unit.

Forward_MAC _status interrupt is asserted by the ASIC hardware when the ASIC forward sync engine status or data registers are updated. Details of the relevant registers related to this interrupt are described later in the Forward Sync Engine section of this document.

The reverse MAC engine hardware interacts with the software reverse MAC module through the following interrupt:

- TX_Response

TX_Response interrupt is generated when the reverse sync engine hardware have completed the reverse channel access task either successfully or otherwise and sync engine status registers are updated . Details of the registers related to this interrupt are available in the reverse sync engine section of this document.

The CDPD management entity which controls the Radio Resource Management entity as defined by the CDPD specification 1.1, determines the radio transceiver frequency synthesizer settings. In this way, the CDPD management entity changes the airlink frequency in accordance to the CDPD specification.

The CDPD management entity monitors both the battery voltage for the battery management block and the RSSI of the incoming signal from the receiver.

The forward MAC module together with the CDPD management entity presents the data for MDLP use. MDLP and SNDCP are the link layer.

3. Baseband Architecture

1 System Description

A Block Diagram of the PC Card is shown in Figure x, below. The system consists of a M16C60 Microcontroller(MCU), a channel interface ASIC, 128Kx8 SRAM, 1Mx8 Flash memory, PCMCIA Adapter, Battery Management circuit, and a Dual Port Ram.

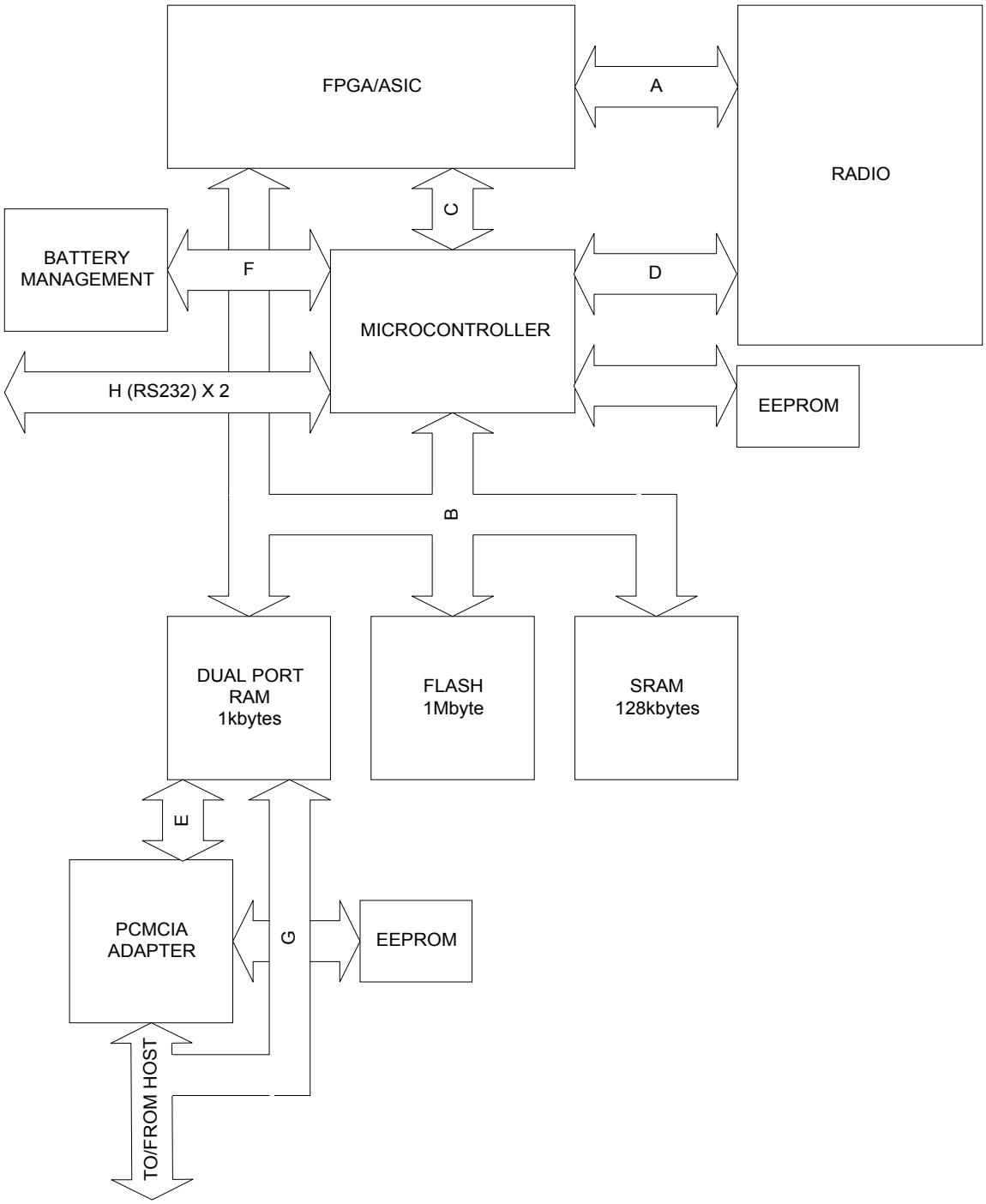


Figure 1 PC Card CDPD Modem Block Diagram

2 Overview

The following discussion relates to two designs. The first design is a test bed used for development of the PC Card CDPD modem, while the second design relates to the final product. The architecture of the two designs is similar, while the implementations are somewhat different, and are detailed in a later section.

The modem is controlled by the Host through the PCMCIA Adapter. Local control of the modem is achieved with the microcontroller (MCU). The Host communicates with the MCU through the Dual Port Ram (DPR), which shall be configured to emulate a 16550 port. The DPR allows the interfacing of two asynchronous bus masters (the PC Card bus and the MCU's local bus). One side of the DPR is mapped into the MCU's memory space, while the other port is mapped into the Hosts memory space. The MCU has 1 MByte of flash nonvolatile memory for code storage, while a 128 KByte static ram (SRAM) is included for volatile variable storage. A FPGA/ASIC performs the channel interface functions, and is memory mapped into the MCU's address space. The MCU controls some Radio functions (PLL and power savings mode directives) and digitizes the RSSI signal from the radio.

3 *MCU*

The M16C60 MCU is selected in this preliminary phase because of its low current consumption, very good interface attributes and the availability of its low profile package size. The MCU is solely responsible for handling all protocol above Data Link Layer and together with the channel interface ASIC. It is also responsible for the Data Link Layer including the MAC protocol interface with the ASIC. In addition to handling the communication protocol, the MPU is also responsible for power management, radio configuring (PLL, etc.). The MCU has an on chip ADC that is used for RSSI monitoring and an on chip UART that provides a pair of RS232 links for debugging purpose on the test bed. In addition one of the two RS232 links may be made available in TTL signal level format to the user. Other M16C features include a watchdog timer, 8 timers, a CRC calculation circuit, and a 1MB addressing range.

.1 Memory Map

The MCU does its first of 4 successive fetches of the reset vector from 0FFFFCH, which means a top boot Flash Memory is required. Up to a 1 MByte flash will be available in the test bed and the fit product. (A 256Kbyte or 512 kByte flash may be substituted). Note that because of the way chip selects are decoded in the MCU, only 832 KBytes of the flash will be available. A 1Kbyte Dual Port Ram is mapped into the MCU space, as well as a 128Kbyte sram. All memory will operate with 0 wait states. The MCU memory map is as follows:

00000 ->003FFH		SFR AREA
00400 ->02BFFH		INTERNAL RAM
04000 ->07FFFH	CS3/	ASIC (LOWEST 512 BYTES OF 16K)
08000 ->27FFFH	CS2/	SRAM (128K)
28000->2FFFFH	CS1/	DPRAM (LOWEST 1K OF 32K)
03000->FFFFFH	CS0/	FLASH (LOWEST 832K OF 1 MB)

Note that the MCU is run in microprocessor mode. Accesses to the dual port ram should be minimized to minimize power consumption.

.2 Interrupts

The interrupt structure is as follows:

NMI/: reset switch on test bed, tied to logic 1 in fit product
INT0/: FEI/: Forward Engine Interrupt..reference ASIC portion of this document for definition
INT1/: RTSOB/: Real Time Start of Block reference ASIC portion of this document for definition
INT2/: TXR/: Transmit Response Interrupt reference ASIC portion of this document for definition
KL0/: DPRintl/: Dual Port Ram Interrupt: Indicates that the Host Processor has written into memory location 043FEH

In addition the MCU can interrupt the Host (for notifying the HOST that receive data is ready) by writing into location 043FFH;

Note that the Dual Port Ram Interrupts are cleared by reading locations 043FEH or 043FFH.

.3 Analog Inputs

The MCU contains a 10 bit A/D with multiplexed inputs. The first input (AN0) is the Radio Signal Strength Indicator from the Radio Module. The second input (AN1) allows the MCU to read the battery voltage. A third input (optional) is a temperature sensor, characteristics tbd.

.4 Clocks

The MCU shall be clocked using a high speed and low speed clock, controllable by software. The low speed clock (32.768 khz) is selected for low power operation, while the high speed clock (18.432 Mhz/8 = 2.304 Mhz) is selected for normal operation.

4 Dual-port Ram

A DPR bridges the PC Card Bus to the MCU bus. Writing to the last two locations in the memory causes an interrupt on the other side of the DPR, which can be cleared by the interrupted side reading that location. Transmit and received data is passed through the DPR, as well as any status bits required. In addition the DPR may contain CIS information, loaded by the MCU.

5 PCMCIA Adaptor

The PCMCIA Adapter provides the Configuration Options Register (COR), the Card Configuration and Status Register (CCSR), Configuration Information Structure (CIS) register, and Pin Replacement Register (PRR), as well as an interface to a serial eeprom for nonvolatile storage of configuration information.

6 Flash Memory

The Flash Memory is up to a 1MByte device mapped into the CS0/ region of the MCU's memory space. A 256 kByte or 512 kByte device may be substituted. It is a top boot device, which means that its top sector can be protected against accidental erasure. A jumper will be provided in an accessible portion of the extended portion of the PC Card which when installed, will force the code to stay in the boot section of software. This bit shall be connected to P10, bit 7, and is high for normal operation, low when the code should stay in the boot monitor.

7 Interfaces

The following tables describe the interfaces between the modules described in Figure 1. Note the letter in the bus of interest and then reference the appropriate table, below.

4. CDPD Channel Interface ASIC

The CDPD Channel Interface ASIC is responsible for performing a number of baseband processing functions for the PCMCIA Modem Card including bit timing recovery, Forward Channel synchronization, Forward Channel decode status flag extraction, Forward Channel Reed-Solomon decoding, Reverse Channel Reed-Solomon en-coding, Reverse Channel DSMA "defer" control, Reverse Channel dotting sequence and sync flag insertion, and the Reverse Channel GMSK modulation.

The CDPD Channel Interface ASIC is implemented as a standard cell, mixed signal ASIC of approximately 40,000 equivalent gates and is housed in a 48-pin TQFP package. The primary need for mixed signal capability is to accommodate the five DACs required for digital-to-analog signal conversion.

The operational voltage for the ASIC is 3.3 volts and its current consumption design goal is 3mA . In order to minimize power, low-power design features are included such as global and localized clock control to the various digital subsystems, and power-down control to the analog subsystems.

A pinout diagram for the CDPD Channel Interface ASIC is provided in Figure 5-1. In addition, this diagram includes the proposed floorplan for the various subsystems within the ASIC. This floorplan takes into consideration the relative sizes of the various subsystem blocks and is layout to best accommodate signal routing to adjacent blocks and to the external inputs and outputs. Digital and analog subsystems are physically segregated to minimize digital crosstalk into the analog functions.

A detailed list of each I/O signal is provided in Table 5-1 along with a brief description of each signals specific function.

1 *Functional Description*

A block diagram of the CDPC Channel Interface ASIC is shown in Figure 5-2. As can be seen in this block diagram, the ASIC consists of a number of functional blocks including the Bit Timing Recovery/ LPF, the Forward Engine, the Reverse Engine, the Reed Solomon Decoder, The Reverse Engine, and the Microprocessor Interface Decoder. A brief description of each of these blocks is provided in the following subparagraphs.

Bit Timing Recovery/ LPF

The Bit Timing Recovery and digital low-pass filter (LPF) functions reside at the front-end of the receive chain and are responsible for recovering the clock from the incoming data and providing an estimate of the frequency and signal offset levels. The 19.2 kHz recovered clock and data are then passed onto the Forward Engine where they are re-synchronized to the ASIC system clock (2.xxx MHz) and subsequently processed.

Forward Engine

The Forward Engine receives the recovered 19.2 kHz clock and data and performs the following tasks:

- Synchronization to the incoming data stream, thereby establishing the micro-slot and data block boundaries

- Extraction of the decode status flags from each received blocks. These decode status flag bits are passed onto the Microprocessor for subsequent processing

- Soft-decision calculation on each of the seven 5-bit sync flags received for each data block. These soft-decision bits are passed onto the Microprocessor for subsequent processing

- Detection/decode of the Busy/Idle flags which are then passed onto to the Reverse Engine

- Stripping out the control-bits from each data block received before transferring the remaining Reed-Solomon encoded data bits to the Reed Solomon Decoder

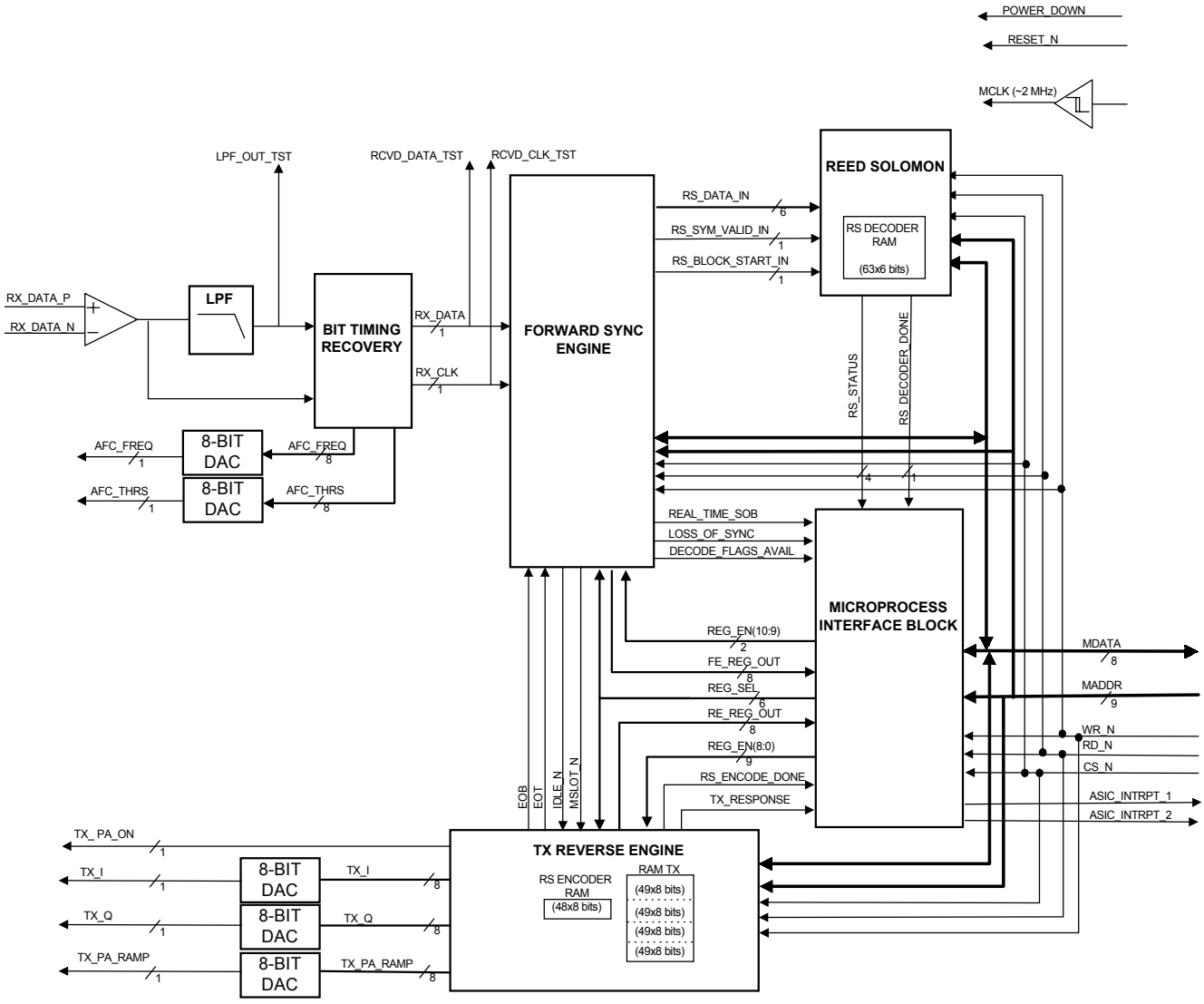


FIGURE 5.2 - PCMCIA ASIC BLOCK DIAGRAM

ASIC BLOCK DIAGRAM.vsd
4-15-97

Reverse Engine

The Reverse Engine receives transmit data from the Microprocessor and is responsible for the following tasks:

- RS Encoder. Receiving unencoded transmit data from the Microprocessor and performing the Reed Solomon Encoding calculation. This calculation results in a 16-bit parity word that is available to the Microprocessor for subsequent formatting of the final transmit data. This interface will consist of the Microprocessor writing the unencoded data block to R.S Encoder RAM which is resident in the Reverse Engine. Upon writing the complete unencoded block into RAM, the processor will write a single bit to a control register resident in the ASIC indicating a data block is available

for Reed-Solomon Encoding. Upon detecting this bit being set, the Reverse Engine will then clear the bit and perform the necessary Reed-Solomon encoding. Upon calculating the 16-bit parity word, the Reverse Engine will write the results to the end of the RS Encoder RAM, appending it to the unencoded data. It will then interrupt the processor indicating the calculation is complete and the parity word is available to be read.

- Reverse Data Transmission Controller. The Reverse Data Transmission Controller will perform the necessary control required to organize and transmit the final TX data stream. This includes interleaving the dotting sequence, synch bits, and data block provided by the Microprocessor, and performing the necessary DSMA "defer" control.

- GMSK Modulation. The GMSK Modulator will take in a serial bit-stream and uses a look-up table to generate the required 8-bit digital I and Q words needed to perform the GMSK waveform modulation. This eight-bit I and Q words will then drive 8-bit DACs that will reside *internal* to the ASIC, thereby developing the I and Q analog signals required to drive the radio transmit subsystem. Any necessary analog filtering will reside external to the ASIC.

- Ramp Function Generator. The Ramp Generator will provide the power control ramp necessary to control the TX power amplifier ramp-up and down control. The design used to implement this function will consist of a look-up table of values that will be cycled through in order to generate the required ramp-up and ramp-down profile.

Microprocessor Interface Decoder. The Microprocessor Interface Decoder will act as a general clearing house for address decoding of ASIC control register addresses, and perform the data multiplexing of return status from the ASIC to the Microprocessor.

- Interrupts. A single interrupt is currently being proposed which is an aggregate of all six interrupt sources internal to the ASIC. The six interrupt sources include; "START_OF_BLOCK", "LOSS_OF_SYNC", "DECODE_FLAGS", "RS_DECODE_DONE", "TX_RESPONSE", and "RS_ENCODE_DONE". In order to distinguish which particular interrupt source internal to the ASIC is responsible for initiating the external interrupt line to the processor, a six-bit interrupt flag register will be set indicating which interrupt sources was responsible for initiating the interrupt line. Provisions for a second interrupt line to the Microprocessor are also under consideration if required by the processor. If the need arises for this additional interrupt line, this document will be updated to describe the specific mechanism of this additional interrupt.

- Addressing Mapping. Approximately347 address locations are required by the ASIC. The specific memory/address requirements are as follows –

  Tx RAM -- 2x98 (x 8 bits wide) = 196 address
  Reed-Solomon Encoder RAM – 48 (x 8 bits wide) = 48 address
  Reed Solomon Decoder RAM – 63 (x 6 bits wides) = 63 address
  Configuration Registers – 40 address

These 347 address locations will require a 9-bit address field in order to address all the require locations. The memory block address assignments are as follows --

Maddr(8:0)	**Memory/Address Block**
00xxxxxx	TX_RAM
01xxxxxx	RS_Decoder_RAM
10xxxxxx	RS_Encoder RAM
11xxxxxx	Configuration Registers

2 Power Control

In order to minimize power consumption, the capability to gate the system clock provided to each of the major digital subsystems is provided. The technique employed for gating the system clock to the digital subsystems utilizes a standardized clock control circuit as shown in Figure 5-3. A timing diagram is also provided to illustrate the on/off control to the clock control circuit as well as the waveform for the glitchless gated clock that results.

Note, as the clock control circuit operates on the negative edge of the clock, the CMD_ON and CMD_OFF signals should be transferred on the positive clock edge of the sending unit in order to provide mid-bit signal transfer and hence avoid potential problems due to clock skew.

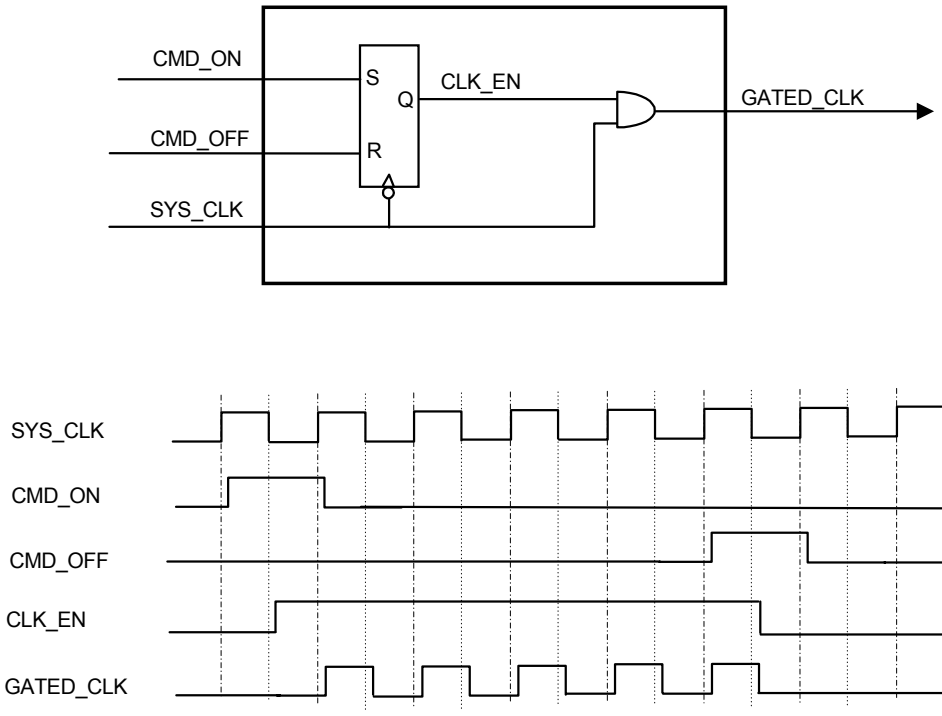


FIGURE 5.2 - GENERAL PURPOSE CLOCK CONTROL SCHEME ck_ctrl2.vsd 3-5-97

An individual clock control circuit will be provided for the Forward Engine, the Reed-Solomon Decoder, the Reed Solomon Encoder, and the Reverse Engine. A block diagram showing the basic architecture of the clock-control scheme is shown in Figure 5-4.

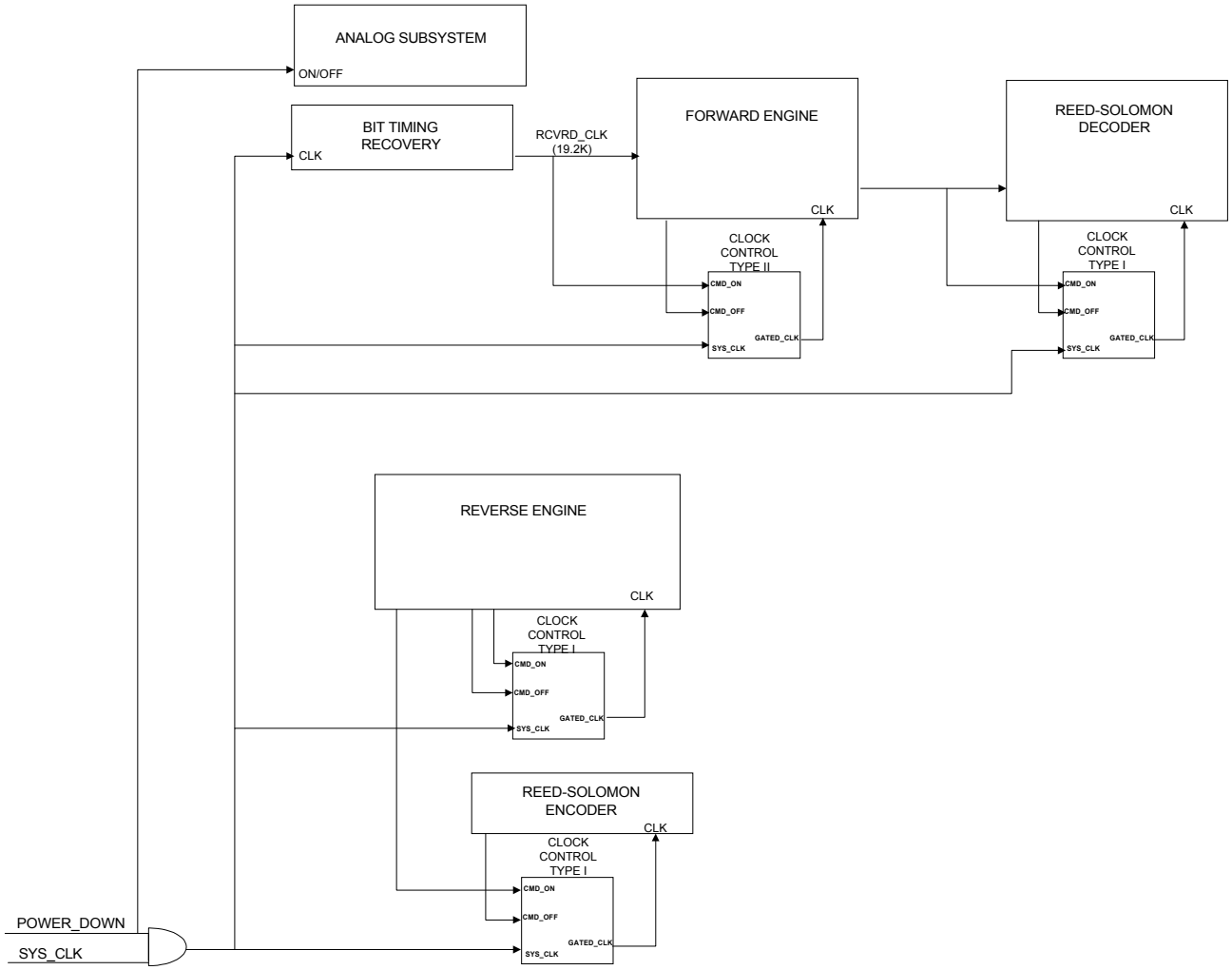


Figure 5.4 Power Control Block Diagram

CLK_SYS.VSD
4-23-97

5. Bit Timing Recovery and Low Pass Filter

The block diagram for GMSK base band demodulator is shown in Figure 1. The discriminator's output after filtering is compared with a threshold, which is provided by the threshold estimation algorithm, to generate the values of either '0' or '1' by a hard limiter (1bit quantizer). The 1bit quantized signals are latched into the shift registers at the clock rate equlas 153.6KH. The over sampled signals will go through a 4^{th} order Buterworth filter with cutoff frequence equal 12KHz. This 4^{th} order Buterworth filter is implemented by a 25-taps FIR filter with coefficients of (-1, -1, -1, -2, -2, -1, 1, 3, 7, 10, 13, 15, 16, 15, 13, 10, 7, 3, 1, -1, -2, -2, -1, -1, -1) as shown in Figure 2. The frequency response curves of the filters are shown in Figure 3. The output of this FIR filter is fed into the bit timing recovery circuit.

The bit timing recovery uses zero-crossing locating method. The algorithm finding the zero-crossing sample positions where the previous sample has different sign compared with the next sample.

The zero-crossing location used by bit timing recovery is those zero-crossing sample positions went through a first-order low-pass filter ($H(Z) = 1 / (1-0.984375Z^{-1})$) to average out the jittering caused by noise, interference and distortion.

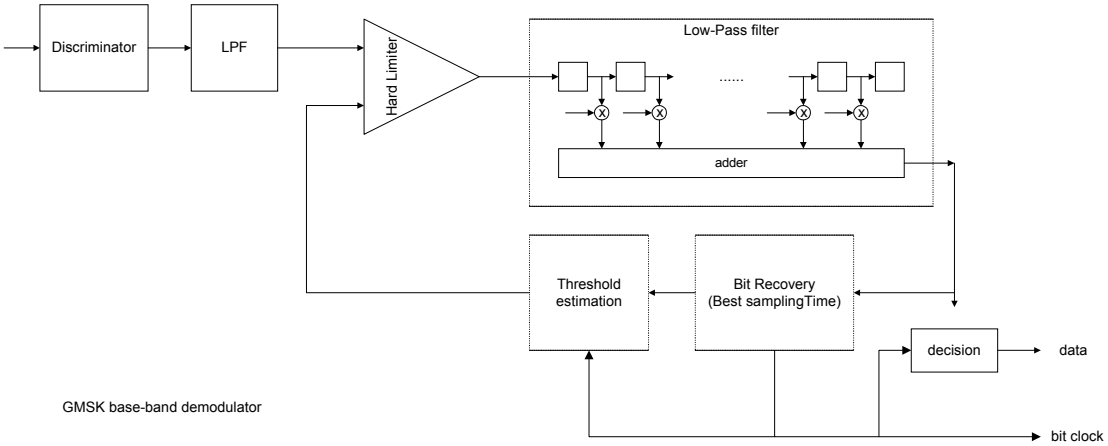


Figure 1 : Block diagram of GMSK base band demodulator

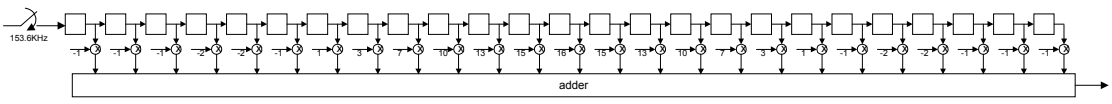


Figure 2 : 4th order Butterworth FIR filter

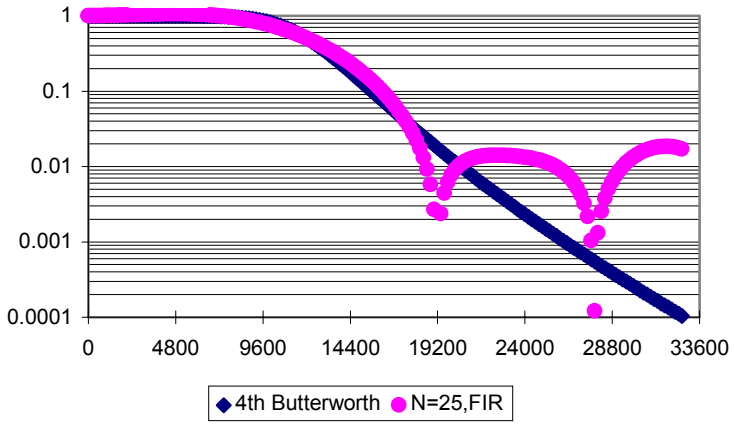


Figure 3 : Frequency response of 4th order Butterworth filter

The best sampling time is the sample position that is half bit away from the zero-crossing location derived above. The bit timing recovery algorithm is shown by a circuit sketch in Figure 4.

The threshold estimation algorithm compares the duration (Td1) of signals been higher than threshold with the duration (Td0) of signals been lower than the threshold. If the Td1 is longer than Td0,

then increases the threshold by 1/256 of the range of discriminator's output. If the Td0 is longer than Td1, then decreases the threshold by 1/256 of the range of discriminator's output. The threshold is then filtered by a first-order low-pass filter ($H(Z) = 1 / (1-0.875Z^{-1})$) to average out the jittering. The filtered threshold is then fed to the hard-limiter.

The performance requirement for Receiver in CDPD specification is to have sensitivity lesser than -113dBm for block error rate lesser than 0.05. With an assumption of 5dB degradation in the RF circuit, the GMSK demodulator needs to achieve bit error rate <0.011 at SNR=11dB. The bit error rate of the above demodulation algorithm is shown in Figure 5.

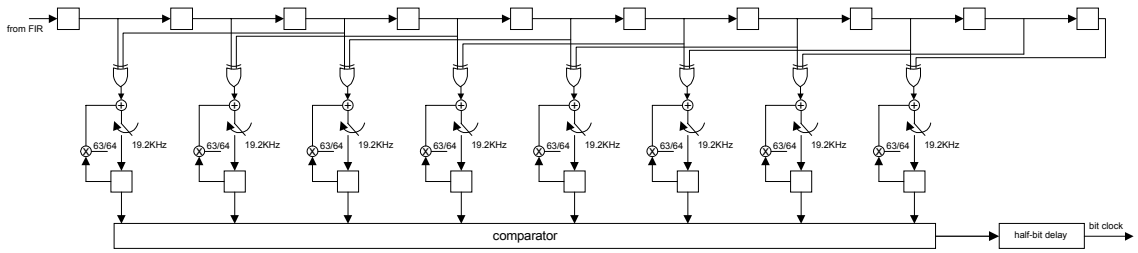


Figure 4 : The circuit sketch of bit timing recoevry algorithm

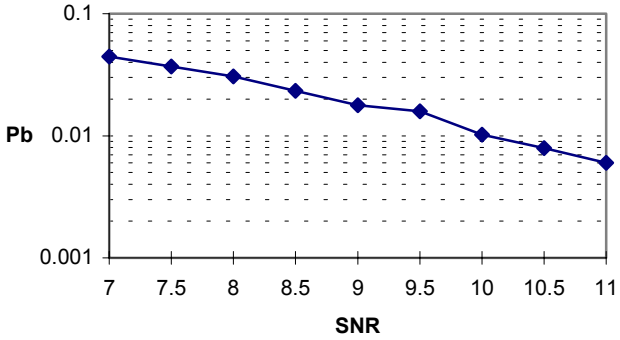


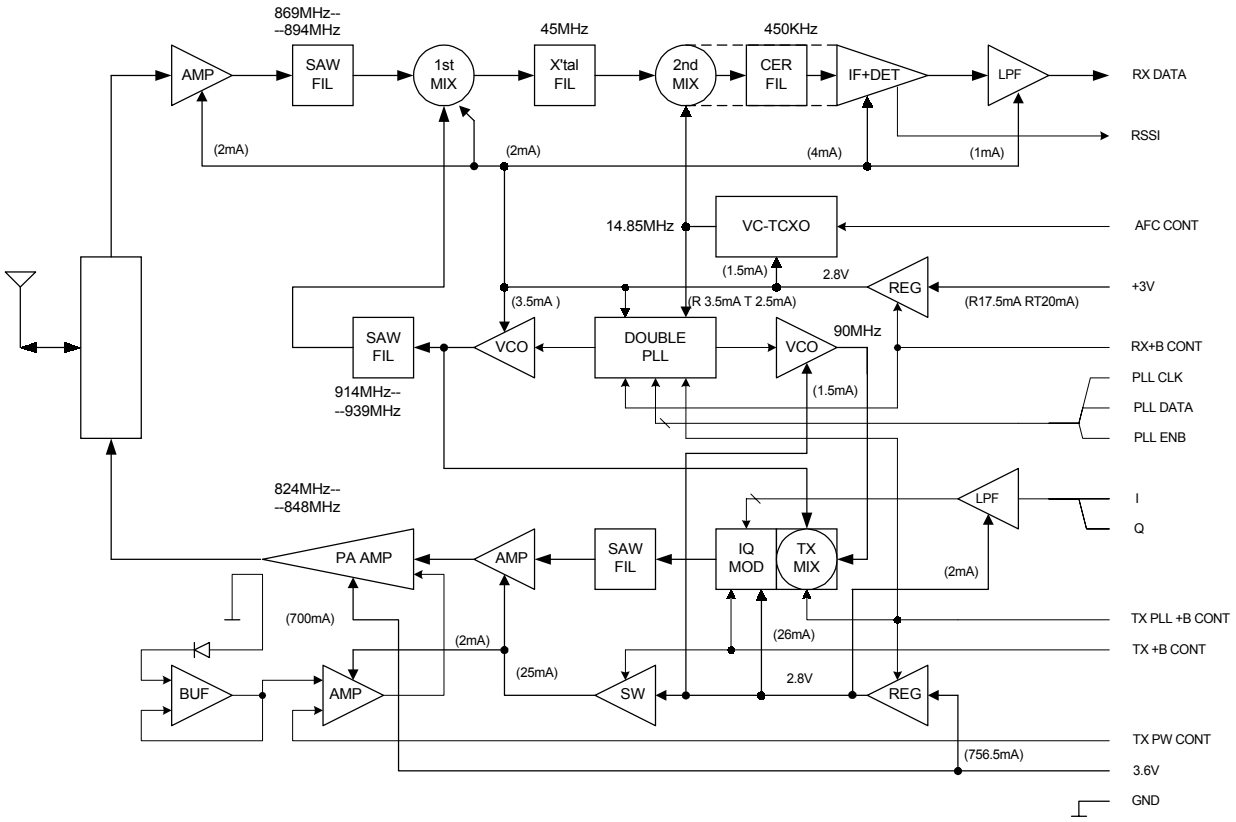
Figure 5 : Performance of the GMSK demodulator

6. RF Hardware

1 Introduction

The radio employs the architecture where the receive synthesizer makes the channel selection and a second synthesizer generates a fixed transmit offset. The block diagram for the radio is shown in figure below. It has three major portions: Receiver, Transmitter and frequency synthesizer.

CDPD PCMCIA TYPE RF BLOCK DIAGRAM



2 Receiver Section

RF inband signal enters the duplexer through the external antenna system. This duplexer has a cutoff frequency of 869 - 894 MHz where emissions outside of this band are well reduced to prevent interference caused by unwanted signals.

The received inband signal is then amplified by approximately tbd dB by the low noise amplifier (LNA) to improve its Noise Figure. This LNA also works as buffer circuit to prevent antenna conducted emissions in the antenna circuit.

Then this amplified inband signal goes to the SAW bandpass filter which has cutoff frequency of 869 - 894 MHz. This filter further rejects out of band interference and reduces antenna conducted emissions.

After filtering, the signal is mixed with the 1st LO frequency to provide the first IF at 45 MHz. At this stage, impedance matching for these signal sources are well achieved to isolate the signals from each other to prevent antenna conducted emissions from going toward the antenna.

The 45 MHz 1st IF signal is filtered by the crystal filter which has bandwidth of 34 KHz. After the matching circuit, the 1st IF signal goes to the 2nd Mixer of IF IC which consists of a Mixer, a RSSI detector, an IF amplifier, and a FM quadrature detector. Here it is mixed with the 3rd harmonic of 14.85MHz which is 44.55MHz to generate 450 KHz second (final) IF. This 2nd IF signal is filtered by the ceramic filter which has bandwidth of 30KHz. After being amplified by the IF amplifier, the signal is lowpass filtered with a 3rd order Butterworth LPF with cutoff frequency of 11KHz to 15KHz (will be finalized after performance test is done).

This analog baseband signal then goes to the ASIC for further processing.

3 Transmitter Section

The transmitter employs vector modulation by using the IC from (tbd) which includes IQ modulator and Mixer. Here the LO frequency is mixed with the fixed offset frequency to generate the TX frequency. The TX frequency is then modulated by the I and Q baseband signal from the ASIC after they have been lowpass filtered.

Modulated carrier signal is then amplified and buffered by driver amplifier to prevent any affects caused by any incidental load change at TX power module. The amplified TX signal then goes to TX SAW filter where the frequency components other than 824-849 MHz are reduced to prevent the spurious emissions from the TX carrier.

As a final amplifier stage, the TX power module is used to amplify the 0dBm input signal to the required transmission power level. The amplified signal then enters the duplexer where final filtering is provided to prevent harmonics and spurious emission of the transmitter.

The directional coupler picks up the -14 dBm down level of TX power and then it is detected by detector diode. The detected power level is compared with the logic system's voltage in order to obtained the required TX output power level. During production, comparator setting voltages are calibrated and stored in EEPROM for channel v.s. TX power. This corresponding voltage is then used to set the required output TX power.

On the other hand, TX +B switching transistor is used to stop the regulated DC power to the TX circuit to prevent spurious emissions when the unit is not in TX mode.

4 Performance Specifications

TX spec

Description	Designed spec	Comments
Output frequency range	824.04MHz - 848.97MHz	Channel 991 to 1023 and 1 to 799

Channel spacing	30KHz	
Output power	0.6W +2dB and -4dB	MES Class III
Frequency accuracy	± 2.5ppm	With AFC
Phase noise	-55dBc/Hz at 1KHz offset -75dBc/Hz at 10KHz offset	
Channel switching time	10ms for 25MHz jump <2ms for 30KHz jump	tentative tentative
Transmitter ON/OFF switching time	<2ms	
Radiated harmonic and spurious emission	< -[43+10(logPout)] dBc	Minimum -40.78 dBc
Conducted harmonic and spurious emission	< -[43+10(logPout)] dBc	except within 75KHz of carrier frequency.

Rx Spec

Description	**Designed spec**	**Comments**
Input frequency range	869.04MHz - 893.97MHz	Channel 991 to 1023 and 1 to 799
Rx sensitivity in AWGN (Es/No = tdb dB for 5%BLER)	-111dBm	Small form factor
Rx sensitivity in Rayleigh Fading	-98 dBm at 8km/hr -100 dBm at 50km/hr -101 dBm at 100km/hr	small form factor MES
Cochannel Interference Ratio in Rayleigh Fading and Delay	17dB and 8uS	
Rx adjacent channel selectivity	16dB at 30KHz 57dB at 60 KHz	adjacent channel alternate channel
Receiver Intermodulation spurious response	57dB	
RSSI	± 6dB absolute ± 3dB relative	
Radiated spurious emission	< -45 dBm < -41 dBm < -41 to -32 dBm log scale < - 32 dBm <-32 to -26 dBm log scale	25-70MHz 70-130MHz 130-174MHz 174-260MHz 260-470MHz

	< -21 dBm	470-1000MHz
Conducted spurious emission	< -80 dBm	869.04-893.97MHz
	< -60 dBm	824.04-848.97MHz
	< -47dBm	Everywhere else

5 Power Consumption

The power consumption for the receiver section is determined as follows:

RX current = LNA + Mixer + IF IC + LPF + VCOrx + PLLrx + VC-TCXO

= 2mA + 2mA + 4mA + 1mA + 3.5mA + 3.5mA + 1.5mA = 17.5mA

and for transmitter:

TX current = IQ Mod + Driver Amp + LPF + VCOtx + PLLtx + Pwr Cntl Amp + PA

= 26mA + 25 mA + 2mA + 1.5mA + 2.5mA + 2mA + 500mA = 558mA

6 Protection against False Transmission

Since the ASIC has control of the TX carrier ON/OFF circuit, it should monitors this signal to determine if the carrier is on more than 10 seconds and shut it off. This is equivalent to monitoring the output power to determine if the carrier is on for more than 10 seconds. Because to shut the carrier off, the control signal must be in working condition which should reflects the state of the carrier.

7 Frequency Synthesizer and Reference

The synthesizer consisting of Dual PLL Frequency Synthesizer IC (MB15F02L) from Fujitsu, a UHF VCO, a 90MHz VCO, and reference VCTCXO 14.85MHz. This 14.85 MHz VCTCXO is a $\pm$ 5 PPM crystal oscillator but it is stabilized well within $\pm$ 2.5 PPM, in the temperature range of -20 deg C to +70 deg C, by the automatic frequency control (AFC) algorithm employed in the ASIC. The RX LO frequency is generated using RF PLL of the Dual PLL IC. The 90MHz TX Offset frequency is generated using IF PLL.

The control of the frequency synthesizer is done through a 3-wire serial interface (Data, Clock, and LE). See the data sheet of MB15F02L for further information.

.1 Programming Information

XTALS: 14.85MHz **(Fosc)**
IF1: 45MHz
IF2: 450KHz
RX LO Ref: 30KHz **(RF Ref)**
RX LO Freq: Rxfreq+45MHz **(RF Fvco)**
TX Offset Ref: 150KHz **(IF Ref)**
TX Offset Freq: 90MHz **(IF Fvco)**

IF PLL Settings:

Reference Counter: R = Fosc/ Ref = 14.85MHz/150KHz = 99 =>**R = 99**;
Using the following equation for programmable counter and swallow counter for IF-PLL:
Fvco = {(MxN) + A} x Fosc/R
We have: Fvco = 90MHz ; Fosc = 14.85MHz; R =99
⇨ (MxN) + A = Fvco x R / Fosc = 600
Set **SW = 1** (Divide ratio for the prescaler = 16/17)
⇨ **M =16**
⇨ **N** = Integer(600/16) **= 37**
⇨ **A** = 600 - (MxN) = 600 - 592 **= 8**
Summarize of IF PLL setting

R = 99
N = 37
A = 8
SW = 1
FC = 1 (phase control bit)

RF PLL Settings:

Reference Counter: R = Fosc/ Ref = 14.85MHz/30KHz = 495 =>**R = 495**;

RF PLL Frequency, Fr:
Fr = 915 + [Channel Number * 0.03] (1)For Channel Numbers: 1 to 866
Fr = 915 + [[Channel Number -1023]* 0.03] (2) For Channel Numbers: 991 to 1023
Division Ratio, Div:

$$Div = \frac{Fr}{0.03} \quad . \qquad (3)$$

Combine equations (1), (2) and (3) for Div:

Div = Channel number + 30500 (4) For Channel Numbers: 1 to 866

Div = Channel number + 29477 (5) For Channel Numbers: 991 to 1023

Set **SW = 1** (Divide ratio setting = 64/65) => **M = 64**

$$\left\lfloor \frac{DIV}{64} \right\rfloor \text{ mod} = \mathbf{N} \qquad (6)$$

$$\left\lfloor \frac{DIV}{64} \right\rfloor \text{ rem} * 64 = \mathbf{A} \qquad (7)$$

Summarize of RF PLL setting

R = 495
N = equation (6)
A = equation (7)
SW = 1
FC = 1 (phase control bit)

8 External interface

The following table describes the interface signals between the radio and digital circuit.

Signal Name	Signal Type	Description
RX DATA	Analog, 200mVp-p nominal	Receive data to ASIC for demodulation
RSSI	Analog, tbd level ….	Receive signal strength indicator, to ADC
AFC CONT	Analog signal, 1.5V ± 1V nominal	AFC control signal from ASIC
+3V?	DC voltage from???	
RX+B CONT	CMOS	Control signal from digital circuit. When HI it turns on the regulated power supply to the Rx RF circuit.
PLL CLK	CMOS, pulled HI on RF side	PLL serial clock from digital circuit
PLL DATA	CMOS, pulled HI on RF side	PLL programmed data serial data from digital circuit
PLL ENB	CMOS, pulled HI on RF side	PLL latch enable from digital circuit
I	Analog, 1Vp-p nominal, 1.5V DC level	GMSK modulated I data from ASIC
Q	Analog, 1Vp-p nominal, 1.5V DC level	GMSK modulated Q data from ASIC
TXPLL +B CONT	CMOS	Control signal from digital circuit. When HI it turns on the regulated power supply to the Tx RF circuit.
TX +B CONT	CMOS	Control signal from digital circuit. When HI it turns on the switch which applies power to the PA and Driver amplifier.
TX PW CONT	Analog	Power level control signal from digital circuit.
3.6V	DC power	Battery power
GND	Ground	Radio circuit zero reference level.

9 Digital to Analog Converters

There are five D-to-A converters used in the PC card for interfacing between the ASIC and RF circuit. Two DACs are used for I and Q signals, one DAC used for TX power control, the last two are used for AFC function. As far as the RF circuit concerns, these DACs belong to the digital portion and they will be powered from digital supply, that why the RF block diagram and the interface table did not show these component.

To save pin out for the ASIC, off -the-shell serial DACs are used. The limitation of space and low power limit the choice of these DACs. So two MAX533ACEE 8-bit Quad DAC from Maxim were chosen. This DAC comes in 16 QSOP package, and operating from 2.7V to 3.6V single supply at a typical 0.7mA. Three DACs from one MAX533 are used for AFC, threshold control and I data. The other MAX533 is used for Q data and for TX power control. These two MAX533 share the same 4.608MHz serial clock, and have separated serial data and separated chip select signals.

7. CDPD Protocol Subsystem (CPS/MCU)

1 Overview

The primary purpose of the CDPD Protocol Subsystem (CPS/MCU) is to be responsible for handling the Forward Channel data that sends from the Mobile Data Base Station (MDBS) to the Mobile-End System (M-ES). It will also responsible for handling the Reverse Channel data that sends from the M-ES to the MDBS. The network interface technique that will be used to communicate between these two systems are structured into an ordered set of the following layers:

- Physical Layer*
- Medium Access Control (MAC) Layer*
- Mobile Data Link Protocol (MDLP) Layer
- Radio Resource Management (RRM) Layer
- Subnetwork Dependent Convergence Protocol (SNDCP) Layer
- Mobile Network Registration Protocol (MNRP) Layer

The above layers are based on the International Organization of Standards (ISO) communications reference model. Each of the above layers is a task within the CDPD Protocol Subsystem (CPS/MCU).

Since the CPS/MCU code is ported from the existing software of the UD1000 product, this document will only discuss the above layers/tasks (with "*" marker) within the CPS/MCU that will be needed to modify to meet the requirements for the PCMCIA product.

2 Physical Layer

The communications between the MDBS and the M-ES occur at the Physical Layer and the MAC layer. The Physical Layer will primarily be responsible for the following functions:

- Accept a sequence of bits from the MAC layer and transforms them into a modulated waveform for transmission to the MDBS.
- Receive a modulated waveform from the MDBS and transform into a sequence of bits to send to the MAC layer.
- Tune to a specific RF Channel.
- Measure the Received Signal Strength Indication (RSSI) of the received signal.
- Set the Power Level of the transmitted signal.

The above functions will be required to handle by the RF, the ASIC Forward Engine, and the ASIC Reverse Engine. However, the Physical task of the CPS/MCU consists of the following drivers which will be used by the RRM Layer task in order to assist the RF and the ASIC engines to accomplish the above functions:

- Program the RF to tune to a particular channel/frequency.
- Monitor the RSSI value.

- Forward the Power Level value to the ASIC for the transmitted signal.

3 MAC Layer

The MAC Layer consists of the following functions:

- Handle the data encapsulation for the Forward Channel and the Reverse Channel.
- Manage the medium access of the Reverse Channel.
- Handle the timing and synchronization of the Forward Channel and the Reverse Channel.

One interrupt line (INT1) will be used by the ASIC engines to notify the CPS/MCU of one of the following events:

1. The REED_SOLOMON signal which will be used by the ASIC Forward Engine to signal the MCU when one of the following conditions occurs:
   - When a forward data block is received and decoded successfully or unsuccessful.
   - When a complete 7-bit of the Decode Status flag is received for the reverse data block that is just transmitted by the ASIC Reverse Engine. (See the ASIC Design Document for further details on the handshake between the Forward Engine and the Reverse Engine).
   - Loss of Sync on the Forward Channel Stream.
2. The START_REC_FWD_BLK signal which will be used by the ASIC Forward Engine to signal the MCU when it starts to receive the first bit of the forward data block (after it finds sync in the forward channel).
3. The TX_RESPONSE signal which will be used by the ASIC Reverse Engine to signal the MCU that it starts to transmission (see section 1.2.2 Reverse Channel Data for further details on this signal).
4. The ENCODED_READY signal which will be used by the ASIC Reverse Engine to signal the MCU that the data that is loaded into the Encoder RAM page is encoded.

All the signals from the CPS/MCU to the ASIC are used through the “Control Registers” mechanism. The format of all the control and status registers are described in details under sections 1.3, 1.4 and 1.5.

.1 Forward Channel Data

The ASIC Forward Engine will be responsible for handling the following functions:

- Receive the raw forward data and handle the timing and the synchronization of the forward channel stream.
- Send a “START_REC_FWD_BLK” signal to the CPS/MCU when receives the first bit of each of the forward data block.
- Perform Reed-Solomon Decoding algorithm on the received forward data blocks.
- Parse the Control Flags (for the Busy/Idle Status Flag and the Decode Status Flag).
- Accept either the “End of Block” (EOB) signal or the “End of Transmission” (EOT) signal from the ASIC Reverse Engine in order to determine when it needs to extract the Decode Status bits from the forward data blocks.

- Send the "REED_SOLOMON" signal to the CPS/MCU when one of the following conditions occurs:
    - After a single forward data block is received and decoded. The Forward Error Correction (FEC) value and Busy/Idle Status flag are expected to be loaded into the necessary control registers.
    - A complete 7-bit Decode Status value is received and loaded to the necessary control register.
    - A loss of signal is detected.
- Accept the "Shutdown" signal from the CPS/MCU.

The MAC task of the CPS/MCU will be responsible for handling the following functions:

- Command the ASIC Forward Engine to start receiving the forward data and detecting the synchronization in the forward channel stream.
- Accept the "REED_SOLOMON" signal from the ASIC Forward Engine.
- Evaluate the FEC value for each received forward data block.
- Map data blocks into frames format if the FEC value is in between 0 and 7.
- Forward the frames to the upper protocol stack layer.
- Evaluate the Channel Color Code.
- Forward the Channel Color Code, the FEC value, the Sync Loss information that are received from the ASIC to the upper protocol stack layer.
- Enable and accept the "START_REC_FWD_BLK" interrupt line when the CPS/MCU needs to resync the system clock.
- Send a "Shutdown" signal to the ASIC Forward Engine when the CPS/MCU enters the Sleep Mode.

.2 Reverse Channel Data

The communications between the ASIC Reverse Engine and the CPS/MCU consists as follows:

- Two Ping-Pong RAM pages will be allocated on the ASIC component which will be used by the CPS/MCU to send the reverse data blocks to the ASIC Reverse Engine.
- Another Encoder RAM page will be allocated on the ASIC component which will be used to load the reverse data blocks so that the ASIC Encoder can process these data blocks.
- Several control registers will be allocated for the CPS/MCU to use either to signal the ASIC Reverse Engine to perform a particular function (such as sending the reverse data block) or to pass the necessary MAC configuration parameters.
- Several status registers will be allocated for the ASIC Reverse Engine to set the necessary status information about the reverse data blocks that are already transmitted.

The ASIC Reverse Engine will be responsible for handling the following functions:

- Perform the M-ES state transition for the Reverse Channel Access that is specified in the figure 402-17 of the CDPD System Specification under the direction of the CPS/MCU. In other words, the CPS/MCU will be responsible for providing the necessary configuration

parameters and indications to the ASIC Reverse Engine so that it can determine the state transition.

- Accept the "TX Send" signal from the CPS/MCU. The following MAC Configuration parameters are expected to load to the necessary control registers before the "TX Send" signal is sent to the ASIC Reverse Engine:
    - Page Number
    - Last Block Indication
    - Number Reverse Blocks that are stored in the selected RAM page
    - Max Entrance Delay
    - Max TX Attempts
    - Min Idle Time
    - Min Count
    - Max Count
- Send a "TX_RESPONSE" signal to notify the CPS/MCU when one of the following conditions occurs:
    - After the first bit of the selected page is transmitted to the MDBS.
    - When a transmission is aborted due to a fatal error (such as detects an invalid Busy/Idle flag or reaches the maximum of the transmission attempts). The CPS/MCU expects the ASIC Reverse Engine to load the address of the last data byte that is sent to the MDBS to the necessary status register when the above signal is generated.
- Send either the "End of Block" (EOB) signal after each block is transmitted or the "End of Transmission" (EOT) signal after the last block is transmitted to the ASIC Forward Engine.
- Terminate the data transmission when a "TX Abort" signal is received from the CPS/MCU. The address of the last transmitted data byte is expected to be loaded into one of the status registers.

The MAC task of the CPS/MCU will be responsible for handling the following functions:

- Accept up to 32 data frames from the upper protocol stack layer.
- Map the received frames into data blocks. This includes handling the zero insertion, the flag delimited, the block encoder, the Pseudo-random Number coverage, and the continuity indicator for all the reverse data blocks.
- Load the MAC configuration parameters that are listed above to the necessary control registers.
- Move the reverse data blocks into the necessary RAM page.
- Send a "TX_SEND" signal to Reverse Engine when there is at least one block that needs to be transmitted..
- Accept and validate the "TX RESPONSE" signal from the ASIC Reverse Engine and perform one of the following steps:

- If this signal indicates that the first data byte is transmitted to the MDBS and if there are more data blocks to be sent, then the CPS/MCU will start to load these blocks into the next available RAM page.

- If this signal indicates that the transmission is aborted due to a fatal error, then the MAC task will notify the MDLP Layer and the RRM Layer tasks to shutdown the current channel. The remain reverse data blocks will be flushed by the CPS/MCU.

- Send a "TX Abort" signal to the ASIC Reverse Engine to stop the transmission when one of the following conditions occurs:

  - Detect a Loss of Signal in the forward channel stream from the ASIC Forward Engine.

  - Receive a failed Decode Status from the ASIC Forward Engine.

- Support the ASIC Reverse Engine in handling the Reverse Channel Access procedure that is specified under section 5.3.3 of the CDPD specification document as follows:
  - Signal to perform the Backoff state when a failed decode status is received from the Forward Engine.
  - Signal to enter the Pre-Idle State when the decode status of the last block in the transmitted burst is received from the ASIC Forward Engine.