

PROCESSING GAIN TEST

CHANNEL18(2442.240MHz)-Base station output to handset input

LOSSES(dB)

Jammer Freq. (MHz)	Transmitter Outputs (dBm)	Signal Level (dBm)	CW Level (dBm)	Mj J/S ratio (dB)	Processing Gain (dB)
2441.240	14.0	-36.0	-33.2	2.8	15.8
2441.290	14.0	-36.0	-33.6	2.4	15.4
2441.340	14.0	-36.0	-34.0	2.0	15.0
2441.390	14.0	-36.0	-34.6	1.4	14.4
2441.440	14.0	-36.0	-36.0	0.0	13.0
2441.490	14.0	-36.0	-36.9	-0.9	12.1
2441.540	14.0	-36.0	-36.2	-0.2	12.8
2441.590	14.0	-36.0	-36.9	-0.9	12.1
2441.640	14.0	-36.0	-36.9	-0.9	12.1
2441.690	14.0	-36.0	-36.4	-0.4	12.6
2441.740	14.0	-36.0	-35.3	0.7	13.7
2441.790	14.0	-36.0	-35.6	0.4	13.4
2441.840	14.0	-36.0	-36.4	-0.4	12.6
2441.890	14.0	-36.0	-36.4	-0.4	12.6
2441.940	14.0	-36.0	-36.6	-0.6	12.4
2441.990	14.0	-36.0	-36.8	-0.8	12.2
2442.040	14.0	-36.0	-36.9	-0.9	12.1
2442.090	14.0	-36.0	-37.0	-1.0	12.0
2442.140	14.0	-36.0	-37.0	-1.0	12.0
2442.190	14.0	-36.0	-36.7	-0.7	12.3
2442.240	14.0	-36.0	-37.4	-1.4	11.6
2442.290	14.0	-36.0	-37.2	-1.2	11.8
2442.340	14.0	-36.0	-37.3	-1.3	11.7
2442.390	14.0	-36.0	-37.5	-1.5	11.5
2442.440	14.0	-36.0	-37.2	-1.2	11.8
2442.490	14.0	-36.0	-36.4	-0.4	12.6
2442.540	14.0	-36.0	-36.3	-0.3	12.7
2442.590	14.0	-36.0	-36.4	-0.4	12.6
2442.640	14.0	-36.0	-35.3	0.7	13.7
2442.690	14.0	-36.0	-34.9	1.1	14.1
2442.740	14.0	-36.0	-34.4	1.6	14.6
2442.790	14.0	-36.0	-36.9	-0.9	12.1
2442.840	14.0	-36.0	-37.1	-1.1	11.9
2442.890	14.0	-36.0	-35.8	0.2	13.2
2442.940	14.0	-36.0	-36.2	-0.2	12.8
2442.990	14.0	-36.0	-35.8	0.2	13.2
2443.040	14.0	-36.0	-35.3	0.7	13.7
2443.090	14.0	-36.0	-34.4	1.6	14.6
2443.140	14.0	-36.0	-33.8	2.2	15.2
2443.190	14.0	-36.0	-33.3	2.7	15.7
2443.240	14.0	-36.0	-32.9	3.1	16.1

Attenuation 50
System Loss 2
S/N ratio 11

Mj J/S ratio =
CW Noise-Sig.Level

ProcessingGain =
Mj J/S ratio + Sytem Loss
+ S/N ratio



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2443.240	14.0	-36.0	-33.9	2.1	15.1

LOSSES(dB)

Attenuation 50
System Loss 2
S/N ratio 11

Mj J/S ratio =
CW Noise-Sig.Level

ProcessingGain =
Mj J/S ratio + Sytem Loss
+ S/N ratio



SD Test Specification for Processing Gain

The Processing Gain is measured with using the CW jamming margin method. Figure 1 shows the test configuration. The test consists of stepping a signal generator in 50 kHz increments across the passband of the system (up to 1MHz away from the center frequency). At each point, the generator level required to be produced the recommended Bit Error Rate (BER) (Set at BER=1.0E-3) is recorded. This level is the jamming level. The output power of the transmitter unit is measured at the same point. The Jammer to Signal (J/S) ratio is then calculated. Discard the worst 20% of the J/S data point. The lowest remaining J/S ratio is used to calculate the processing gain. The maximum implementation loss a system can claim in calculating processing gain is 2dB. The equation to calculate the processing gain (Gp) is as follows:

$$G_p = (S/N)_o + M_j + L_{sys}$$

Where $(S/N)_o$ = signal to noise ratio required for a FSK system with BER of 1.0E-3 = 11dB,

M_j = jamming margin (J/S) in dB,

L_{sys} = system implementation loss = 2dB.



[TEST PROCEDURE]

1. B/S output to H/S input

- (1)The B/S is connected by its RF test connector to the fixed attenuator which is 50dB. The output of the fixed attenuator is combined with the output of the signal generator through a combiner. The output of the combiner is connected by the H/S RF test connector. The H/S is connected by the BB-ASIC(UC2575)'s test pins to the BER counter (RX data is pin32 and RX clock is pin41).
- (2)TONE/PULSE SW set to PULSE. The B/S is powered by the adapter while pushing the page-key. The page-key shall be held at least for 3 seconds. Then the page-key is released and pushed shortly (within 500 mSec) 10 times. TONE/PULSE SW is set to TONE. Then the PAGE-KEY is pushed shortly (within 500 mSec) once. The H/S is powered by the battery while pushing the *-KEY and #-Key. Those keys are held at least for 2 seconds. Then those keys are released and the 'flash'-key is pushed once. And then "channel-key" is pushed once.
- (3)BER counter is JRC NJZ-940 (Continuous mode, PN15, and the receive clock uses an external clock with its leading edge.).
- (4)The signal generator is stepped in 50kHz increments. The required BER is 1.0e-3. When this error rate is achieved (displayed on the BER counter), the reading of signal generator is taken. This reading is then subtracted from the signal level of the B/S (while adding in the combiner loss and signal generator calibration factor) to obtain the J/S ratio. The J/S ratio is then combined with the system loss (2dB) and signal to noise ratio (11dB) of the unit to obtain the processing gain.

2. H/S output to B/S input

- (1)The H/S is connected by its RF test connector to the fixed attenuator which is 50dB. The output of the fixed attenuator is combined with the output of the signal generator through a combiner. The output of the combiner is connected by the B/S RF test connector. The B/S is connected by the BB-ASIC(UC2575)'s test pins to the BER counter (RX data is pin32 and RX clock is pin41).
- (2)TONE/PULSE SW set to PULSE. The B/S is powered by the adapter while pushing the PAGE-KEY. The PAGE-KEY shall be held at least for 3 seconds. Then the page-key is released and pushed shortly (within 500 mSec) 10 times. TONE/PULSE SW is set to TONE. Then the PAGE-KEY is pushed shortly (within 500 mSec) once. The H/S is powered by the battery while pushing the *-KEY and #-Key. Those keys are held at least for 2 seconds. Then those keys are released and the 'FLASH'-KEY is pushed once. And then "channel-key" is pushed once.
- (3)BER counter is JRC NJZ-940 (Continuous mode, PN15, and the receive clock uses an external clock with its leading edge.).
- (4)The signal generator is stepped in 50kHz increments. The required BER is 1.0e-3. When this error rate is achieved (displayed on the BER counter), the reading of signal generator is taken. This reading is then subtracted from the signal level of the H/S (while adding in the combiner loss and signal generator calibration factor) to obtain the J/S ratio. The J/S ratio is then combined with the system loss (2dB) and signal to noise ratio (11dB) of the unit to obtain the processing gain.



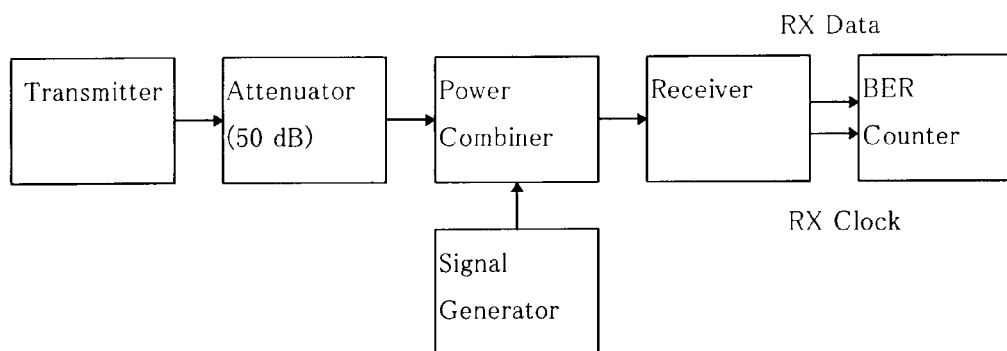


Fig. 5 The test configuration.

Processing Gain Test Equipment

	MANU-FACTURER	EQUIPMEN T TYPE	SERIAL NUMBER	CAL. DATE	CAL. DUE DATE
Variable Attenuator	Hewlett Packard	HP8496B	3308A71267	Aug. 11, 2000	Aug. 31, 2001
Variable Attenuator	Hewlett Packard	HP8494B	3308A37106	Aug. 11, 2000	Aug. 31, 2001
BER Counter	JRC	NJZ-940	ED24250	Nov. 08, 1999	JAN. 31, 2001
Signal Generator	Hewlett Packard	E4432B	US38441753	Aug. 24, 2000	Aug. 31, 2001
Combiner	Mini-Circuit	15542	942705	N/A	N/A



Other information

1. Actual frequencies for each channel:

CH	Frequency	CH	Frequency	CH	Frequency	CH	Frequency
1	2407.424MHz	11	2427.904MHz	21	2448.384MHz	31	2468.864MHz
2	2409.472MHz	12	2429.952MHz	22	2450.432MHz	32	2470.912MHz
3	2411.520MHz	13	2432.000MHz	23	2452.480MHz	33	2472.960MHz
4	2413.568MHz	14	2434.048MHz	24	2454.528MHz	34	2475.008MHz
5	2415.616MHz	15	2436.096MHz	25	2456.576MHz	35	2477.056MHz
6	2417.664MHz	16	2438.144MHz	26	2458.624MHz		
7	2419.712MHz	17	2440.192MHz	27	2460.672MHz		
8	2421.760MHz	18	2442.240MHz	28	2462.720MHz		
9	2423.808MHz	19	2444.288MHz	29	2464.768MHz		
10	2425.856MHz	20	2446.336MHz	30	2466.816MHz		

2. Chipping rate: 1.366 M cps

3. Antenna Gain for both the Base unit and Handset:

Gain respect to dipole

Base unit: + 3.16 dB

Handset : + 0.36 dB

Gain respect to isotropic

Base unit: + 5.3 dBi (=+3.16+2.14)

Handset : + 2.5 dBi (=+0.36+2.14)

Note that antenna gain measurement were conducted based on substitution method using with double ridged antenna.

4. Processing Gain: Please see attached documents.

