DESCRIPTION OF COMPONENTS

RX PLL : Z1, TX PLL : Z4 (X58-3120-10)

Ref. No.	Parts No.	Descriptions
IC1	MB504F	Prescaler
IC2	JLC1075F	PLL system
Q1	2SC3829TS	RF amplifier
Q2 ~ 5	DTC114EK	Inverter
D1	02CZ3.0(Z)	Level shifter

RX VCO : Z2 (X58-3150-10)

Ref. No.	Parts No.	Descriptions
Q1	2SK508NV (K52)	Oscillator
Q2, 3	2SC3356	Buffer amplifier
Q4	2SC3099	Buffer amplifier
D1	1SV166	Tuning

TX VCO : Z5 (X58-3460-10)

Ref. No.	Parts No.	Descriptions
Q1	2SK508NV (K52)	Oscillator
Q2	2SC3356	Buffer amplifier
Q3, 4	2SC3356	RF amplifier
D1	1SV166	Tuning
D2	1SV164	Modulator

MIC AMP : Z7 (X59-3210-10)

Ref. no.	Parts no.	Descriptions
IC1	NJM4560M	Mic amplifier/Limitter
IC2	NJM4558M	Limitter
IC3	NJM4558M	Active filter
Q1	2SC3326(A)	Muting switch

IF : Z8 (X59-3220-10)

Ref. No.	Parts No.	Descriptions
IC1	MC3361	IF system
Q1	2SC2712(Y)	Noise amplifier
D1	DA204K	Noise detector

BPF/VCA : Z9 (X59-3230-10)

Ref. No.	Parts No.	Descriptions
IC1	NJM4558M	Audio amplifier
IC2	NJM4558M	Active filter
IC3	M5222FP	Electronic attenuator
IC4	NJM4558M	Active filter

DESCRIPTION OF COMPONENTS

AVR UNIT (X43-3040-10)

Ref. No.	Parts No.	Descriptions
Q1 ~ 3	2SC2712(Y)	DC amplifier
Q4	2SB968(Q)	DC amplifier
Q5, 6	2N5885	DC amplifier
D1	1B2C1	Rectifier
D3	S25VB20	Rectifier
D4	1SS181	Temperature compensate
D5	RD7.5EB2	Voltage reference
D6	1SS181	Temperature compensate

FINAL UNIT (X45-3250-10)

Ref. No.	Parts No.	Descriptions
IC1	M57729H-01-P	TX power amplifier
Q1	2SC3357	RF amplifier
Q2	2SC2954	RF amplifier
Q3	2SB946(Q)	DC amplifier
Q4	2SC2712(Y)	DC amplifier
Q5, 6	2SC3326(A)	DC amplifier
D1	1SV172	RF switch
D2	1SS226	Voltage reference
D3, 4	1SS101	RF detect
D5	DSA3A1	Reverse polarity protection

SIGNALING UNIT (X52-3140-10)

Ref. No.	Parts No.	Description
IC1	MC78L05M	Voltage regulator 5V
IC2	M51943BML	Reset system
IC3	BA4558F	Data recovery, active filter
IC4	BA4558F	Active filter
IC5	BA4558F	Data recovery
IC6, 7	BA4558F	Active filter
IC8	27C256QJESB	EPROM
IC9	TC74HC573AF	Data latch
IC10	BR93LC46	EEPROM
IC11	μPD78310AGF	Microprocessor
Q1	DTC144EK	Level translator
Q2	DTC144EK	Inverter
Q3 ~ 7	DTC144EK	DC switch
Q8	DTA114EK	DC switch
Q9	2SC3326(A)	Audio amplifier
Q10	2SJ106(GR)	Audio amplifier
D1, 2	1SS184	Current steering
D3	HSM88AS	Voltage clamp
D4 ~ 6	1SS184	Current steering
D7	B30-0838-05	LED (Red)

DISPLAY UNIT (X54-3070-11)

Ref. No.	Parts No.	Descriptions
IC1	μPD75104GF-J99	Microprocessor
IC2	BR93LC46	EEPROM
IC3	M51943BML	Precision reference
IC4	AN78N05	Voltage regulator 5V
IC5	μPC4558C	Audio amplifier
IC6	μPC4558C	Active filter
Q1, 2	DTC114EK	DC switch
Q3	2SA1162(Y)	Digital switch
Q4	DTC114EK	DC switch
Q6	2SC3326(A)	AF switch
Q7, 8	DTC114EK	DC switch
D1	B30-0855-05	LED (Red)
D2	B30-0856-05	LED (Green)
D3	B30-0855-05	LED (Red)
D4 ~ 6	1SS184	Voltage clamp
D7, 8	1SS181	Current steering
D9	1S1555	Current steering
D10, 11	1SS181	Current steering
D12	1SS184	Current steering
D13	1SS181	Current steering
D16	B30-0857-05	LED (Yellow)
D17	B30-0856-05	LED (Green)
D18	B30-0857-05	LED (Yellow)
D21	1SS272	Current steering

TX-RX UNIT (X57-3270-10)

Ref. No.	Parts No.	Descriptions
IC1	μPC1242H	AF power amplifier
IC2	MB3756	Voltage regulator
IC3	NJM4558D	AF amplifier
IC4	AN78N08	Voltage regulator
Q1, 2	2SC2712(Y)	Voltage shift
Q3	2SC4093(R27)	RF amplifier
Q4, 5	2SK125	IF amplifier
Q6	2SK302(GR)	IF amplifier
Q7	2SC2712(Y)	Level translator
Q8	DTC114EK	Inverter
Q9, 10	2SC3326(A)	Audio mute switch
Q11	DTC114EK	DC switch
Q12, 13	DTC114EK	Inverter
D1	1SV128	TX VCO output mute
D2	1SV172	TX VCO output mute
D3	1SS226	Voltage clamp
D4	ND487C1T	Double balanced modulator
D5 ~ 9, 11	1SS184	Current steering

ADJUSTMENT

Test equipment required for alignment

Test Equipment	Major Specifications	
1. Standard Signal Generator (SSG)	Frequency range	40 0~512MHz
	Modulation	Frequency modulation and external modulation.
	Output	0.1μV to greater than 1mV
2. Power meter	Input impedance	50 ohms
	Operation frequency	400 to 512MHz or more.
	Measurement capability	Vicinity of 50W.
3. Deviation meter	Frequency range	400~512MHz
4. Digital Volt Meter	Measuring range	1~10V DC.
	Accuracy	High input impedance for minimum circuit loading.
5. Oscilloscope		DC through 30MHz.
6. High sensitivity frequency counter	Frequency range	10Hz to 600MHz.
	Frequency stability	0.2 ppm or less.
7. Ammeter		15A.
. AF Volt Meter (AFVTVM)	Frequency range	50Hz to 10kHz.
	Voltage range	3mV to 3V.
9. Audio Generator (AG)	Frequency range	50Hz to 5kHz or more.
	Output	0 and 1V.
10. Distortion meter	Capability	3% or less at 1kHz.
	Input level	50mV to 10Vrms.
11. Voltmeter	Measuring range	10~1.5V DC or less.
	Input impedance	50 kohms/V or greater.
12. 4 ohm dummy load		Approx. 4 ohm, 3W.

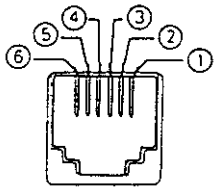
The set has been adjusted for the frequencies shown in the following table. When required, re-adjust them following the adjustment procedure to obtain the frequencies you want in actual operation.

		RX freq' (MHz)	TX freq' (MHz)
TKR-820	K	469.900	464.900
TKR-820	K2	489.900	484.900
TKR-820	K3	511.900	506.900
TKR-820	K4	429.900	424.900

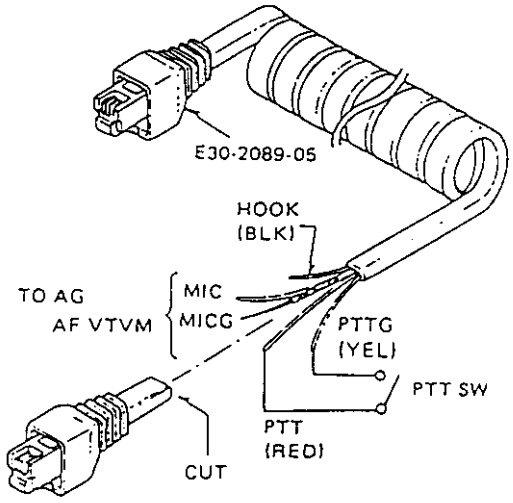
SIGNALING

CH	RX		TX	
	QT (Hz)	DQT	QT (Hz)	DQT
1	67		77	
2	192.8		179.9	
3		023		754
4	88.5		167.9	
5	100			351

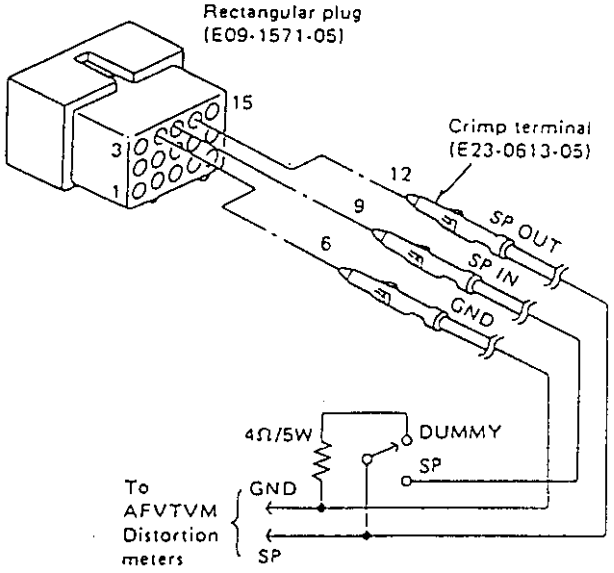
MIC connector front view



- The following test cables are recommended.



Test cable for Microphone input

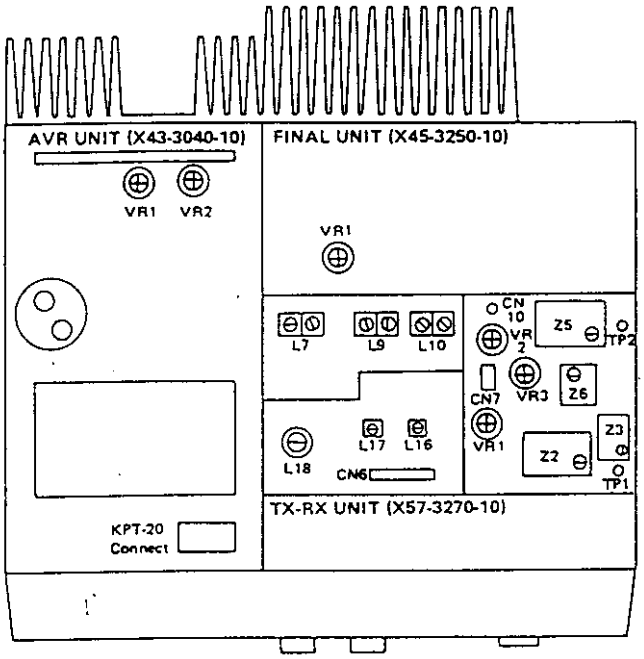


Test cable for Speaker output

ADJUSTMENT

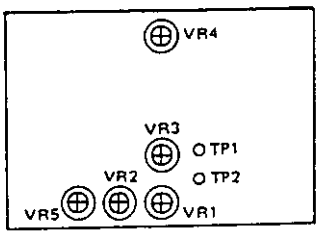
Adjustment location

Top view

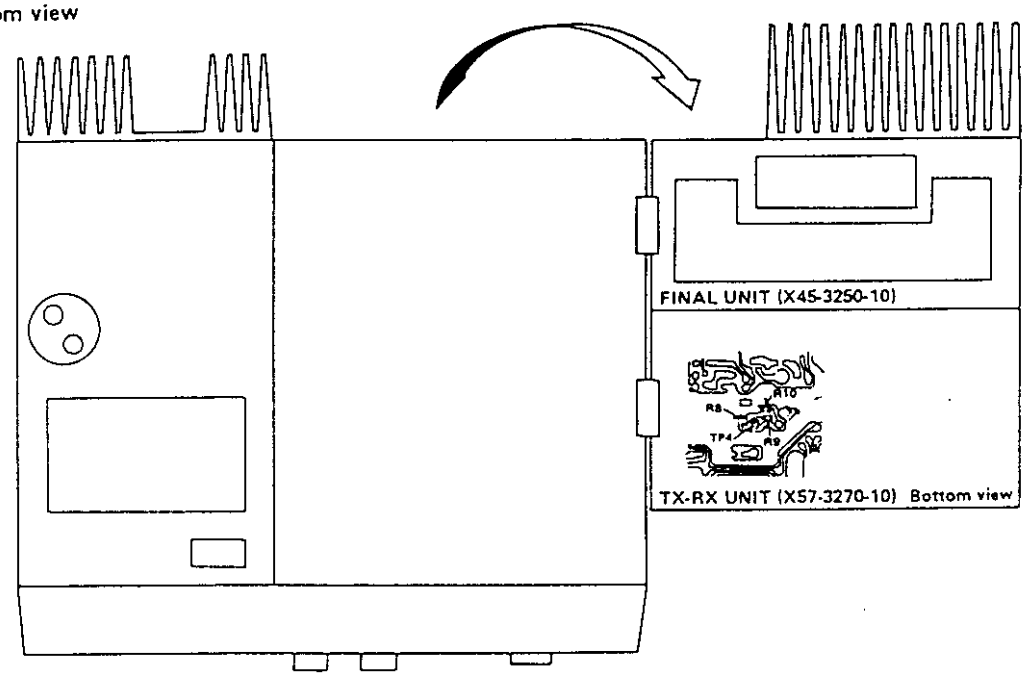


Adjustment points

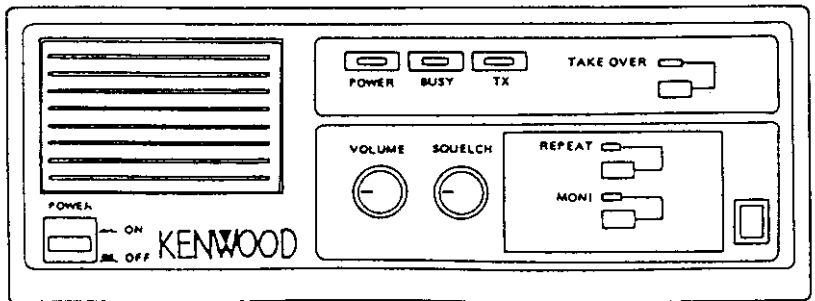
SIGNALING UNIT (X52-3140-10)



Bottom view

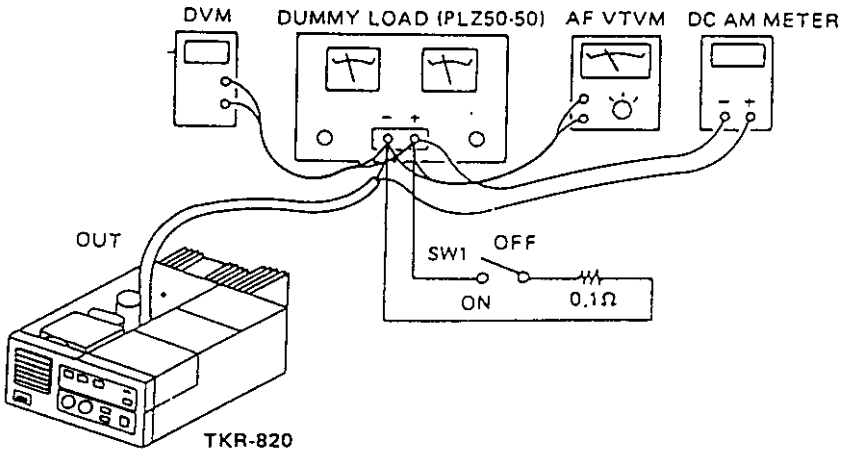
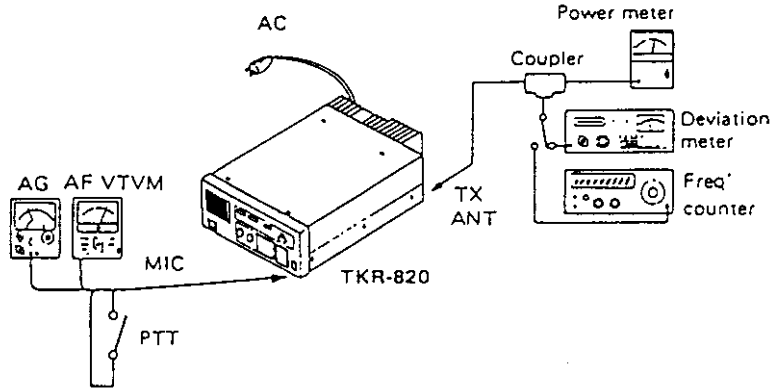


Front panel view

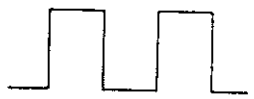


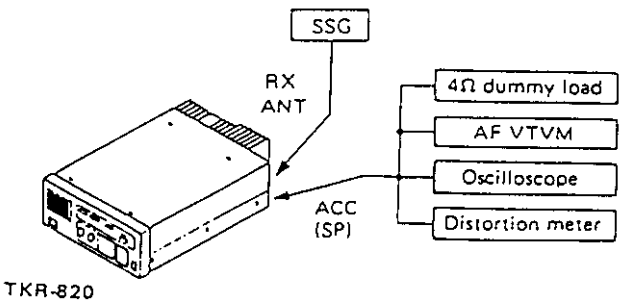
ADJUSTMENT

Alignment

Item	Condition	Measurement			Adjustment			Specifications/Remarks
		Test-equipment	Unit	Terminal	Unit	Part	Method	
Setting	1) AC voltage for destination : 120V 2) Connect to the DC output (OUT terminal) and GND of the AVR unit. (+)							
Test equipment set-up	1) Function : 0.1Ω resistor Meter : 60A, 60V DC : ON Power : ON SW1 : OFF							
Voltage setting	1) Power switch : ON	DVM		Output	AVR	VR1	Adjust the load for 10A.	13.6V ± 0.4V (Verify power indicator lights.)
	2) Vary the load for 2A — 10A draw. (Set to 10A after check.)	DVM AF VTVM						13.6V ± 0.7V DC Less than 30mV AC.
	3) Power switch : OFF							
Protection	1) SW1 : ON VR2 : MAX CW. Power switch : ON	DVM		Output	AVR	VR2	0.2V	0.2V ± 0.1V.
	2) SW1 : OFF						Check	13.6V ± 0.4V
Setting	1) Write in freq' designed with EEP ROM writer. (For freq' writing, set the power of TKR-820 to ON.) 2) Connect the power cable to the rear panel. 3) Final unit VR1 : MAX CCW. 4) TX-RX unit VR1 : MAX CCW. VR3 : MAX CCW. 5) Power SW : ON							
PLL lock voltage		DVM	TX-RX	TP1	TX-RX	Z2	4.0V ADJ.	±0.1V
PLL lock voltage			TX-RX	TP2	TX-RX	Z5	4.0V ADJ.	±0.1V

ADJUSTMENT

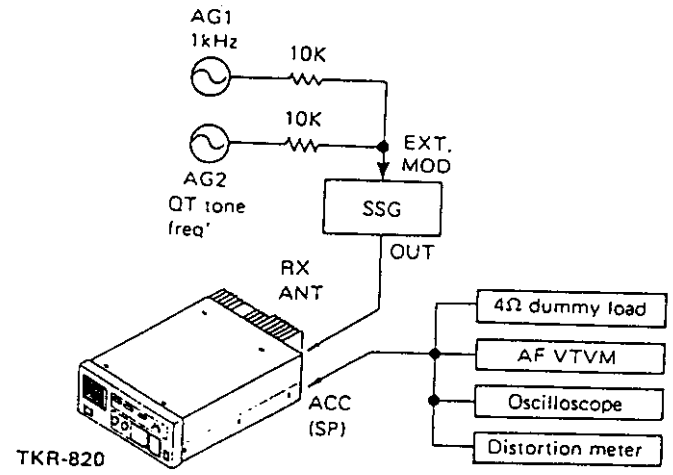
Item	Condition	Measurement			Adjustment			Specifications/Remarks
		Test-equipment	Unit	Terminal	Unit	Parts	Method	
8. TCXO Freq' ADJ.	1) PTT : OFF (RX) Note : TCXO is adjusted precisely at 25°C. If it is readjusted, the frequency stability is changed. Do not touch it normally.	Power meter FREQ' counter	TX-RX	TP4 (Foil side)	TX-RX	Z3	f – 21.4MHz ADJ.	±100Hz
9. Power ADJ. (APC)	1) PTT : ON	Power meter Ammeter	Rear panel	TX ANT	Final	VR1	MAX CW.	26W or more.
							MIN	2W or less.
							26W ADJ.	±1W
10. Transmit Freq' ADJ.	1) PTT : ON	Power meter FREQ' counter	Rear panel	TX ANT	TX-RX	Z6	FREQ' ADJ. of TX.	±100Hz
11. Tone deviation ADJ.	1) QT tone freq' being written. Deviation meter filter : LPF : 3kHz, HPF : OFF, De-emphasis : OFF PTT : ON	Power meter Deviation meter	Rear panel	TX ANT	Signal-ing	VR4	±0.75kHz	±100Hz
12. Maximum deviation ADJ.	1) Connect AG to the MIC terminal. AG : 1kHz/50mV Deviation meter filter : LPF : 20kHz, HPF : 50Hz, De-enphasis : 750μsec. TX-RX unit VR1 : MAX CW. PTT : ON	Power meter Deviation meter	Rear panel	TX ANT	TX-RX	VR2	±2.1KHz ADJ. (±2.4kHz ADJ. In use of signaling.) Adjust one more than the other by switching between –P and +P.	±100Hz
3. MIC sensitivity ADJ.	1) AG : 1kHz/5mV PTT : ON	Power meter Deviation meter	Rear panel	TX ANT	TX-RX	VR1	±1.5KHz ADJ. (±1.95KHz ADJ. In use of signaling.)	±100Hz
4. DQT waveform correction	1) Connect AG to the TX-RX (TP3) and enter a square wave of 100Hz, 2Vp-p. Deviation meter filter : OFF PTT : ON	Power meter Deviation meter Oscillo-scope			TX-RX	VR3	Make the demodu-lation waveform neat.	
5. RX sensitivity ADJ.		AF VTVM 4Ω dummy load	Rear panel	EXT.SP	Front panel	AF VOL.	0.78V/4Ω (Noise)	



ADJUSTMENT

Item	Condition	Measurement			Adjustment			Specifications/Remarks
		Test-equipment	Unit	Terminal	Unit	Parts	Method	
	1) SSG output : 500μV/−53dBm MOD : OFF	SSG AF VTVM Distortion meter 4Ω dummy load	Rear panel	EXT.SP	TX-RX	L7 L9 L10	Reduce noise level using L7, L9 and L10. Decrease the SSG output so that noise level is always 20 to 30dB lower than 0.45V Repeat 3 to 4 times.	
	2) SSG output : 500μV/−53dBm MOD : 1kHz/3kHz DEV.					L18	Adjust for maximum AF output.	
	3) SSG output : 0.32μV/−117dBm					L16 L17	Adjust for maximum SINAD.	
					Front panel	AF VOL.	0.45V/4Ω ADJ.	
	4) SSG output : 500μV/−53dBm						Check	SINAD 12dB or more.
					Front Panel	AF VOL.	4.0V/4Ω ADJ.	
quelch	1) SSG output : OFF Rotate SQL VR to a point at which noise disappears.	SSG AF VTVM 4Ω dummy load Oscillo-scope	Rear panel	EXT.SP			Check	S/N 45dB or more. Distortion : 5% or less.
	2) SSG output : 0.2μV/−121dBm							SQL index angle 8:00 ~ 10:00
eset uelch DJ.	1) Signaling unit VR1 to VR5 : MAX CCW. SSG output : OFF	SSG			Signal-ing			Squelch should open.
	2) SSG output : 0.2μV/−121dBm					VR1	MAX CW.	D7 : LED should light.
							Rotate VR1 CCW. to a point at which D7 lights.	D7 : LED should go out.
ngup et ADJ.	1) SSG output : 1.58μV/−103dBm The set time can be continuously varied by VR2. 0 ~ 5V → 0 ~ 5sec.	DVM	Signal-ing	TP2	Signal-ing	VR2	1.0V	±0.1V
	2) SSG output : 501μV/−53dBm REPEAT SW : ON	Power meter SSG	Rear panel	TX ANT RX ANT			Check	TX LED should light. REPEAT LED should light.
	3) SSG output : OFF							TX LED should go out about 1 sec. later after turning SSG OFF.
T	1) The set time can be continuously varied by VR3. 0 ~ 0.3V : OFF ~ 0.5V : 30sec. ~ 5V : ~ 5min.	DVM	Signal-ing	TP1	Signal-ing	VR3	Set it to the target time.	
ter ion	1) SSG output : 501μV/−53dBm	Power meter SSG Deviation meter	Rear panel	EXT.SP	Signal-ing	VR5	±1.5KHz	±100Hz

ADJUSTMENT

Item	Condition	Measurement			Adjustment			Specifications/Remarks
		Test-equipment	Unit	Terminal	Unit	Parts	Method	
21. Signaling squelch	1) SSG output : Turn the SSG output so that the SINAD sensitivity becomes 10dB. 2) SSG MOD SW : EXT. MOD AG1 FREQ' : 1kHz AG2 FREQ' : QT tone freq'. 3) AG1 : Power switch OFF. AG2 output : Adjust the output level of AG2 so that SSG deviation becomes 0.75kHz. 4) AG1 : Power switch ON. AG1 output : Adjust the output level of AG1 so that the SSG deviation becomes 3.75kHz. (i.e., QT tone frequency/ 0.75kHz deviation, +1kHz/3kHz deviation) MONITOR SW : OFF			Rear panel	EXT.SP	Signal-ing		Check	Open.
22. TAKE-OVER					Front panel	TAKE-OVER switch	Check	The TAKEOVER LED must light on.

TKR-820

CIRCUIT DESCRIPTION

Transmitter Circuit

The signal generated at the transmitter frequency synthesizer is amplified by RF amplifier transistors (Q1 and Q2) and amplifier module (IC1) to a level of 25W in the power amplifier unit. The signal is then routed to the antenna connector after going through a harmonics filter.

The transmitter output is detected by D3, 4 and is converted to a DC form. The DC signal thus detected is level adjusted by APC control (VR1) and is applied to the base of Q6. The base current of Q3 is varied according to the difference from the comparison voltage at Q5, 6 so that the collector voltages of Q2 and the IC1 first stage are controlled to maintain the transmitter output level constant.

In the event an abnormal temperature rise occurs, the temperature is sensed by a thermistor (TH1) and reduces the output power to a safe level.

The harmonics filter is of a fifth order Butterworth type lowpass filter having a minimum attenuation of more than 55dB at the second harmonics frequency with a passband insertion loss of less than 0.5dB. With a characteristics of the transmitter final power amplifier module, which has more than 30dB of attenuation for the frequency at the second harmonics or higher, total attenuation of harmonics is more than 70dB.

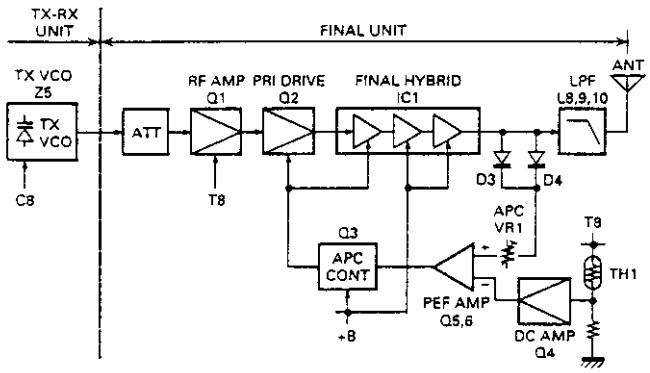


Fig. 1 Transmitter block diagram

Receiver Circuit

An incoming RF signal from the antenna is fed into a bandpass filter (L7). Then eliminated RF signal pass a protector (D3).

The signal is then amplified by an RF amplifier (Q3) and filtered again by bandpass filters (L9 and L10). After amplification and filtering, the signal is applied to a double balanced modulator (DBM, D4) for mixing with the first local signal generated at the Rx frequency synthesizer.

The heterodyning action of the first mixer produces a 21.4MHz first intermediate frequency (1st IF), which is applied to a 6-pole monolithic crystal filter (MCF, XF1) after being amplified by a buffer amplifier (Q4 and Q5 connected in parallel). The signal out of the MCF is further amplified by a 1st IF amplifier (Q6) and sent to the IF unit (Z8).

The signal applied to Z8 is mixed with a 20.945MHz signal at IC1 in Z8, which produces a 455kHz 2nd IF signal. The signal obtained at the 2nd mixer is filtered by a 455kHz ceramic filter (CF1) and amplified by limiting amplifier stages in IC1. The recovered audio signal from the incoming signal is also obtained at IC1 by a quadrature type FM detector. This recovered audio signal is then sent to the audio amplifier circuit and to the noise actuated squelch circuit.

In the receiver audio amplifier section, the recovered audio signal from Z8 is first applied to a bandpass filter/voltage controlled amplifier (BPF/VCA, Z9) unit. At this BPF/VCA unit, the signal is amplified and sent to pin 9 of CN6 as the DET signal. The signal is returned to Z9 by way of the Signaling unit. IC1 forms a lowpass filter and a highpass filter, and IC2 forms a bandpass filter and lowpass filter in Z9. The frequency components below 300Hz and above 3000Hz are attenuated in the above filter circuits.

The filtered audio signal is then applied to an electronic volume control (IC3), where the audio signal level is controlled by a DC voltage sent from the front panel volume control. The signal is then de-emphasized and sent to the audio power amplifier circuit (IC1) after going through squelch switches (Q9 and Q10).

The alert signal is also applied to IC1, when a specific signaling board, which requires an audible alert through the speaker, is installed. The signal, which is amplified by IC1, drives either the internal speaker or the optional external speaker and this selection is done through the accessory connector located on the Final unit.

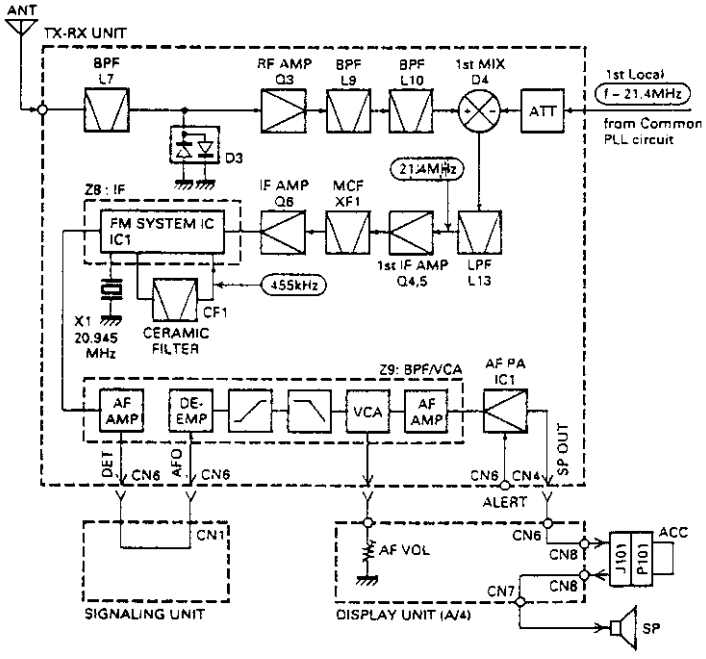


Fig. 2 Receiver block diagram

CIRCUIT DESCRIPTION

Squelch Circuit

The high frequency component of the recovered audio signal is fed to a noise amplifier within IC1 of Z8 and it is further amplified by an external noise amplifier (Q1). The signal is then detected by a noise detector (D1) and applied to the squelch switch in IC1. This detected noise is also routed to the squelch control (VR3) through the Display unit (C/4) for adjusting the noise squelch sensitivity.

The busy information is sent from the above IC1 in the Display unit in serial format to turn on or off the busy LED. The squelch switch output and the audio control (AC) signal from the signaling board are combined at D8 and applied to squelch switch transistors Q9 and Q10 along with the inverted signal of transmit/receive control signal. The squelch switch controls the input signal to the audio amplifier to mute or unmute the receive audio.

While the busy LED is being controlled only by the noise squelch circuit, the actual audio signal is controlled by the following signals and in order to unmute the audio, each signal must be in the condition as specified.

SQL signal = Low
R8 line = High
T/R signal = High
AC signal = Low

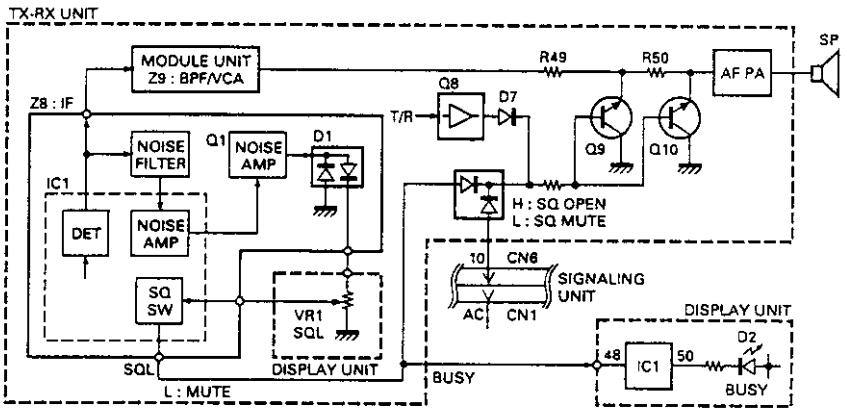


Fig. 3 Squelch circuit

RX Frequency Synthesizer

The RX frequency synthesizer consists of three major circuits. They are the temperature compensated crystal oscillator (TCXO, Z3), RX voltage controlled oscillator (RX VCO, Z2) and RX phase locked loop unit (RX PLL, Z1).

The TCXO is operating at 12.8MHz and its frequency stability is maintained within ±2.5ppm from −30°C to +60°C. This output signal is fed to the frequency synthesizer IC (IC2) in Z1. At IC2, this signal is divided by 1024 to become a 12.5kHz reference signal.

The output from the RX VCO operates at the frequency of the receiver first local signal and a portion of the signal is fed to a dual modulus counter formed by IC1 and IC2 in Z1. IC1 divides the incoming signal by 1/64 or 1/65 depending on the control line status sent from IC2. The output of the dual modulus counter is also a 12.5kHz and this signal is compared against the 12.5kHz reference signal in a phase comparator at IC2. The output signal from the phase comparator is then fed back to the RX VCO after going through a charge pump and a lowpass filter to maintain the RX VCO frequency.

If this RX frequency synthesizer phase locked loop becomes UNLOCK, the unlock condition is detected by IC2 and it prevents the transmitter frequency synthesizer from sending a transmitter signal to following amplifier stages in order to prevent an unauthorized transmission.

TX Frequency Synthesizer

The TX frequency synthesizer consists of three major circuits. They are the modulator/voltage controlled crystal oscillator (VCXO, Z6), TX voltage controlled oscillator (TX VCO, Z5) and TX phase locked loop unit (TX PLL, Z4).

The audio signal from the microphone amplifier and the Signaling unit is applied to the TX VCO (Z5) and the VCXO (Z6) operating at 12.8MHz to obtain an FM modulated signal. And its frequency stability is maintained within ±2.5ppm from −30°C to +60°C. This output signal is fed to the frequency synthesizer IC (IC2) in Z4. At IC2, this signal is divided by 1024 to become a 12.5kHz reference signal.

The output from the TX VCO operates at the frequency of the transmit signal and a portion of the signal is fed to a dual modulus counter formed by IC1 and IC2 in Z4. IC1 divides the incoming signal by 1/64 and 1/65 depending on the control line status sent from IC2. The output of the dual modulus counter is also a 12.5kHz and this signal is compared against the 12.5kHz reference signal in a phase comparator at IC2. The output signal from the phase comparator is then fed back to the TX VCO after going through a charge pump and a lowpass filter to maintain the TX VCO frequency.

If this TX frequency synthesizer phase locked loop becomes UNLOCK, the unlock condition is detected by IC2 and it prevents the transmitter frequency synthesizer from sending a transmitter.

CIRCUIT DESCRIPTION

Microphone Amplifier

The audio signal originating at the microphone is applied to a microphone amplifier unit (Z7) after going through a microphone sensitivity control (VR1).

The signal is amplified and voltage limited by IC1 and IC2 in Z7, then applied to an active lowpass filter/pre-emphasis network (IC3).

The processed audio signal is sent to the modulator/voltage controlled crystal oscillator (VCXO, Z6) and voltage controlled oscillator (TX VCO, Z5) in the transmitter frequency synthesizer via IC3.

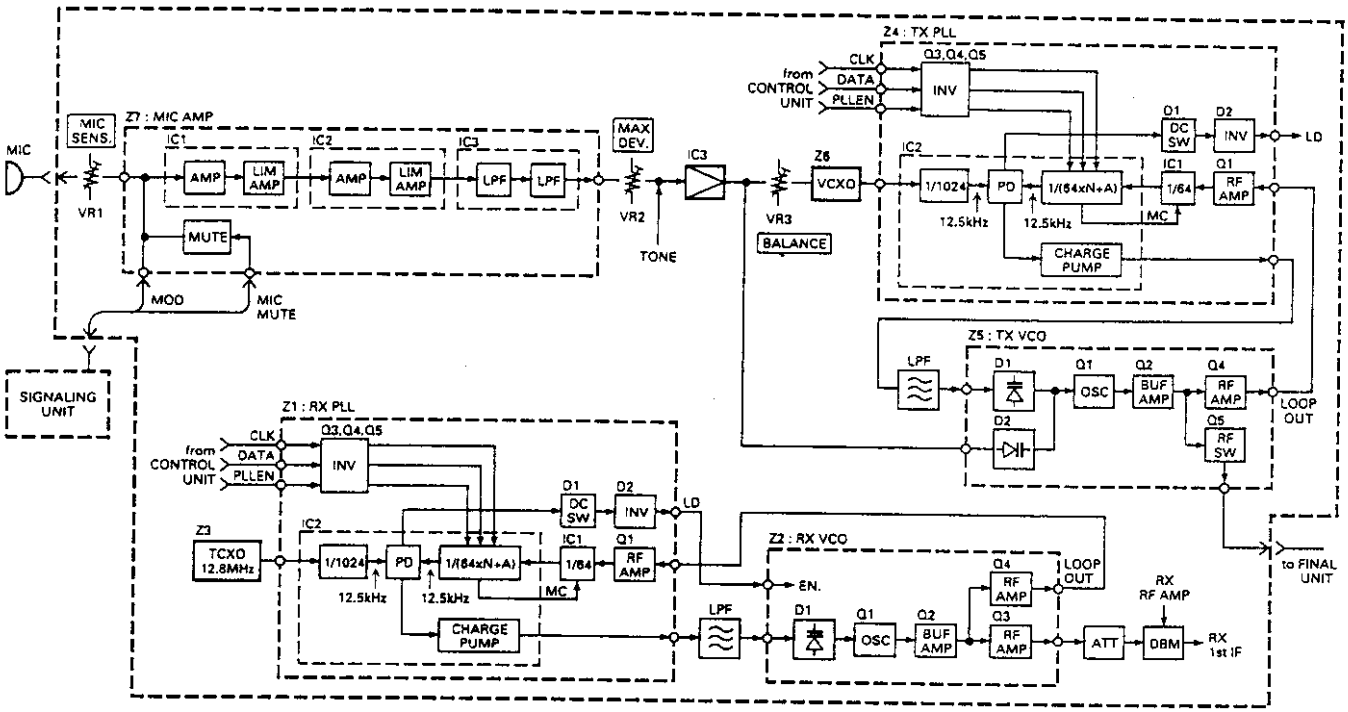
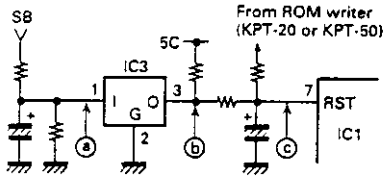


Fig. 4 PLL & Modulation circuit block diagram

Reset Circuit

Upon initial power up, the line voltage gradually increases and this causes the reset system (IC3) to generate a reset pulse. This reset pulse is applied to the microprocessor (IC1) to insure the initialization of the circuit.



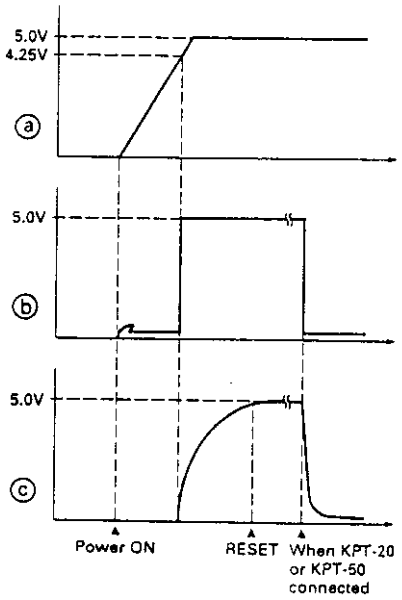


Fig. 5 Reset circuit block diagram

CIRCUIT DESCRIPTION

AVR Circuit

This power supply uses a tapped secondary transformer to maintain low voltage between the pass transistor collectors and emitters (Q5 and Q6) for excellent efficiency. Control and operating voltages are rectified and supplied independently for good ripple characteristics.

Temperature compensation for the regulator Zener diode D5 and error amplifier transistor Q4 is provided by silicon diodes D4 and D6.

At initial POWER-ON Q3 is ON to turn-down Q4 base voltage. This prevents a surge voltage from being output when no load is connected. As C5 charges, Q2 turns ON to shut Q3 OFF. Q4 is thereafter fully ON.

If the load is shorted, comparator Q1 is turned OFF and current proportional only to that in the initial turn-on circuit is output. When the output is shorted, the output current drops to 1A. This circuit protects the pass transistors, transformer and full wave bridge rectifies from thermal damage.

Changing between AC and DC is done with the DC switch (D101) for the TKR-820A only. The output from the AVR unit and the DC input from the external power input terminals are changed automatically.

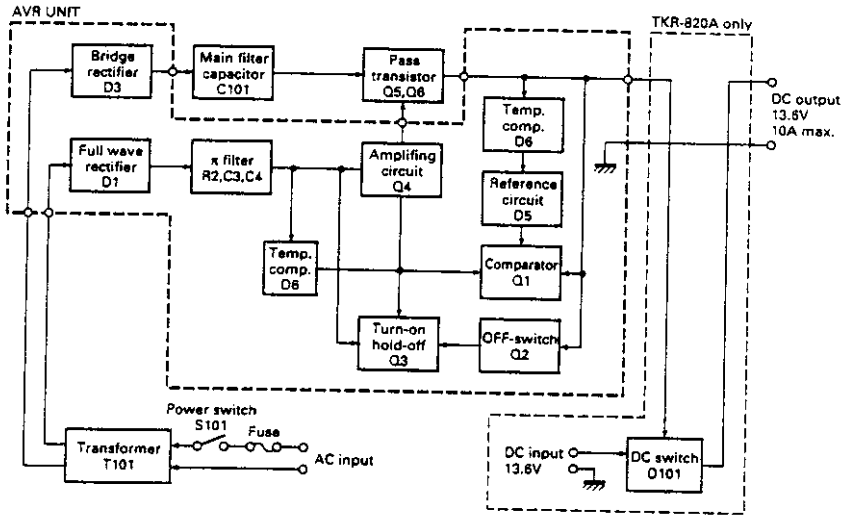


Fig. 6 AVR circuit block diagram

CIRCUIT DESCRIPTION

EEPROM Programming

Programming of data into the EEPROM (IC2) in the Display unit is done by connecting the KPT-20 programmer to the transceiver by cable provided with the KPT-20 or KPT-50. When the programmer is connected to CN1 in the Display unit, this causes microprocessor IC1 to go into reset condition. In the reset condition, the output ports of IC1 becomes high impedance and are isolated from the data transfer lines. This permits data transfers between the programmer and the EEPROM.

Signaling Unit

- **Decoder operation**

The receive audio signal from the receiver section is fed to the Signaling unit. A part of this signal is returned to the receive audio amplifier circuit and fed to mute circuit after going through an active high-pass filter, in which any frequencies below 300Hz are removed. The mute circuit control a transfer audio signal by microprocessor. The other part of the audio signal is fed through a fifth-order active low-pass filter, of which the cut-off frequency is set at 220Hz, to discriminate the QT and DQT signals from other audio signals.

The QT tone obtained from the above filtered audio signal is applied to the microprocessor (IC11) as an analog signal for tone detection after being amplified by IC4 (2/2).

The DQT code is passed through a low-pass filter IC3 (2/2), of which the cut-off frequency is 140Hz, and the circuit consists of IC3 (1/2) and IC5 (1/2), where the DC drift component (low frequency) is removed from the signal. The signal is then amplified by IC5 (2/2). The amplified signal is applied to IC1 after waveform shaping by Q2.

IC11 sends an audio control signal (AC) to the AC terminal of CN1 through an inverter (Q4) according to the status of the incoming signal. If the incoming QT tone or DQT code matches the data stored, the AC terminal of CN1 is forced to become "LOW" to unmute the receive audio circuit.

- **Monitor circuit**

The RESET terminal of CN1 is connected to the MONITOR and MIC MONITOR circuits in the repeater.

The RESET terminal signal level goes to "HIGH" state, if either the MONITOR switch is on or the microphones MONITOR switch is on, causing pin 4 (RESET) of IC11 to become "HIGH". In this condition, the AC terminal of CN1 is held "LOW", enabling only the noise actuated squelch operation.

- **Encoder operation**

In the transmit mode, the PTT terminal of CN1 becomes "LOW" and this information is inverted to "HIGH" by Q7 before being applied to IC11. Upon receipt of this PTT signal or when the programmed tone has been decoded at the time of the REPEAT operation, IC11 starts the encode function. The encode signal is sent out from output ports, A/D 0 through A/D 7, of IC11 in a binary format and is fed to a ladder network resistor (CP1) for Digital-to-Analog signal conversion. The output signal from CP1, which is either the QT tone or the DQT code, is routed to the TONE terminal of CN1 after going through a level control for modulating the transmit signal.

- **Local/Repeater operation**

When the REPEAT switch on the front panel of the main body is set to ON, the repeater operation is engaged, while when this switch is set to OFF, the full-duplex transceiver operation is engaged.

- **Preset squelch operation**

The squelch circuit for the repeater operation which is independent from the main body consists of noise conditioner IC6 (1/2), waveform shaper Q1, microprocessor IC11 and squelch sensitivity adjuster VR1.

The preset squelch level, the hangup timer time and the time-out timer time are compared in IC11 respectively with the voltages at pins 30, 29 and 28 set by VR1, VR2 and VR3 with the reference of the voltage at pin 31 of IC11 and are thus subject to software control.

TAKEOVER Switch

The TAKEOVER switch is used to isolate the remote control. (The remote control is isolated when the TAKEOVER switch is pressed.)