TK-7150 Circuit Description

The Kenwood model TK-7150 is an all solid-state frequency synthesized VHF/FM transceiver designed for operation in the frequency range of 136 MHz to 174 MHz.
This model has maximum 128 channels.
The unit consists of a TX-RX unit and Display unit and its transmitter is rated for 50 W output power.

1. TX-RX Unit

The TX-RX unit consists of phase-locked loop (PLL) frequency synthesizer, receiver, transmitter, and control circuit.

1.1 PLL Frequency Synthesizer

The transmit signal and the receiver first L.O. signal are generated by the PLL digital frequency synthesizer. The frequency synthesizer consists of a transmitter voltage controlled oscillator (TX VCO: Q507), a receiver voltage controlled oscillator (RX VCO: Q509), a buffer amplifier (Q513 and Q515), an RF amplifier (Q516), a low-pass filter (Q501, Q503 and Q504), a PLL IC (IC501), and TX VCO / RX VCO switches (Q510 and Q512).

In the transmit signal mode, an operating frequency programming data is sent to IC501, from the CPU (IC701), to set the programmable counter within IC501. Q512 is turned on to activate the TX VCO and the output signal of the TX VCO is amplified by Q513 and Q516.
The signal is then divided down in frequency, at the programmable counter in IC501, to 5.0kHz or 6.25kHz, 7.5kHz which is compared in phase with a 5.0kHz or 6.25kHz, 7.5kHz reference signal, derived from 16.8MHz VCXO (X501) and a 1/3360 or a 1/2688, 1/2240 fixed counter in IC501, at the phase comparator in IC501. The VCXO operates at 16.8MHz and its frequency stability is maintained within 2.5ppm (temperature range of –30 to +60 degrees).

The phase comparator output signal is fed into a low-pass filter (Q501, Q503 and Q504) before being applied to the TX VCO as a frequency control voltage. If an unlock condition occurs in the phase locked loop, this condition is detected by Q518 and Q519. This cause the transmitter 8V supply cut off, resulting in the prevention of an unauthorized transmission.

The transmitter modulation signals (processed Mic. audio and sub-audible signaling) are applied to the TX VCO for frequency modulation.

In the receive mode, the VCO is substituted with Q509 (RX VCO) and it generates the receiver first local oscillator signal according to the data sent from the CPU (IC701).
The basic operation of the synthesizer remains the same.

1.2 Receiver Circuit

The receiver is double conversion super-heterodyne, designed to operate in the frequency range of 136MHz to 174MHz.
The receiver circuit consists of front-end circuit, First Mixer, IF amplifier circuit, audio amplifier circuit, and squelch circuit.

The front-end circuit consists of former BPF(D209), RF amplifier Q213, and latter BPF (D208,207). The BPF covers frequency ranges 136 to 174MHz. The latter BPF(D208,207) attenuates the unwanted signals, and sends only the necessary signal to the first mixer.

The signal from the BPF is heterodyned with the first local oscillator signal from the PLL frequency synthesizer circuit at the first mixer DBM (Q209,210,211,212) to become a 44.85MHz first intermediate frequency (IF) signal. The first IF signal is fed through two monolithic crystal filters (XF201: Wide, XF202: Narrow) to further remove spurious signals.

The first IF signal is amplified by Q207 and Q206, and then enters IC201 (FM system IC).
The signal is heterodyned again with a second local oscillator signal(44.395MHz) with in IC201 to become a 455kHz second IF signal. The second IF signal is fed through a 455kHz ceramic filters (CF201,203: Wide, CF202,204: Narrow) to further eliminate unwanted signal, and the quadrature detection circuit FM-detects the signal to produce a base-band signal and output it from pin 9.

The recovered audio signal obtained from IC201 is amplified and anti-aliasing filtered by IC712(A/2), inputted to the AINR terminal of CODEC IC (IC713), and audio processed by DSP (IC710).
The processed audio signal from AOUTR terminal of IC713 is amplified and filtered by IC716 (A/2) to a sufficient level. The audio signal goes to an electronic volume (IC718), to the input of multiplexer IC (IC717), and is amplified to drive a loudspeaker by an audio power amplifier (IC720).
The 12W audio output can be provided to external 4 ohms speaker through the 6-pin ACC connector “ES1,ES2” on the rear panel.

The output signal from IC201 enters FM IC again, then passed through a band-pass filter.
The noise component output from IC201 is amplified by Q204 and rectified by D202 to produce a DC Voltage corresponding to the noise level. The DC voltage is sent to the analog port of the CPU (IC701). And IC201 outputs a DC voltage(RSSI) corresponding to the input of the IF amplifier.

1.3 Transmitter Circuit

The transmitter circuit consists of Microphone circuit, Modulation level adjustment circuit, Driver and Final power amplifier circuit, and Automatic power control circuit.

The signal from the microphone is passed through AGC circuit (Q707, Q708 and D711, D712 and IC714 A/2) so that it dose not saturates. The AGC is operated by controlling the + and －side levels of amplitude using the current obtained by positive and negative detection of the amplified audio signal. The audio signal is amplified by IC712 B/2, inputted to the AINL terminal of CODEC IC (IC713), and audio processed by DSP (IC710). The processed audio signal from the AOUTL terminal of IC713 is filtered by IC716 (B/2), and amplified by the summing amplifier IC719 (B/2). The output of the summing amplifier IC719 (B/2) is passed to an electronic volume (IC718) for maximum deviation adjustment before being applied to a varactor diode in the voltage controlled oscillator (VCO).

The transmit signal is generated by the TX VCO, and amplified by Q515, and sent to Driver and Final power amplifier circuit. This amplified signal is amplified by Driver circuit consists of Q1, Q2, and Q4. And this signal is passed to the FINAL stage. The RF power amplifier consists of MOS FET transistor (Q5).
This signal is routed to the antenna connector after going through the antenna switching network and the low-pass filter. This filter has a minimum attenuation of 75dB at the second harmonic

frequency.

The automatic power control (APC) circuit stabilizes the transmitter output power at a pre-determined level. The forward /reflected power detector circuits detects RF power to DC voltage, and consists of RF detector D5, D6 and DC amplifier IC2 (A/2). The voltage comparator (IC2 B/2) compares the voltage obtained by the above detected voltage with a reference voltage, set using the CPU (IC701) and IC718, IC715 (A/2). An APC voltage proportional to the difference between the sensed voltage and the reference voltage appears at the output of IC2. This output voltage controls the gate voltage for the drive amplifier Q4 and final amplifier Q5, which keeps the transmitter output power constant.

1.4 Control Circuit

The control circuit mainly consists of CPU, memory circuit, DSP circuit, and power supply circuit.

The CPU (IC701) controls the flash ROM, the DSP, the receiver circuit, the transmitter circuit, the control circuit, and the display circuit and transfers data to or from an external device.

IC705 has a flash ROM with a capacity of 4M bits that contains the control program for the CPU, the signal processing program for DSP and data such as channels and operating features.
This program can be easily written from an external devices. Data such as the operating status are programmed into the EEPROM (IC704).

The DSP circuit filters transmit/receive audio signal and encode/decodes signaling (QT, DQT, MSK,
DTMF, 2TONE, LTR ID). This circuit consists of IC710, IC706, IC707, IC708, IC709, IC713.
The receive audio signal is converted from analog to digital by IC713 with a sampling frequency of 19.2kHz. The digitized audio signal is sent to DSP IC710 to process the signaling signal and audio signal. The processed digital audio signal is fed to CODEC IC713, converted from digital to analog, and the analog signal is output from pin 16(AOUTR).
The transmit audio signal coming from IC714(A/2) is amplified by IC712(B/2), fed to pin 3 (AINL) of CODEC IC713, and converted from analog to digital at a sampling frequency of 19.2kHz .
The digitized transmit audio signal is AGC-processed , pre-emphasized and filtered at 300Hz to 3kHz by DSP IC710, and the resulting signal is fed back to CODEC IC713, and converted from digital to analog, and the analog signal is output from pin 15 (AOUTL).
IC706,IC707,IC708 and IC709 are interface IC between the CPU operated at 5.0V and the DSP operated at 3.3V.

2. Display Unit

The display unit consists of CPU (IC904), LCD assembly, LED, and other components.

Channels are changed by the rotary encoder (S1). The up/down pulses from the rotary encoder enter the CPU (IC904), and converted to a serial data signal, and are sent to the CPU (IC701) in TX-RX unit. The on/off signals of keys other than the power switch, and the PTT and HOOK signals, are converted to serial data and sent to the CPU (IC701) in TX-RX unit.

Data is displayed on the 12 digits and 3 digits dot matrix alphanumeric display.