Tuning Procedures

Preparation for tuning the transceiver.

Before attempting to tune the transceiver, connect the unit to a suitable power supply. Whenever the transmitter is tuned, the unit must be connected to a suitable dummy load, unless the instruction specify otherwise. The speaker output connector must be terminated with a 8ohm dummy load at any time during the tuning and connected to an AC voltmeter and an audio distortion meter or a SINAD measurement meter at all the time during the tuning.

Transceiver tuning

PLL Section

1) Connect a volt meter to terminal LV and a power meter to antenna connector.
2) Adjust VR203 in the control unit to obtain 450mW power on transmission mode.
3) Adjust TC2 in the RF unit to obtain the 0.7V.
4) Select the frequency to 467.7125MHz (Channel 14)
5) Adjust the frequency to 467.7125MHz ± 100Hz by TC1 in the transmission mode.

Transmitter Section

1.TX Power
1) Select the frequency to 462.6375MHz (Channel 4)
2) Be sure RF output power should be in 200mW to 400mW.

2. Modulation
1) Apply a 1kHz tone with a 50mV(RMS) level to Mic input.
2) Adjust the maximum deviation to 2.0kHz ± 0.05kHz by VR200 in the transmission mode.
3) Reduce the 1khz tone level to 5mV.
4) Be sure modulation should be in 1.2kHz to 1.9kHz in the transmission mode.

3. CTCSS
1) Select tone frequency to 127.3Hz (Tone number 19)
2) Adjust the maximum deviation to 0.3kHz ± 0.05kHz in the transmission mode.
3) Select tone frequency to 67.0Hz (Tone number 01)
4) Be sure modulation should be in 0.25kHz to 0.4kHz in the transmission mode.

Receiver Section

1. Sensitivity
1) Select the frequency to 462.6375MHz (Channel 4).
2) Apply a receive signal with 1kHz modulation and a -120dBm level to the receiver.
3) Be sure SINAD should be in 12dB or more.

2.Squelch

1) Reduce the RF signal level to -117dBm.
2) Be sure squelch should be open.
3) Increase the RF signal level to -123dBm.
4) Be sure squelch should be closed.

Circuit Descriptions

Receiver block

- Front end

  High frequency signals coming from the antenna passes through the low-pass filter, then the RF switch diode (D7) which allows the receiving/transmitting switch (when receiving, the receiver side is conducting) and is input to the SAW filter (L18).

  The SAW filter (L18) rejects the unnecessary bands for the signal from low pass filter. The signal which unnecessary bands were rejected by L18 is amplified by the RF amplifier Q12 and is sent to the first mixer (Q9).

- First mixer

  The signal sent to Q9 is mixed with the first local signal from the VCO and is converted to the first IF signal (21.7MHz).
  (Received frequency - First local frequency = First IF frequency = 21.7MHz)

  The MCF:XF1 (Monolithic Crystal Filter) rejects the unnecessary bands for the first IF signal.
  The first IF signal is amplified by the IF amplifier Q6, then sent to IF IC(IC2).

- IF amplifier

  The IF circuit is configured with the IC2 of IF IC. Local input, mixer, limiter amplifier, FM DET, AF amplifier are contained in the IF IC.
  The IF signal output from the IF amplifier (Q6) is input to the IF IC mixer, is mixed with the second local signal (21.25MHz) and is converted to the second IF signal.
  (21.7MHz - 21.25 MHz = 450kHz).

  The second local signal is common with the PLL reference oscillation.

  The ceramic filter CF1 rejects the unnecessary bands for the second IF signal.
  The second IF signal which passed through the ceramic filter passes through a limiter amplifier composed of a 6-stage direct coupled differential amplifier and is then detected.

  The FM detection is effected with the quadrature detection method. The detection output is obtained by using a Quad coil discriminator to change the limiter amplifier output phase by 90 degrees and by comparing with the original waveform.

· Squelch circuit

A squelch circuit is set up so that no-signal noise or hardly audible low level signals are not output to the speaker, when communicating.

The FM detection output is amplified using the operational amplifier, internal to the base band IC (IC206). It then passes through a high pass filter composed of CR, the noise components of the detected output is converted to a pulse using the IC internal comparator.

This output is input to a microcomputer. In case the pulse output exceeds a certain figure (no signal or low level signal), the DC SW (Q202, 205) turns the power of the audio amplifier IC to off which consequently turns the speaker output to off. Furthermore, in order to reduce the speaker noise output when the audio amplifier switch is used, the direct-coupled FET SW (Q207) is controlled to be turned off before switching the power.

The squelch operating level is set by programming the EEPROM(IC203).

· AF amplifier

The FM detection output passes through the amplifier internal to the base band IC (IC206), the band pass filter (300 to 3kHz), the de-emphasis circuit, the amplifier, the AF volume (VR202) and is then amplified to the specified output level using the AF amplifier (IC207).

Transmitter block

· Microphone amplifier circuit

The audio signal from the microphone passes through the amplifier internal to the base band IC (IC206), the 6dB/OCT pre-emphasis circuit, the band pass filter (300 to 3kHz), the amplifier, the limiter. The distortion component out of audio band is then removed by the splatter filter.

· Modulation circuit

The microphone amplifier output passes through the VR200 for modulation adjustment, is applied to the modulation input of the VCO circuit and is variable-reactance phase modulated.

· Transmission output circuit

The VCO output is amplified by the RF amplifier (Q8,10,11 and 13), passes through the switch diode (D7) (conducting when transmitting), the low pass filter and is

supplied to the antenna.

- Low pass filter circuit
  The output signal filtering is performed a 2-stage Chebyshev type lowpass filter located between the antenna and the transmission/reception switch circuit. This filter has an insertion loss of 0.5dB or less and a minimum attenuation of 35dB at the second harmonics frequency. The second harmonics attenuation at the output of Q13 is 15dB or more. Therefore, the total attenuation of any frequency above the second harmonic signal is guaranteed to be grater than 50dB.

PLL block

- VCO circuit
  The VCO is contained in a shield case.
  The constituents are a transistor for oscillation (Q4), a variable capacitance diode for frequency control (D2), a variable capacitance diode for modulation (D4), a diode for the transmission/reception oscillating frequency shift (D3), a transistor for control (Q3) and an oscillator buffer amplifier (Q7).
  The shift signal T/R at reception becomes 'H', Q3 is turned to ON and the shift diode (D3) is conducting, Q4 oscillates at the received first local frequency.
  (Received channel frequency - 21.7MHz)
  The shift signal T/R at transmission becomes 'L', Q3 is turned to OFF and D3 is brought out of conduction, Q4 oscillates at approximately 460MHz and VCO oscillating frequency = transmission channel frequency.
  3.0V passes through a ripple removing filter circuit Q5 and is used as the circuit voltage.

- PLL circuit
  At power-on, at channel switch and at transmission, the frequency data is sent as a serial data from the microcomputer to the PLL IC (IC1). This sets the programmable frequency divider internal to the PLL IC.
  A stable reference oscillating frequency of 21.25MHz is obtained using a TCXO X1 and a PLL IC internal CMOS oscillator. It is then divided to obtain a 12.5kHz PLL comparison frequency.
  Input from the VCO is divided using a ratio present in the PLL IC internal frequency divider and becomes a comparison frequency of 12.5kHz. It is then compared with the reference comparison frequency with the phase comparator and the phase shift is detected.
  The PLL IC internal charge-pump circuit converts it to a control voltage which

directly drives the VCO.

The obtained control voltage passes through a loop filter with a low band pass characteristics, is applied to the VCO control terminal and the oscillation frequency is controlled. The loop filter removes unnecessary higher harmonic elements and noise contained in the output of the phase comparator and at the same time, determines the PLL response characteristics and synchronization properties with the amplitude or phase characteristics.

· Unlock detection circuit

At channel switch or transmission/reception switch, during the process of synchronization or when in some way synchronization was impossible, an unlock detection signal 'L' is output from the PLL IC. This signal is sent to the microcomputer and is used to disable transmission in an unlock position.

Control block

· Reset circuit

At power-on, after approximately 500 μ s, the microcomputer (IC200) power becomes the operating voltage and approximately 500 μ s later, the voltage detection IC (IC201) sets the reset terminal to 'H' and reset is operated.

When the battery is extracted, the voltage detection IC (IC202) detects the reduction of the B power and the detection output is changed from 'H' to 'L', is applied to the microcomputer VD terminal and stops the microcomputer operation.

· Battery voltage detection circuit

This device features a function which detects the reduction of the battery voltage and indicates it by flashing the LCD BATT display. The battery voltage is divided and applied to the microcomputer analog value input terminal (BATT), A/D converted and compared with the reference voltage from the 3M power. If the value is smaller than or equal to the preset value, it flashes the LCD BATT display of the power display.

Upon production, the display is set to flash when the voltage of the battery terminal is reduced to 3.5V.

· Power circuit

Power becomes a constant-voltage of 3.0V using a series regulator (IC204). It is used as it is as the 3M power for the microcomputer.

The transmission power 3T is supplied to the transmission output circuit as the microcomputer turns the Q204 ON only on transmission.

The reception power 3R is supplied to the reception circuit and/or IF circuit as the microcomputer turns the Q203 (1/2) ON only on reception.
The common power to transmission and reception 3C is supplied to the VCO circuit and the PLL circuit as the microcomputer turns the Q203 (2/2) ON on reception and on transmission.
The 3MS power interlocked with the power switch is supplied to the base band IC (IC206) and/or the frequency divider (IC205) as the microcomputer turns the Q201 ON when the power switch is ON.
When no input is received for 10 seconds, the device enters the power saving mode. The microcomputer sends signals for a synchronization of ON state 1, OFF state 4, the common power 3C and the reception power 3R repeat the ON/OFF and saves the consumption of the battery. When the power saving mode continues for two hours, the device enters the auto power off mode. The common power 3C, the reception power 3R and the 3MS power interlocked with the power switch are all turned OFF.

- Remote control circuit

The voltage of the REM (remote) terminal of the CPU (IC200) is A/D converted and the device operates remotely accordingly to the voltage.
Under normal circumstances, the REM terminal is set to a voltage of approximately 3.0V using R218. When the remote control microphone is switched on, the serial resistance to the switch and the voltage divided by R201 allows to discriminate which switch has been pushed on.

- CTCSS circuit

The serial data from the CPU (IC200) sets the tone frequency of the base band IC (IC206).
Upon reception, the FM demodulation output is input to the IC206 RX IN terminal and when the tone frequency coincide, the IC206 DET OUT terminal turns to 'L' level, is applied to the microcomputer port, turns the MU1 to 'H' level and turns the power of the AF amplifier to ON. When the tone frequency does not coincide, audio signals are not output from speakers.
Upon transmission, the tone set by the microcomputer is output from the IC206 TX TONE terminal, is set to level using VR201 and modulates the VCO through the IC206 internal thumbing amplifier.

DESCRIPTION OF COMPONENTS

KENWOOD

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TX-RX Unit (X57-5840-10) (A/2) : Control

Ref. No.	Part number	Use/Function	Operation/Condition/Compatibility
Q200	DTC123JE	Lamp LED switch	On when lamp LED on
Q201	DTA123JU	3MS switch	3MS (3.0V)
Q202	2SK1824	DC switch	AF power off when mute (MU1)
Q203	FMA5	3R, 3C switch	3R (3.0V), 3C (3.0V)
Q204	KTA1298(Y)	3T switch	3T (3.0V)
Q205	2SB815(6,7)	DC switch	AF power off when mute (MU1)
Q206	DTC314TK	AF switch	On when microphone mute (MM)
Q207	2SK1588	AF switch	Off when mute (MU3)
Q208	2SD1757K	AF switch	On when mute (MU2)
IC200	M38223M4472GP	CPU	
IC201	PST9124NR	Voltage detection	2.4V, CPU reset
IC202	PST9130NR	Voltage detection	3.0V
IC203	AT93C4610SI1.8	EEPROM	
IC204	S-81330HG-KB	AVR	3M (3.0V)
IC205	TC7W74FU	Divider	7.3728MHz → 3.6864MHz
IC206	AK2342B	CTCSS	
IC207	NJM2070M	AF amplifier	2 : Input, 6 : Output
D200	B30-2143-05	lamp LED	
D201	DAN202U	Separator	
D202	MA742	Tone signal detection	
D203	MA742	Microphone tone quality detection	
D204	DTZ3.0(A)	FPU programming	For M-type used only, Over voltage protection

TX-RX Unit (X57-5840-10) (B/2) : RF

Ref. No.	Part number	Use/Function	Operation/Condition/Compatibility
Q1	2SC4215(Y)	Buffer	
Q2	2SC5108(Y)	RF amplifier	
Q3	2SK1824	DC switch	On when RX
Q4	2SC5066(0)	Oscillator	RX:440.8625 ~ 446.0125MHz, TX:462.5625 ~ 467.7125MHz
Q5	2SC4617(S)	Ripple filter	
Q6	2SC4649(N,P)	IF amplifier	1st IF 21.7MHz
Q7	2SC5108(Y)	Buffer	
Q8	2SC5108(Y)	RF amplifier	
Q9	3SK309	1st mixer	RX frequency – Local oscillation frequency
Q10	2SC5108(Y)	RF amplifier	For TX
Q11	2SC4226(R24)	RF amplifier	For TX
Q12	3SK309	RF amplifier	For RX
Q13	AT-31625	RF power amplifier	Transmit power
IC1	TB31202FN	PLL IC	
IC2	TA31136FN	FM IC	
D2	MA2S376	Variable capacitance diode	VCO frequency control
D3	HSU277	RF switch	
D4	MA360	Variable capacitance switch	VCO modulation
D5	ISS355	Speed up	For 3C
D6	ISS312	RF switch	On when TX / RX
D7	MA2S077	RF switch	TX / RX switch
D8	MA742	Amplitude restriction	Surge absorption
D9	MA2S077	RF switch	TX / RX switch