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Preliminary Specification

For

WaveLAN-II/PC Card type 2 Turbo 11Mbps

Source Organization: Lucent Technologies Nederland B.V. / WCND

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Change sheet

		Description of change			Approval
Rev.	Date	Pages	Par.		& Date

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Data Sheet status

Data sheet status	Product status	Definition
Target specification	Development	This specification contains the design target or goal specifications for product development. Specifications may change in any manner.
Preliminary specification	Qualification	This specification contains preliminary data, and possible supplementary data will be published at a later date.
Functional specification	Production	This specification contains final product functional specification.

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1 EXECUTIVE SUMMARY

1.1 Scope

This document specifies the hardware functions and requirements for WaveLAN -II Network Interface Card (NIC) operating in the 2.4GHz band, having PC Card standard type -II extended form factor. The Network Interface Card complies to the IEEE802.11 Wireless LAN Medium Access Control (WMAC) standard and the IEEE802.11 Physical Layer (PHY) standard for Direct Sequence Spread Spectrum.

1.2 Functional Summary

The Network Interface Card is capable to operate in quasi -static indoor environments. It functions as an interface b etween the PC Card Host bus and the Wireless Local Area Network (WLAN) transport medium (free space).

The Network Interface Card covers 1Mbit/s DBPSK and 2Mbit/s DQPSK modulation as defined in the IEEE802.11 PHY standard for Direct Sequence Spread Spect rum (DSSS). As enhanced functionality, it also covers 5.5Mbit/s and 11Mbit/s Complementary Code Keying (CCK). These Physical Layer characteristics comply with the regulations of the Federal Communication Committee (FCC) Part 15, Japanese MPT and European E TS regulations. The 2.4GHz ISM band is used for information transmission in compliance with government regulations.

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2 REFERENCE DOCUMENTS

2.1 WCND reference documents

TAS-25004	Top-level Architecture Specification for WaveLAN -II: System.
SFS-25011	System Functional Specification for WaveLAN -II PCMCIA NIC and Software.
407-0024595	Functional Specification for Hermes WMAC controller.
CIS-010127	Functional Specification Card Information Structure (CIS)

2.2 EMC radio and safety regulations and standards

1	USA	FCC CFR47 Rules and Regulations Part 2 and Part 15, Radio Frequency Devices.
2	USA	UL1950 Product Safety Standard for IT Equipment.
3	Canada	ISC RSS-210 Low-Power Radio Communication Devices.
4	Japan	VCCI Voluntary Control Council for Interference of IT Equipment.
5	Japan	MPT ordonnance 78/79 and MPT announcement 579 Radio Regulations.
6	Europe	ETS 300-826 General EMC standard.
7	Europe	ETS 300-328 Wide-Band Transmission systems in 2.4GHz ISM band.
8	Europe	EN55022 EMC emissions for IT Equipment.
9	Europe	EN60950 Product Safety Standard for IT Equipment.
10	International	CISPR 22 EMC emissions for IT Equipment.
11	International	IEEE.C95,1-1991 Standard for Safety Levels wrt Human Exposure to RF EM fields 3kHz-300GHz.
12	International	IEC950 Product Safety Standard for IT Equipment.

2.3 Other documents and standards

13	P802.11	Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications, November 18, 1997.
14	IEEE Std 802.11b/D4.1	Draft supplement to IEEE802.11 - 1997 edition (CCK addition)
16	0295-02-1500	PCMCIA/JEIDA PC card Standard Volume 2: Electrical Specification, First Printing February 1995.
17	0295-03-1500	PCMCIA/JEIDA PC card Standard Volume 3: Physical Specification, First Printing February 1995.
18	0295-04-1500	PCMCIA/JEIDA PC card Standard Volume 4: Metaformat Specification, First Printing February 1995.
19	0295-10-1500	PCMCIA/JEIDA PC card Standard Volume 10: Guidelines, First Printing February 1995.
20	0295-11-1500	PCMCIA/JEIDA PC card Standard Volume 11: PCMCIA Specific Extensions, First Printing February 1995.

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3 GENERAL DESCRIPTION

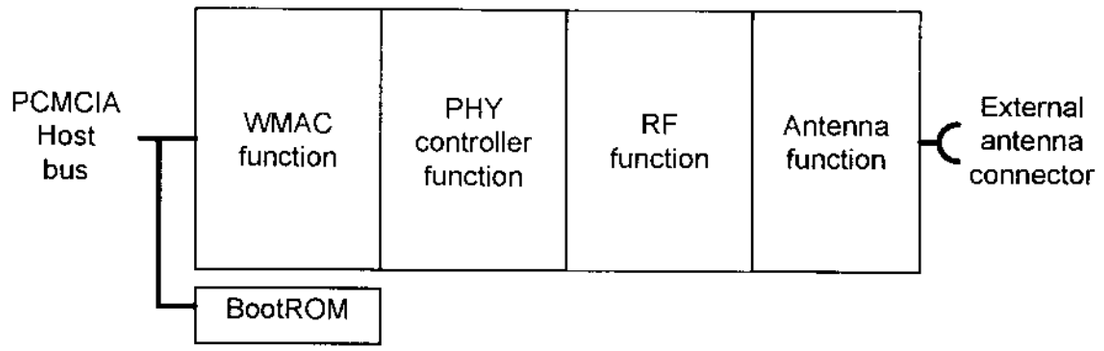

Figure 1: Functional diagram of the WaveLAN-II Network Interface Card.

3.1 Wireless Medium Access Controller function

The Wireless Medium Access Control (WMAC) function of the NIC provides for the data communication protocol and control of the Physical Layer. The WMAC function is built up by the Hermes WMAC controller with 128Kx8 peripheral flash EEPROM [1] and 128Kx8 peripheral RAM. The WMAC functions are described in the "Functional Specification for Hermes WMAC Controller".

In this document, the Wireless Medium Access Controller functio n is referred to as WMAC.

3.2 PHY controller function

The PHY controller function of the NIC is implemented by a DSP ASIC and provides the core Direct Sequence Spread Spectrum (DSSS) Physical Layer functionality and control of the RF Section. It communicates with the WMAC for data exchange, Physical Layer control and parameter setting.

In this document, the PHY controller is referred to as DSP.

3.3 RF function

The RF function of the NIC provides the functionality in which the spre aded signal from the DSP is modulated onto an RF carrier and transmitted, while received RF signals are demodulated and the resulting spreaded signal is passed to the DSP. Its hardware implementation is referred to as RF Section.

3.4 Antenna function

The Antenna function of the NIC provides a built -in Diversity Antenna and a connection to an optional external Diversity Antenna module. The internal Diversity Antenna is disabled if a plug is inserted on the external antenna connector. The Diversi ty Antenna contains two radiating elements: One of them is used for transmission; while one out of two can be selected for reception. Antenna selection is controlled by the DSP.

3.5 BootROM

The BootROM is an optional 32Kx8 or 128Kx8 EEPROM con nected directly to the PCMCIA bus facilitating diskless platforms. The BootROM is used at Host startup only and is no functional part of the Network Interface Card.

[1] Recommended flash EEPROM type is AT29LV010.

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4 PHYSICAL ENVIRONMENT

The Network Interface Card shall comply to the PC Card Standard, February 1995, as defined in "PC Card Standard Volume 3: Physical Specification ".

4.1 Dimensions

The Network Interface Card shall comply to the PCMCIA standard, February 1995, for type - II extended PC cards as defined in "PC Card Standard Volume 3: Physical Specification, Section 3: Card Dimensions" and 'PC Card Standard Volume 11: PCMCIA Specific Extensions". The length of the thick extension part (dimension "D" in PC Card Standard Volume 11, Section 4) shall not exceed 24 mm.

4.2 Operating and Storage Environment

The Network Interface Card shall be capable to pass the environmental tests as specified in "PC Card Standard Volume 3: Physical Specification, Section 9: PC card Environmental ".

Operating temperature range:	0°C to 60°C ambient temperature. NIC operating within specifications.
	-20°C to 70°C ambient temperature. NIC operating, may not be within specifications.
Relative humidity when operational:	95% maximum (non condensing).
Storage temperature range:	-20°C to 75°C ambient temperature.
Relative humidity during storage:	95% maximum (non condensing).

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5 OPERATIONAL ENVIRONMENT

The Network Interface Card shall comply to the PCMCIA standard, February 1995, for 16 - bit PC cards as defined in "PC Card Standard Volume 2: Electrical Specification ". I/O operations can be 16-bit.

5.1 Power supply

The Network Interface Card shall be capable to operate from both 5V and 3.3V Host supply voltage. Refer to Section 12.1 for configur ation of card type and supply voltage. The peak current consumption, which is current consumption averaged over 10ms and the average current consumption (averaged over 1s) will not exceed the following values:

mode	
Doze	15mA
Receive	240mA
Transmit	330mA

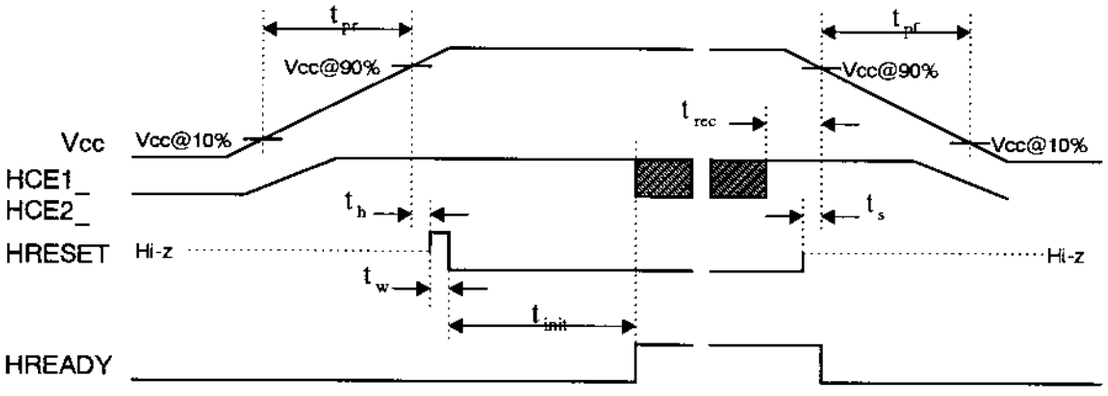
A 120mV peak-peak ripple on the supply voltage with a fundamental frequency not greater than 150kHz shall not degrade the Network Interface performance.

The total load capacitance of the supply voltage shall not exceed 150µF in order to meet the inrush current requirement.

5.2 Power-up and Reset

After power-up, a hardware reset or a COR reset, the Network Interface Card shall be reset and operate as memory-only card in Doze mode. The Network Interface Card shall not leave Doze mode prior to configuration as I/O card by setting bit 0 of the Configuration Index in the Configuration Option Register (COR).

Figure 2 shows the power-up and power-down timing sequence for PCMCIA release 2.0 or higher / JEIDA release 4.1 or higher[2] as applied by the WMAC. A pull-up resistor on the HRESET line in the NIC is recommended in order to keep the NIC in reset state when the HRESET line is in high impedance state during power-up and power-down.



Item	Symbol	Value Min.	Max.	Unit	notes
Vcc rising time	t_{pr}	0.1	100	ms	

[2] PCMCIA release 1.0 and JEIDA release 4.0 always keep RESET asserted (high).

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Vcc falling time	t_{pf}	3.0	300	ms	
Reset holdoff time	t_h	1		ms	
Reset width	t_w	.01	600	ms	see chap 11.1.2
Reset shutdown time	t_s	0		ms	
WMAC init time	t_{init}	20		ms	

Figure 2: Power-up and power-down timing sequence.

Figure 3 shows the hardware reset timing sequence for PCMCIA release 2. 0 or higher / JEIDA release 4.1 or higher as applied by the WMAC.

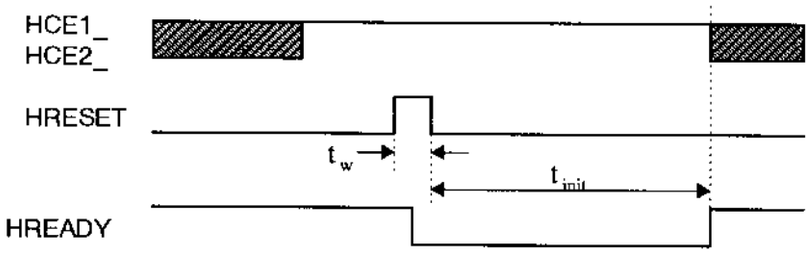

Figure 3: Hardware reset timing sequence.

Upon assertion of the HRESET line, the WMAC clears the COR register, configures the NIC as memory-only card and negates the HREADY line The WMAC assert the HREADY line as soon as the NIC is accessible with CIS available. Refer to "PC Card Standard Volume 2: Electrical Specification" Section 4.12 for more details.

Refer to Section 6.1 for COR reset.

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6 CONFIGURABILITY

6.1 Function configuration registers.

The WMAC only supports the Configuration Option Register (COR) located in the attribute memory space at address 3E0h (Section 12.1.2). The Host software shall obtain this address from CISTPL_CONFIG (Section 6.2.9).

b7	b6	b5	b4	b3	b2	b1	b0
CRESET	LevIREQ	Configuration Index					

CRESET

COR reset bit. Setting this bit places the Network Interface Card in reset state. This is equivalent to the Host asserting HRESET, except that thi s bit is not cleared. The Host shall clear this bit by writing 00h to the COR register in order to assure that the NIC continues as memory-only card after the software reset.

LevIREQ

When set, the WMAC shall generate level -mode interrupts. When cleared, t he WMAC shall generate pulse-mode interrupts. The WMAC supports both interrupt modes.

By default, the level-mode interrupt shall be used.

Configuration index

The NIC is configured as memory-only card if the configuration index is 00h. The card is configured as I/O card by writing 01h to the configuration index.

By default, the card is configured as I/O card by writing 41h to the COR register.

6.2 Card Information Structure

The Card Information Structure (CIS) is accessible by the Host through the attribute address space (Section 12.1.2). The WMAC downloads the CIS from its non -volatile memory in the attribute memory after a reset.

The CIS shall contain the following : See CIS (010127)

6.3 Configuration parameters

All configuration parameters of the Network Interface are stored in non -volatile memory of the WMAC and are accessible by the Host. Refer to the Functional Specification for Hermes WMAC Controller.

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7 SECURITY

The Network Interface supports the IEEE-WEP algorithm and RC4 enhanced encryption for anti-eavesdropping security.

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8 COMPATIBILITY

The Network Interface Card shall comply to the PCMCIA Standard, February 1995.

The Network Interface shall comply with the IEEE802.11 standardized Wirel ess Medium Access Control (WMAC) and the IEEE802.11 Physical Layer (PHY) standard for Direct - Sequence Spread Spectrum (DSSS).

The PHY standard covers 1Mbit/s Differential Binary Phase -Shift Keying (DBPSK) and 2Mbit/s Differential Quadrature Phase -Shift Keying (DQPSK). In addition, the Network Interface also supports 5.5Mbit/s and 11Mbit/s Complementary Code Keying (CCK)..

The WaveLAN-II Network Interface shall be coexistent with a WaveLAN(-I) 2.4GHz Network Interface for 1Mbit/s DBPSK and 2Mbit/s DQPSK wh en operating on the same RF center frequency.

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9 MIGRATION

An optional external Range Extender can be connected to the Network Interface Card. When inserting a plug on the external antenna connector, the internal Diversity Antenna is disabled.

The Network Interface Card also supports an active external antenna with RF power booster.

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10 LEGAL, REGULATORY AND OTHER TECHNICAL CONSTRAINTS

10.1 Electromagnetic compatibility

The Network Interface Card will comply with the following EMC regulations and standards and will be certified accordingly:

Emissions:	USA:	FCC CFR47 Part 15
	Japan:	VCCI
	Europe:	EN55022
	Europe:	ETS 300-826

The product will meet the Class B limits.

Immunity:	Europe:	ETS 300-826

For Europe the product will comply with the EMC Directive 89/336/EEC

The Network Interface Card will comply with PC Card Standard Volume 3: Card Physical, specifying ESD requirements.

10.2 Product Safety

The Network Interface Card will comply with the following product safety standards for IT Equipment:

USA	UL1950
Europe:	EN60950

The product will operate at Safety Extra Low Voltages supplied by the host unit.

10.3 Radio Regulations

The Network Interface Card will comply with the following radio regulations/standards and will be certified accordingly:

USA:	FCC CFR47 Part 15, section 15.247
Canada:	ISC RSS210
Japan:	MPT Radio Regulations
Europe:	ETS 300-328

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11 PERFORMANCE REQUIREMENTS

11.1 General

Receiver input levels and transmitter output levels are specified at either the external antenna connector or the feeding point of the internal main antenna.

11.1.1 Antenna port impedance

The nominal antenna port impedance is 50 Ω.

The Network Interface Card shall not be damaged and remain unconditionally stable for any Voltage Standing Wave Ratio (VSWR) 0 ≤VSWR≤ ∞.

11.1.2 Power-on start-up time

The Network Interface Card shall be operational within 600ms after switching the powe r supply on. This includes a delay of max 500 ms for the Flash ROM power up sequence.

11.1.3 Doze to receive mode start-up time

The Network Interface Card shall be operational within 0.75ms after switching from Doze mode to Receive mode. This includes lock-in and stabilization of the synthesizers (see Section 11.1.6). Transmissions are not allowed during this period.

11.1.4 Receive to transmit turnaround time

The time from transition of the TXE control line (transmit enable control line from WMAC to DSP) from inactive state to active state until the RF section is in transmit mode shall be not more than 5µs. The NIC is said to be in transmit mode at the moment the RF output power level is within 90% of its final value.

11.1.5 Transmit to receive turnaround time

The time from transition of the TXE control line (transmit enable control line from WMAC to DSP) from active state to inactive state until the NIC is in receive mode shall be not more than 10µs.

11.1.6 RF center frequency

The RF function provides programming of the RF center frequency from 2400MHz to 2500MHz in steps of 1MHz. This covers all IEEE802.11 RF channel frequencies listed in Section 13.6.

The RF center frequency for transmission and reception shall b e stable within 25kHz of its final value, 0.75ms after reprogramming or switching from doze mode to receive mode.

11.1.7 RF center frequency and clock accuracy

The master clock frequency and the RF center frequency shall be within +/ -25ppm of the nominal value.

The carrier jitter is within 25kHz of its final value 40µs after switching between RX and TX mode.

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11.2 Transmitter

11.2.1 Transmit power-on and power-down ramp

The transmit power-on ramp from 10% to 90% of the maximum power shall not take longer than 2µs.

The transmit power-down ramp from 90% to 10% of the maximum power shall not take longer than 2µs.

The transmit power ramp shall be constructed such that the emissions comply with the radio regulations mentioned in Section 10.

11.2.2 Transmitted power level

The transmitted power shall be between 10dBm and 20dBm EIRP with nominal values of 15dBm EIRP for 1 and 2Mbit/s and 12dBm EIRP for 5 and 8Mbit/s. This range complies with the IEEE802.11 PHY standard and the radio regulations according to Section 10.

The power density shall not exceed 10dBm/MHz EIRP (ETS), including an external antenna.

11.2.3 Transmitted output spectrum

The transmitted spectral products shall be less than –30dBr (dB relative to the sin(x)/x peak) for frequencies between 11MHz and 22MHz from the center frequency and –50dBr for frequencies more than 22MHz from the center frequency as illustrated in Figure 4. The measurement shall be made at the antenna port u sing 100kHz resolution bandwidth.

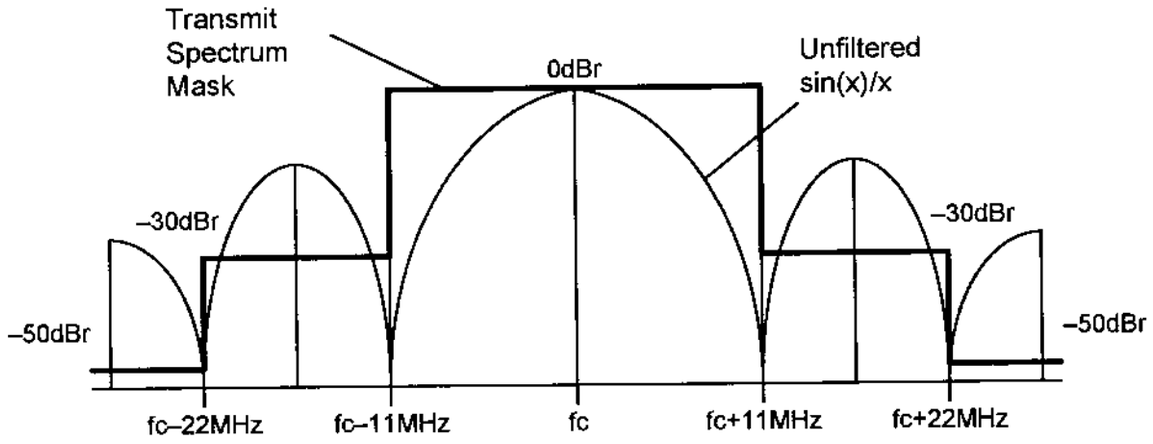

Figure 4: IEEE802.11 transmit spectrum mask.

11.2.4 RF carrier suppression

The RF carrier suppression measured at the channel center frequency shall be at least 15dB below the peak sin(x)/x power spectrum.

11.3 Receiver

11.3.1 Medium busy

The DSP reports to the WMAC the presence of a spread -spectrum signal on the medium by the MBUSY signal.

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MBUSY is set if a spread-spectrum signal is present on the medium with a level above the *defer threshold*. This *defer threshold* shall cover the input range from the *minimum input level sensitivity* conform 11.3.3 to the *maximum input level* conform 11.3.4 in steps of 1dB.

MBUSY is set at the end of an antenna slot according to Figure 5. If the signal is present within 5µs from the start of a slot (15µs before the end) MBUSY must be set at the end of the same slot, else MBUSY may be set at the end of the next slot. The antenna slot time is 20µs.

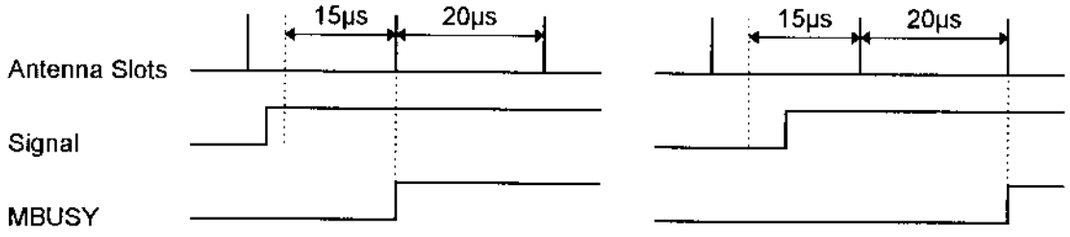

Figure 5: MBUSY active timing.

MBUSY is cleared at the end of a received frame.

11.3.2 Carrier Detect threshold

The receiver is activated if a spread-spectrum signal is present on the medium with a level above the *Carrier Detect threshold*. Incoming signals below that threshold are ignored.

The Carrier Detect threshold shall cover the input range from the *minimum input level sensitivity* conform 11.3.3 to the *maximum input level* conform 11.3.4 in steps of 1dB.

11.3.3 Minimum input level sensitivity

- an input level of -93dBm at 25°C or -91dBm at full operational temperature range, measured at the antenna connector using 1Mbit/s DBPSK modulation
- an input level of -90dBm at 25°C or -88dBm at full operational temperature range, measured at the antenna connector using 2Mbit/s DQPSK modulation
- an input level of -87dBm at 25°C or -85dBm at full operational temperature range, measured at the antenna connector using 5.5Mbit/s CCK modulation.
- an input level of -84dBm at 25°C or -82dBm at full operational temperature range, measured at the antenna connector using 11Mbit/s CCK modulation.

The test for the minimum input level sensitivity shall be conducted with the *Carrier Detect threshold* set less than –95dBm.

11.3.4 Maximum input level

The FER shall be less than $8*10^{-2}$ (1024 byte frames) for a maximum input level of –4Bm measured at the antenna connector. This applies to all modulation types and data rates.

11.3.5 Over-voltage protection

The receiver shall not be damaged by over-driving levels up to +17dBm at the antenna connector. No DC voltage shall be exposed to the antenna input.

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11.3.6 Adjacent channel rejection

The adjacent channel rejection sh all be at least 35dB with a FER of $8*10^{-2}$ (1024 byte frames) using DQPSK and CCK modulation.

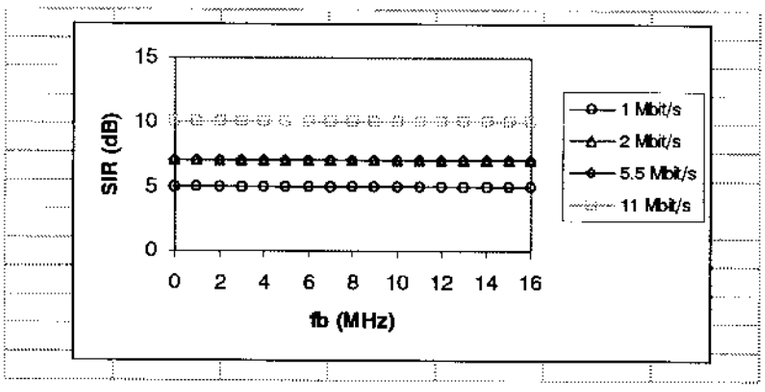
The adjacent channel rejection shall be measured using a WaveLAN input signal at a level of 6dB above the *minimum input level sensitivity (Ref. 14: -80dBm for 2Mb/s DQPSK modulation, -76dBm for 11Mb/s CCK modulation)* as desired input signal. The adjacent channel signal being modulated in a similar matter and compliant to the *transmitted spectrum mask,* shall have a level of 41dB above the *minimum input level sensitivity.* The adjacent channel signal must be derived from a separate signal source. The center frequency spacing shall be 25MHz or more. Under these conditions, the FER shall be no worse than $8*10^{-2}$.

11.3.7 FCC spreading gain

The unit shall comply with a minimum processing gain of 10dB, as specified in Ref.1
A WaveLAN signal is applied together with a Continuous Wave (CW) interference signal at the receiver input. The level of the WaveLAN signal is –55dBm. The interference signal is stepped in 50kHz increments across the passband of the system. The minimum Signal to Interference Ratio (SIR) needed for a BER better than $1*10^{-8}$ is shown in Figure 6 for each data rate as a function of fb=|fc -fint|, where:

fb is the down converted base-band interference frequency.
fc is the carrier frequency of the WaveLAN signal.
fint is the CW interference frequency.

The SIR is calculated discarding the worst 20% of the SIR data points. Note that total losses in the system should be assumed to be no more than 2dB. (See Ref.1)



SIR(1Mbps) = 5dB
SIR(2Mbps) = 7dB
SIR(5.5Mbps) = 7dB
SIR(11Mbps) = 10dB

Figure 6. SIR frequency mask.

11.3.8 Out-of-band signal rejection

A WaveLAN signal is applied together with two Continuous Wave (CW) int erference signals at the receiver antenna input. The level of the WaveLAN signal is –55dBm. The CW interference signals have equal level and 1.2MHz frequency distance. The maximum level of each of the two interfering CW signals for a FER better than $8*10^{-3}$ (1024 byte frames) is shown in Table 1 as a function of the average frequency of both interfering frequencies.

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Average frequency of interferers	max. level of each interferer for 10^{-5} BER, $T_{AMBIENT}$ = 25°C 2Mbit/s DQPSK
<1.0GHz	-6dBm
1.0-2.0 GHz	-10dBm
2.0-2.35 GHz	-26dBm
2.55-2.9 GHz	-26dBm
>2.9 GHz	-10dBm

Table 1: Out of band maximum interference levels.

11.3.9 Irreducible Frame Error Ratio

The Irreducible FER (1024 byte frames) in an RF-clean environment (anechoic chamber) at nominal temperature between two Network Interfaces one meter apart using 2Mbit/s DQPSK will be better than $1*10^{-8}$.

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12 INTERFACES

12.1 Host interface

The Network Interface is connected to the Host through the PC Card type-II interface bus, for which the interface lines are defined in "PC Card Standard Volume 2: Electrical Specification". The PC Card hardware can be configured as 8/16-bit PC card capable of 8/16-bit I/O operations.

The Network Interface power is supplied by the Host through both Vcc lines. The Vpp[1::2] lines are not used. All four ground lines are directly connected to the Network Interface ground plane.

The following signal lines are connected to the WMAC:

HA[0::9]	The lower ten bits of the 26-bit address bus are used.
HD[0::15]	The 16-bit data bus.
HCE[1::2]_	Card enable 1 and Card Enable 2.
HOE_	Output enable.
HWE_	Write enable.
HIORD_	I/O read (if I/O card).
HIOWR_	I/O write (if I/O card).
HIREQ_ / HREADY	Interrupt request (if I/O card) / Card Ready (if memory-only card).
HWAIT_	Extend bus cycle.
HINPACK_	Input acknowledge (if I/O card), may be used for DMA request.
HREG_	Register select line for attribute memory access (if low).
HSTSCHG_	Card status change (if I/O card).
HRESET	Hardware Reset command from the Host[3].

The following signal lines are used for a 32K/128Kx8 BootROM:

HA[0::14/16]	The lower 15 address lines.
HD[0::7]	The lower 8 bits of the data bus.
HOE_	Output enable.
HWE_	Write enable.
BOOTCS_	= not(HREG_) + HCE1_ . HCE2_.

The following lines are used for hardware card configuration:

HCD*[1::2]	Card Detect 1 and Card detect 2. These lines are connected to ground.
HIOIS16_	16-bit I/O operation capability, connected to ground.
HVS[1::2]	Voltage Select to be connected according to Table 2.

	5V-only card	3.3V-only card	5V/3.3V card
HVS1	open	ground	ground
HVS2	open	open	open
socket	5V key	low-voltage key	5V key

Table 2: Configuration of the Voltage Select lines.

12.1.1 Common memory address space

The WMAC has no common memory. The common memory of the NIC is occupied by the BootROM only.

[3] A 100kΩ pull-up resistor is recommended.

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12.1.2 Attribute memory address space

The attribute memory is mapped onto the WMAC internal RAM. The available address range is 0–3FFh, of which only the even bytes are defined. It also contains the COR register at address 3E0h. For details, refer to the "Functional Specification for Hermes WMAC controller".

12.1.3 I/O address space

The Host interfaces with the WMAC through its I/O register set. The WMAC register set contains 32 registers, 16-bit wide. For details, refer to the "Functional Specification for Hermes WMAC controller".

12.2 JTAG interface

The JTAG interface of the WMAC controller and DSP is combined with the PCMCIA host interface, where the JTAG lines are mapped as follows:

TMS	(card input)	mapped to HA20	(pin 49)
TDI	(card input)	mapped to HA21	(pin 50)
TDO	(card output)	mapped to HA22	(pin 53)
TCK	(card input)	mapped to HA23	(pin 54)
TRST_	(card input)	mapped to HSPKR_	(pin 62) through an inverter.

The JTAG interface shall be in reset state and TDO shall be in tri-state if TRST_ is low or HSPKR_ is high. HSPKR_ shall be pulled up in the NIC.

The HSPKR_ line is normally a card output. For the NIC, it is the active high JTAG Test Reset input, internally pulled up, to be used in a special test environment only.

12.3 DSP serial test interface

A three-bit serial test interface of the DSP is mapped onto the following PCMCIA bus lines:

ENGTEST	(card input)	mapped to HIOIS16_	(pin 33)
EDD0	(card output)	mapped to HA17	(pin 46)
ETD1	(card output)	mapped to HA18	(pin 47)
ETD2	(card output)	mapped to HA19	(pin 48)
ETSYN	(card output)	mapped to HA24	(pin 55)
ETSCK	(card output)	mapped to HA25	(pin 56)

The test interface shall be enabled only if ENGTEST is high. The test interface outputs shall be in tri-state if ENGTEST is low. ENGTEST ot HIOIS16_ shall be pulled down in the NIC.

The HIOIS16_ line is normally a card output. For the NIC it is also the DSP test bus enable line, internally pulled down, to be used in a special test environment only.

12.4 External antenna connection

The external antenna connector is located at the backside of the Network Interface Card, which is the edge opposite to the PCMCIA connector.

The external antenna connector is a single coax connector that carries the RF transmit and receive signal as well as the antenna select signal. The antenna select signal is a bias voltage that has 3.3V CMOS levels; high for selecting the transmit/receive antenna and low for selecting the second receive antenna. The coax connection is mechanically unique, such that no off-the-shelf connector will fit (FCC requirement).

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In the case of an external active antenna with RF power booster, the DSP is set such that the antenna select signal has the following levels:

High (Vcc=3.3V nominal):	transmit mode.
Medium (Vcc/2=1.65V nominal):	receive mode using the RX/TX antenna.
Low (0V nominal):	receive mode using second RX antenna.

12.5 Human interface

The Network Interface Card contains two LED's, one for power -up and one for activity indication. These LED's are situated on the backside of the Network Interface Card.

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13 FUNCTIONAL DESCRIPTION

13.1 Medium Access and Data Protocol

Refer to the Functional Specification for Hermes WMAC controller.

13.2 Physical Layer Convergence Procedure

This section provides a convergence procedure in which MPDUs (MAC Protocol Data Units) are converted to and from PPDUs (PHY Protocol Data Units). During transmission, the MPDU is appended with a PLCP preamble and a PLCP header to create the PPDU. At the receiver, the PLCP preamble and the PLCP header are processed facilitating demodulation and delivery of the MPDU.

Figure 7 shows the PPDU format. The PLCP preamble contains synchronization (Sync) and Start Frame Delimiter (SFD) fields. The PLCP header contains the 802.11 signal (Signal), 802.11 service (Service), MPDU length (Length) and CCITT CRC-16 fields. Each of these fields will be described in detail in the following paragraphs.

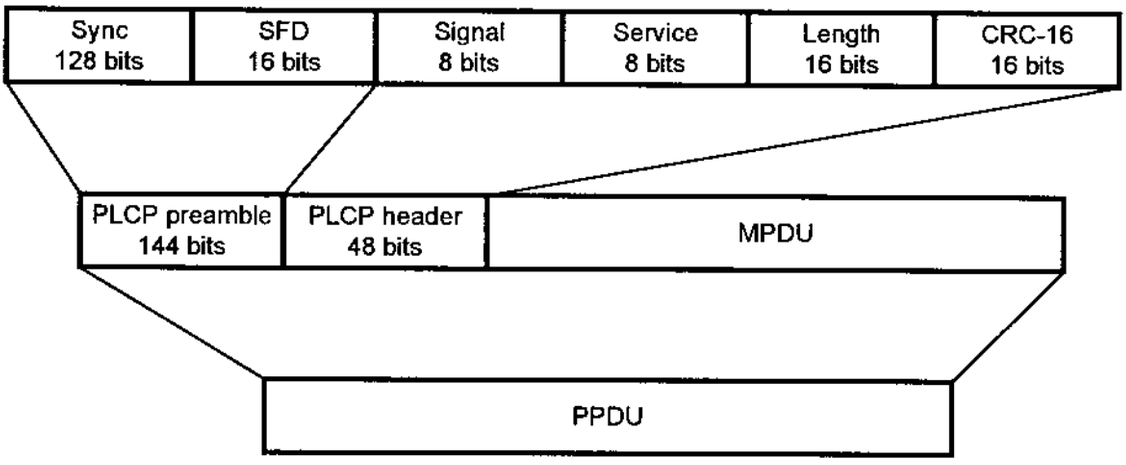

Figure 7. PLCP frame format.

13.2.1 PLCP synchronization

The Sync field consists of 128 1-bits. This field is provided facilitating the necessary operations for synchronization at the receiver. The PLCP preamble and PLCP header fields will not implement the short PLCP preamble and header fiel ds at 11 Mbps and 5.5 Mbps as specified in the 802.11 final adopted specification.

13.2.2 PLCP Start Frame Delimiter

The Start Frame Delimiter is a unique word provided to indicate the start of PHY dependent parameters within the PLCP preamble. Th is unique word consists of a 16 bits field, F3A0h (MSB to LSB), where the LSB is transmitted first in time.

13.2.3 PLCP 802.11 signal field

The 8 bit Signal field indicates the modulation and data rate which will be used for transmission and reception of the MPDU. The data rate is equal to the Signal field value multiplied by 100kbit/s. This Network Interface supports four different bit-rates given by the following 8-bit words, where the LSB is transmitted first in time:

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a) 0Ah (MSB to LSB) 1Mbit/s DBPSK
b) 14h 2Mbit/s DQPSK
c) 37h 5.5Mbit/s CCK
d) 6Eh 11Mbit/s CCK

13.2.4 PLCP 802.11 service field

The 8 bit Service field is reserved for future use. The value of 00h signifies 802.11 compliance. The LSB is transmitted first in time.

13.2.5 PLCP Length field

The PLCP Length field is an unsigned integer which indicates length of the MPDU in microseconds. The LSB is transmitted first in time. The Length field is calculated as follows:

a) 1Mbit/s DBPSK: Length = #bytes * 8.
b) 2Mbit/s DQPSK Length = #bytes * 4.
c) 5.5Mbit/s CCK Length = #bytes * 8 / 5.5, rounded up
d) 11Mbit/s CCK Length = #bytes * 8 / 11, rounded up

At the receiver, the number of bytes in the MPDU frame is calculated as follows:

a) 1Mbit/s DBPSK: #bytes = Length / 8.
b) 2Mbit/s DQPSK #bytes = Length / 4.
e) 5.5Mbit/s CCK #bytes = Length * 5.5 / 8, rounded down
f) 11Mbit/s CCK #bytes = Length * 11 / 8, rounded down

13.2.6 PLCP CRC16 field

The 802.11 signal, 802.11 service and length field is prot ected with a CCITT CRC-16 Frame Check Sequence (FCS). The CRC-16 FCS is the ones complement of the remainder generated by the module 2 division of the protected PLCP fields by the polynomial:

$$x^{16} + x^{12} + x^{5} + 1$$

The protected bits are processed in transmi t order. All FCS calculations are made prior to data scrambling.

The SSFD is a single 0-bit following the 83 1bits in the SYNC field.
This field contains 8 data bits.

13.3 PHY Data Scrambler and Descrambler

The polynomial $1 + x^{-4} + x^{-7}$ is used to scramble the entire PPDU or short ACK. The feedthrough configuration of the scrambler is self initializing. No prior initializing of the scrambler is required for receive processing. The scrambler should be initialized to any state except all ones when transmitting.

13.4 Data modulation and modulation rate change

The PLCP preamble, PLCP header and an entire short ACK are transmitted using 1Mbit/s DBPSK modulation. The 802.11 signal field indicates the modulation and data rate used to transmit the MPDU. The transmitter and receiver initiates the modulation indicated by the 802.11 signal field starting with the first symbol (1 bit for DBPSK, 2bits for DQPSK) of the MPDU.

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13.5 DSSS Spreading Sequence

The following 11 chip Barker sequence is used:

+1, −1, +1, +1, −1, +1, +1, +1, −1, -1, −1

The left most chip is output first in time. The first chip is aligned as the start of a transmitted symbol. The symbol duration is exactly 11 chips long.

13.6 DSSS Modulation and channel data rates

13.6.1 1Mbps DBPSK modulation and 2Mbps DQPSK modulation

Four modulation formats and data rates are specified for the Network Interface. The lowest rate is based on 1Mbit/s DBPSK modulation. The BPSK encoder is specified in Table 3. The 2Mbit/s data rate is based on DQPSK. The DQPSK encoder is specified in Table 4. The initial phase of the (I,Q) vector (the first symbol in the PLCP) will be $\pi/4$.

Bit input	Phase change
0	0
1	π

Table 3. 1Mbit/s DBPSK modulation.

Dibit pattern (b0,b1) b0 is first in time	Phase change
00	0
01	$\pi/2$
11	π
10	$3\pi/2$ $(-\pi/2)$

Table 4. 2Mbit/s DQPSK modulation.

The DSP provides analog baseband signals w here the output voltage is linearly related to these levels.

13.6.2 Modulation for Channel Data Rates of 5.5 and 11 Mbit/s

The extended Direct Sequence specification defines two additional data rates. The modulation scheme for 5.5 Mbit/s and 11 Mbit/s is Complementary Code Keying (CCK).

13.6.2.1 Spreading Codes

The spreading code length is 8 and based on complementary codes. The chipping rate is 11 MHz. The symbol duration shall be exactly 8 complex chips long.
The following formula shall be used to derive the CCK code words that shall be used for spreading both 5.5 and 11 Mbit/s:

$$c = \{e^{j(\varphi_1+\varphi_2+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_4)},$$
$$-e^{j(\varphi_1+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_3)}, e^{j(\varphi_1+\varphi_3)}, -e^{j(\varphi_1+\varphi_2)}, e^{j\varphi_1}\}$$

This formula creates 8 complex chips (LSB to MSB) that are transmitted LSB first.

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This is a form of the generalized Hadamard transform enc oding where φ_1 is added to all code chips, φ_2 is added to all odd chips, φ_3 is added to all odd pairs of chips and φ_4 is added to all odd quads of code chips.
The phases $\varphi 1_i$ (i=1..4) modify the phase of all chips of the sequence and will be DQPSK encoded for 5.5 and 11 Mbit/s. This will take the form of rotating the whole symbol by the appropriate amount relative to the phase of the preceding symbol. Note that the MSB chip of the symbol defined above is the chip that indicates the symbol's phase and it is transmitted last.

13.6.2.2 Cover codes

The 4th and 7th chips are rotated 180 degrees by a cover sequence to optimize the sequence correlation properties. This can be seen by the minus sign on the 4 th and 7th terms in the equation in clause 12.6.2.1.

13.6.2.3 Bias suppression

All odd numbered symbols of the MPDU shall be given an extra 180 degree (π) rotation in addition to the DQPSK modulation. This is to prevent a DC bias in the modulation in the event that the scrambler hangs up on all '0s' or all '1s' packets. This shall apply to both the 5.5 and 11 Mbit/s modes. The symbols of the MPDU shall be numbered starting with "0" for the first symbol for the purposes of determining odd and even symbols. That is, the MPDU starts on an even numbered symbol. The phase shift for the symbol following the 'flipped' symbol shall depend on the 'flipped' phase, that is, the phase shifts shall be cumulative. To illustrate this behavior, consider the following example of the net carrier phases starting at the first symbol following an odd symbol which was at 0 phase:
for an all '0s' packet: 0 π π 0 0 π π 0 0 π π 0 0.....
for an all '1s' packet: π π 0 0 π π 0 0 π π 0 0 π .....
For this example we assume that the scrambler is hung and the data is as shown.

13.6.2.4 5.5 Mbit/s modulation

At 5.5 Mbit/s 4 bits (d0 to d3; d0 first in time) are transmitted per symbol..
The data bits d0 and d1 encode φ_1 based on DQPSK. The DQPSK encoder is specifie d in Table 5 (In the tables, +jω shall be defined as counterclockwise rotation.). The phase change for φ_1 is relative to the phase φ_1 of the preceding symbol. For the case of the preamble to header transition, the phase change fo r φ_1 is relative to the phase of the preceding DBPSK (1 Mbit/s) symbol. See the definition in clause 12.6.1 for the reference phase of this Barker symbol. A "+1" in the Barker code shall represent the same carrier phase as a "+1" in the CCK code. All odd numbered symbols of the MPDU shall be given an extra 180 degree (π/2) rotation in addition to the DQPSK modulation.

Dibit pattern (d(I0),d(1)) d(0) is first in time	**Phase Change (+jω)**
00	0
01	π/2
11	π
10	3π/2 (-π/2)

Table 5. DQPSK Encoding Table

The data dibits d2, and d3 CCK encode the basic symbol as specified in Table 6. This table is derived from the formula above by setting φ_2 = (d2*π)+ π /2, φ_3 = 0, and φ_4 = d3*π. In the table d2 and d3 are in the order shown and the complex chips are shown LSB to MSB (left to right) with LSB transmitted first.

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d2, d3									
00	:	$1j$	1	$1j$	-1	$1j$	1	$-1j$	1
01	:	$-1j$	-1	$-1j$	1	$1j$	1	$-1j$	1
10	:	$-1j$	1	$-1j$	-1	$-1j$	1	$1j$	1
11	:	$1j$	-1	$1j$	1	$-1j$	1	$1j$	1

Table 6. 5.5 Mbit/s CCK Encoding Table

13.6.2.5 11 Mbit/s modulation

At 11 Mbit/s, 8 bits (d0 to d7; d0 first in time) are transmitted per symbol.
The first dibit (d0,d1) encodes φ_1 based on DQPSK. The DQPSK encoder is specified in Table 5 above. The phase change for φ_1 is relative to the phase φ_1 of the preceding symbol. In the case of rate change, the phase change for φ_1 is relative to the phase φ_1 of the preceding CCK symbol or relative to the phase of the preceding DBPSK symbol. See the definition in clause 12.6.1 for the reference phase of the Barker sym bols used at 1 Mbit/s. A "+1" in the Barker code shall represent the same carrier phase as a "+1" in the CCK code. All odd numbered symbols of the MPDU shall be given an extra 180 degree ($\pi/2$) rotation in addition to the DQPSK modulation. Symbol numberin g starts with "0" for the first symbol of the MPDU.
The data dibits: (d2,d3), (d4,d5), (d6,d7) encode φ_2, φ_3, and φ_4 respectively based on QPSK as specified in Table 7. Note that this table is binary, not Grey, coded.

Dibit pattern (d(i),d(i+1)) d(i) is first in time	**Phase**
00	0
01	$\pi/2$
10	π
11	$3\pi/2$ $(-\pi/2)$

Table 7. QPSK Encoding Table.

13.7 RF channel frequencies

The Network Interface in the 2.4-2.5GHz ISM band uses the channel ce nter frequencies as defined by the IEEE802.11 PHY standard for DSSS. These channel frequencies and the countries of application are listed in Table 8.

Channel ID	FCC Channel Frequencies (MHz)	ETS Channel Frequencies (MHz)	Japan Channel Frequencies (MHz)	France Channel Frequencies (MHz)
1	2412	2412	-	-
2	2417	2417	-	-
3	2422	2422	-	-
4	2427	2427	-	-
5	2432	2432	-	-
6	2437	2437	-	-
7	2442	2442	-	-
8	2447	2447	-	-

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9	2452	2452	-	-
10	2457	2457	-	2457
11	2462	2462	-	2462
12	-	2467		2467
13	-	2472		2472
14	-	-	2484	-

Table 8. IEEE802.11 channel frequencies.

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13.8 Diagnostics and test provisions

The WMAC has self diagnostics provisions, such that its functionality can be verified through the Host bus.

The WMAC and DSP contain test provisions, such that the DSP functionality can be verified through the Host bus.

The WMAC and DSP contain test provisions that enable direct control of the RF section through the Host bus. This direct control is for test purposes only and shall not be used during normal operation.

The WMAC and DSP contain provisions to generate the following test signals on its In-phase and Quadrature baseband outputs in transmit mode, to be controlled through the Host bus:

1. I-out at high level / Q-out at low level and I-out at low level / Q-out at high level respectively resulting in a constant carrier at the RF output.
2. I-out and Q-out produce square wave signals with +90° and –90° phase difference, resulting in a SSB modulated carrier (USB and LSB) at the RF output. The frequency is fixed between 1MHz and 2MHz.
3. Continuous spreaded and scrambled data output, either DBPSK or QPSK.

The WMAC and DSP contain provisions to measure the receiver quadrature alignment and obtain the results through the Host bus. To do this, a constant carrier RF with frequency offset between 1MHz and 2MHz has to be injected at the receiver input.

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14 RASUI

The MTBF is 125,000 hours based on a workload of 2040 hours/year. This assumes the card does not exceed its ambient temperature ceiling of 60°C.

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