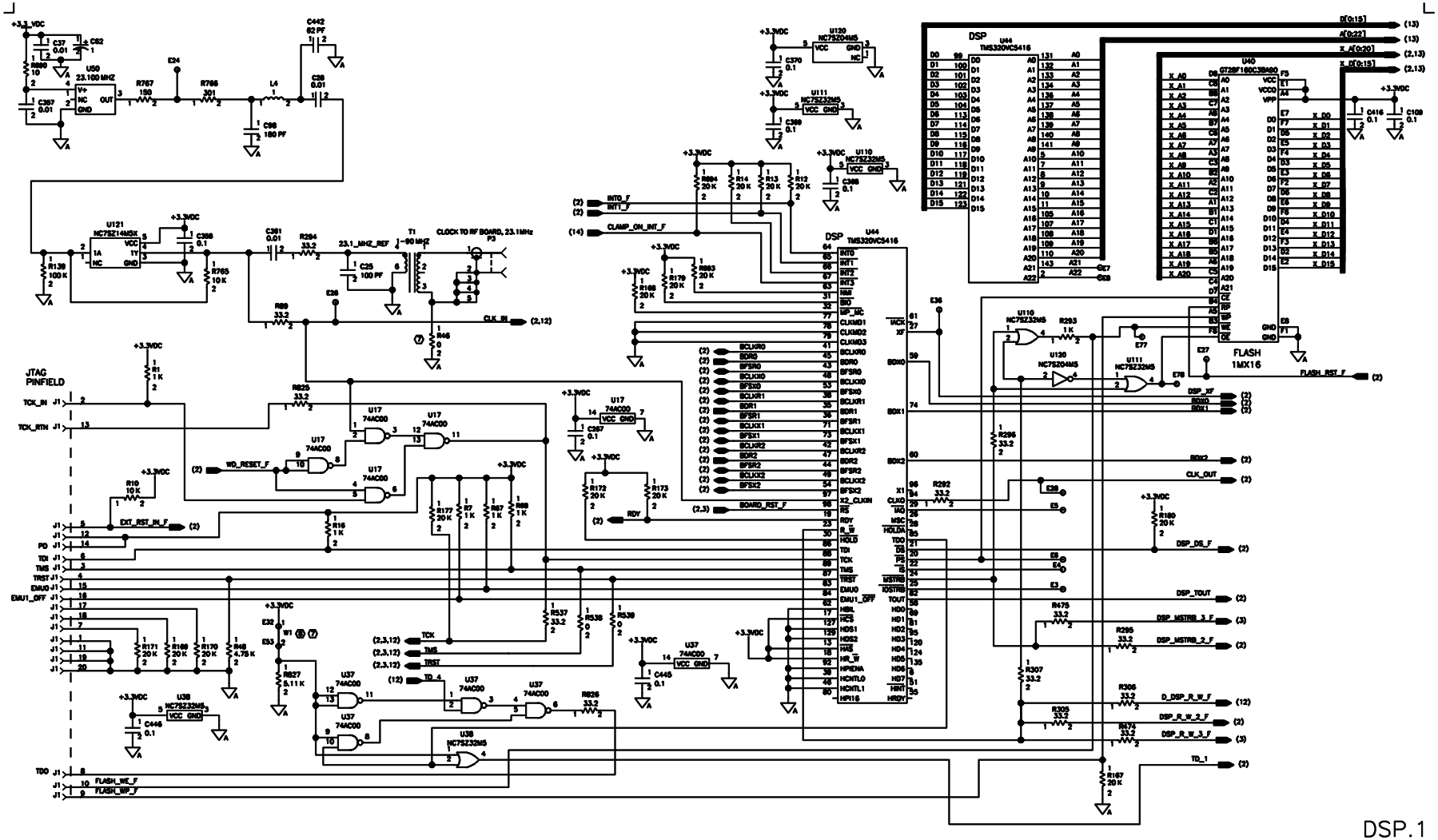
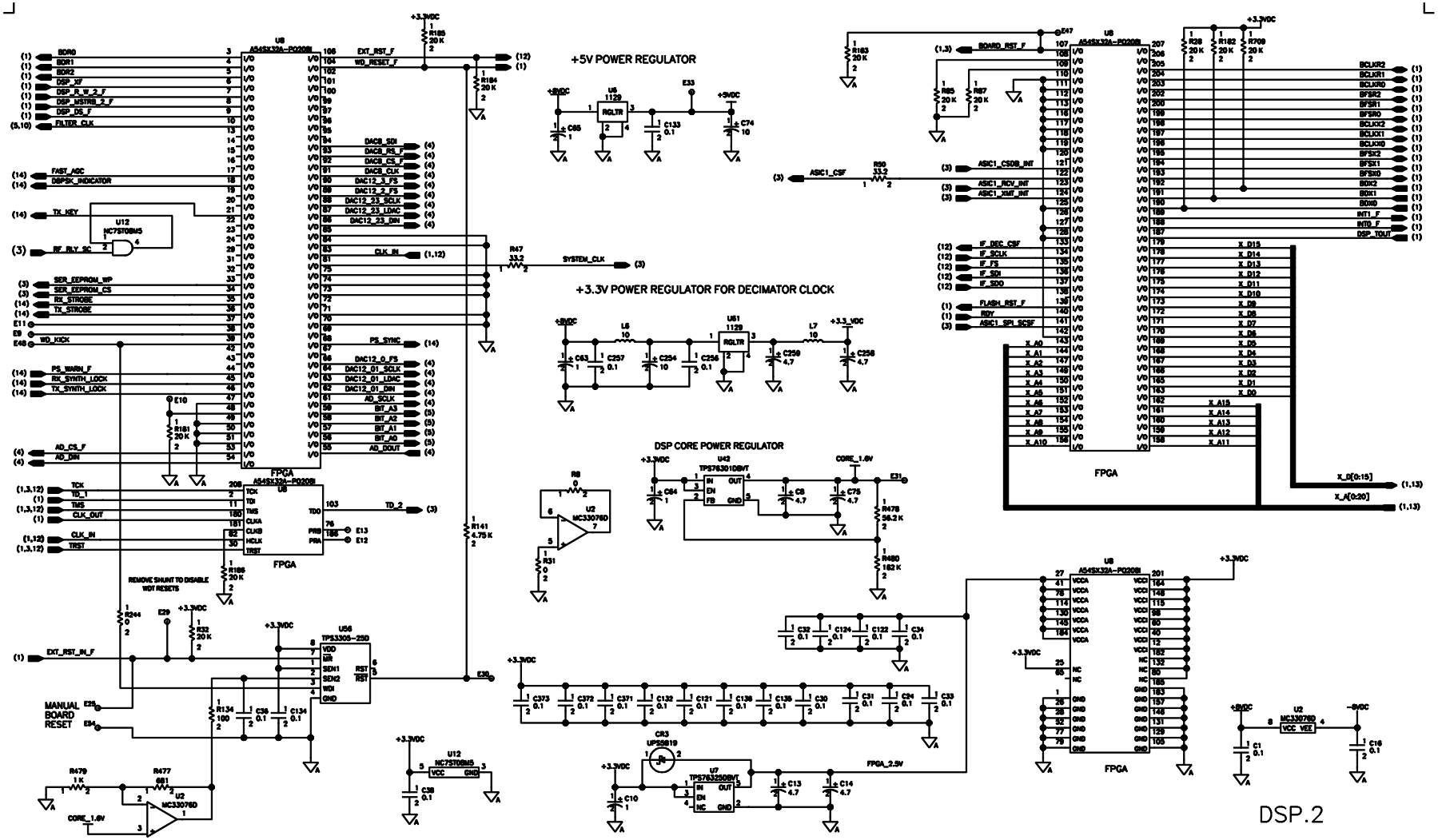
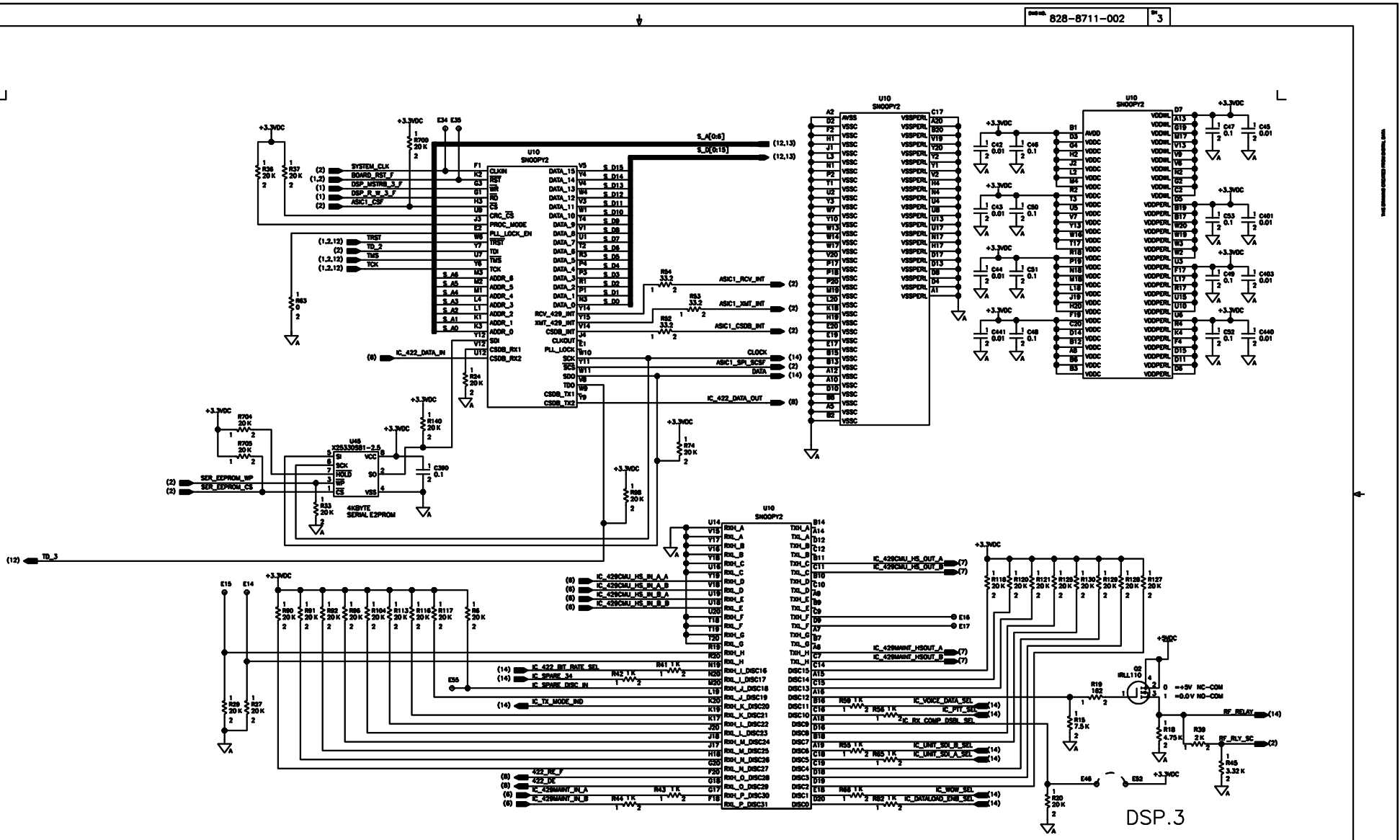
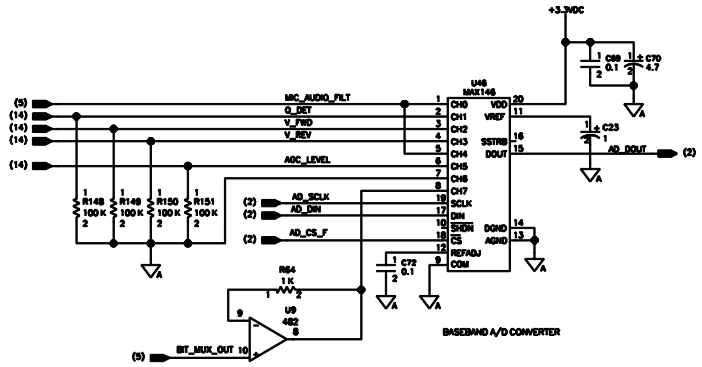
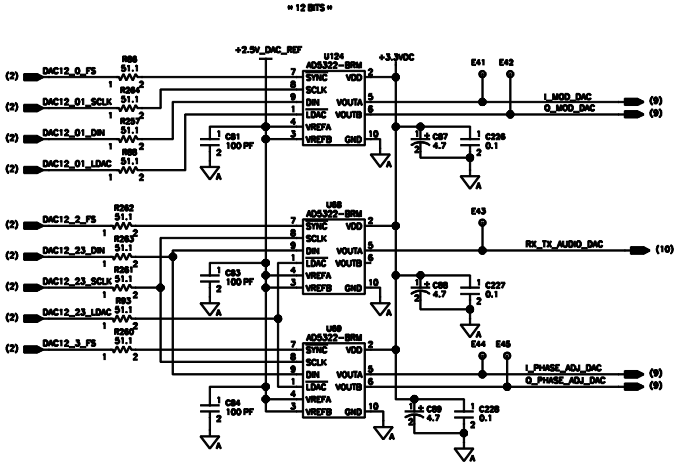
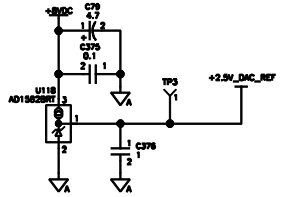

DSP
FLASH 1MX16
JTAG PINFIELD
ROCKWELL COLLINS, INC
400 COLLINS RD. NE CEDAR RAPIDS, IA 52498
SCHEMATIC DIAGRAM, DSP
828-8711-002
DSP.1
ROCKWELL COLLINS PROPRIETARY INFORMATION.
THIS DRAWING IS CREATED FROM DIGITAL DATA
Plotted 09/06/01 15:57


+5V POWER REGULATOR
+3.3V POWER REGULATOR FOR DECIMATOR CLOCK
DSP CORE POWER REGULATOR
FPGA
REMOVE SHUNT TO DISABLE WDT RESETS
MANUAL BOARD RESET
DSP.2

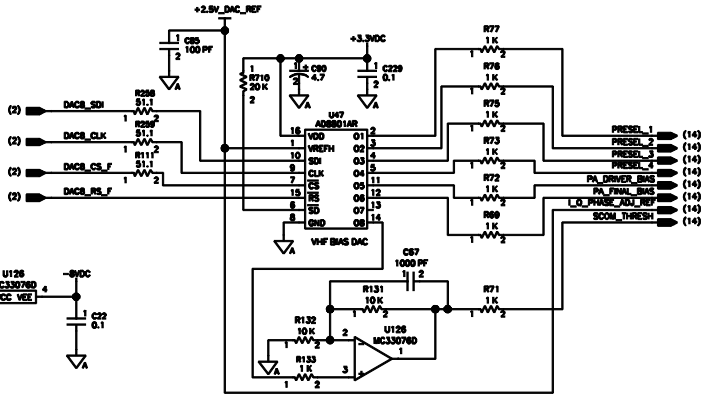

828-8711-002
3
U10
SNOOPY2
+3.3VDC
SYSTEM_CLK
BOARD_RST_F
DSP_MSTRB_3_F
DSP_R_W_3_F
ASIC1_CSF
TRST
TD_2
TMS
TCK
S_A[0:8]
S_D[0:15]
ASIC1_RCV_INT
ASIC1_XMT_INT
ASIC1_CSDB_INT
IC_422_DATA_IN
IC_422_DATA_OUT
CLOCK
DATA
U45
X25330S8I-2.5
4KBYTE
SERIAL E2PROM
SER_EEPROM_WP
SER_EEPROM_CS
TD_3
IC_429CMU_HS_IN_A_A
IC_429CMU_HS_IN_A_B
IC_429CMU_HS_IN_B_A
IC_429CMU_HS_IN_B_B
IC_429CMU_HS_OUT_A
IC_429CMU_HS_OUT_B
IC_429MAINT_HSOUT_A
IC_429MAINT_HSOUT_B
IC_422_BIT_RATE_SEL
IC_SPARE_34
IC_SPARE_DISC_IN
IC_TX_MODE_IND
422_RE_F
422_DE
IC_429MAINT_IN_A
IC_429MAINT_IN_B
IC_VOICE_DATA_SEL
IC_PTT_SEL
IC_RX_COMP_DSBL_SEL
IC_UNIT_SDI_B_SEL
IC_UNIT_SDI_A_SEL
IC_WOW_SEL
IC_DATALOAD_ENB_SEL
IRLL110
=+5V NC-COM
=0.0V NO-COM
RF_RELAY
RF_RLY_SC
DSP.3
THIS DRAWING IS CREATED FROM DIGITAL DATA
ROCKWELL COLLINS
PROPRIETARY INFORMATION.
D
4V792
828-8711-002
NONE
SHEET 3
design.3
Plotted 09/06/01 15:57

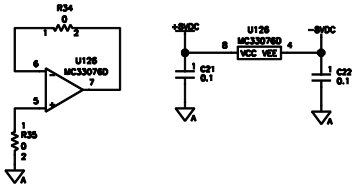






2.5V Reference





DSP.4

THIS DRAWING IS CREATED FROM DIGITAL DATA

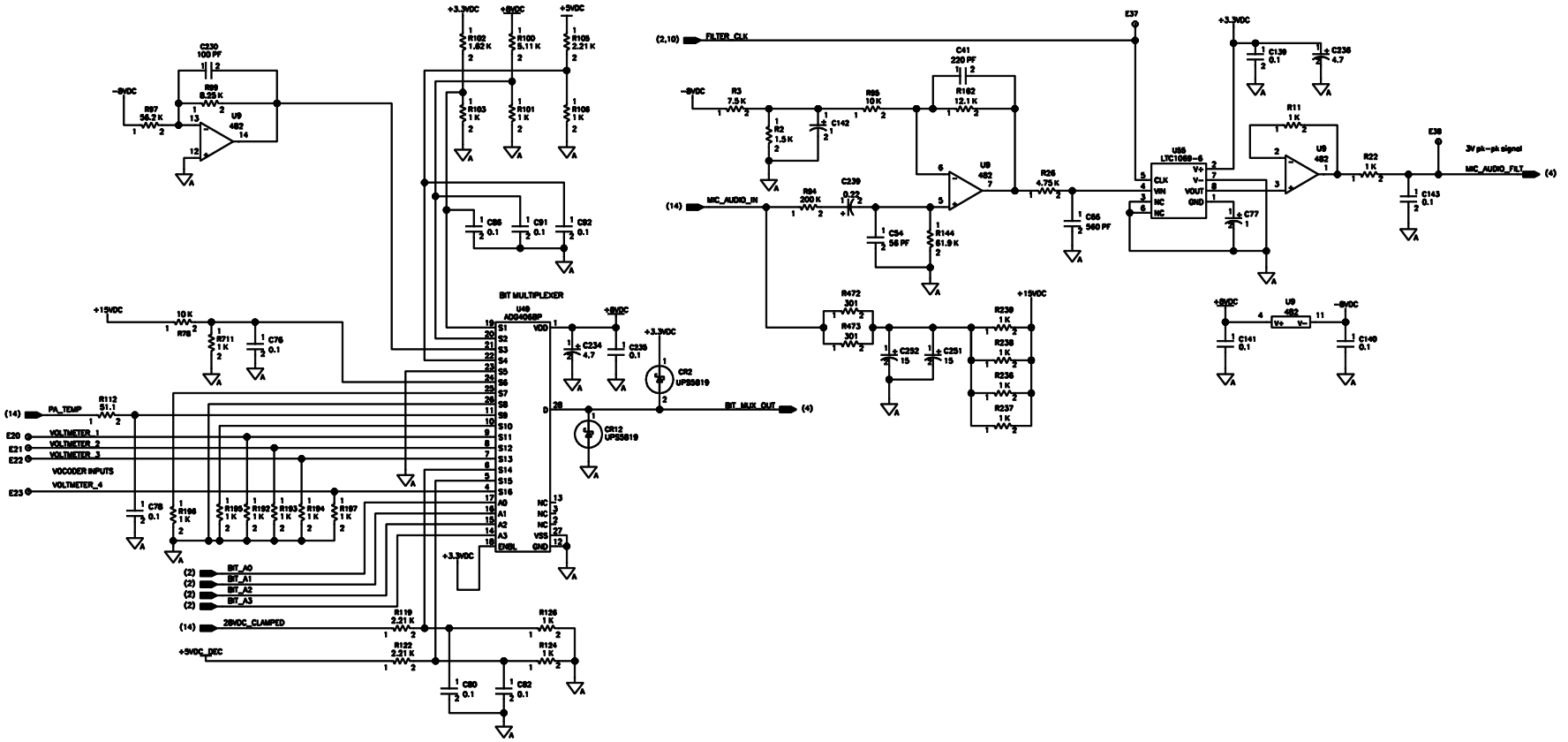
ROCKWELL COLLINS
PROPRIETARY INFORMATION.

SIZE	CAGE CODE	DWG NO.	REV LTR
D	4V792	828-8711-002	-
SCALE	NONE		SHEET 4

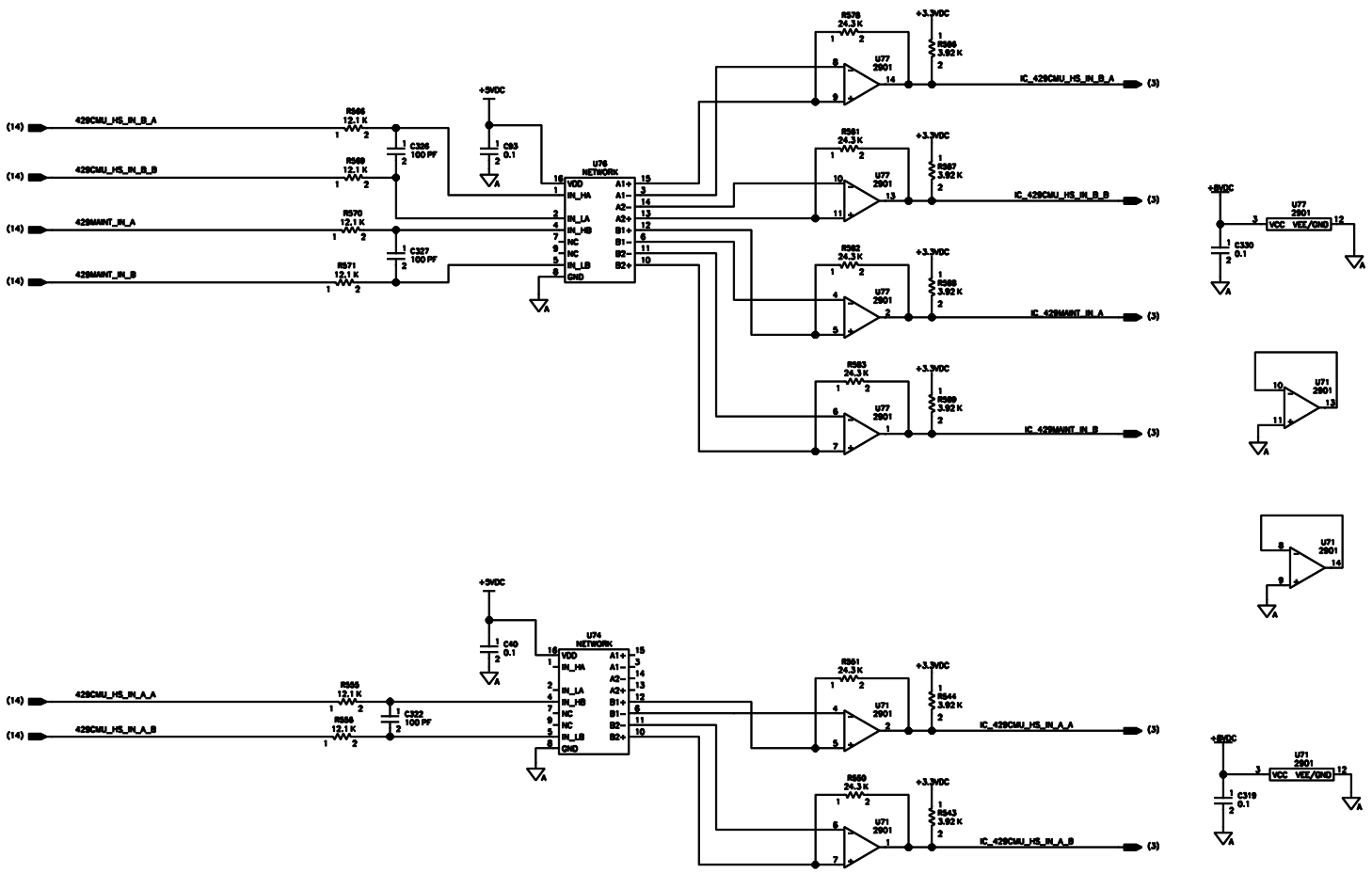
design.4

Plotted 09/06/01 15:57

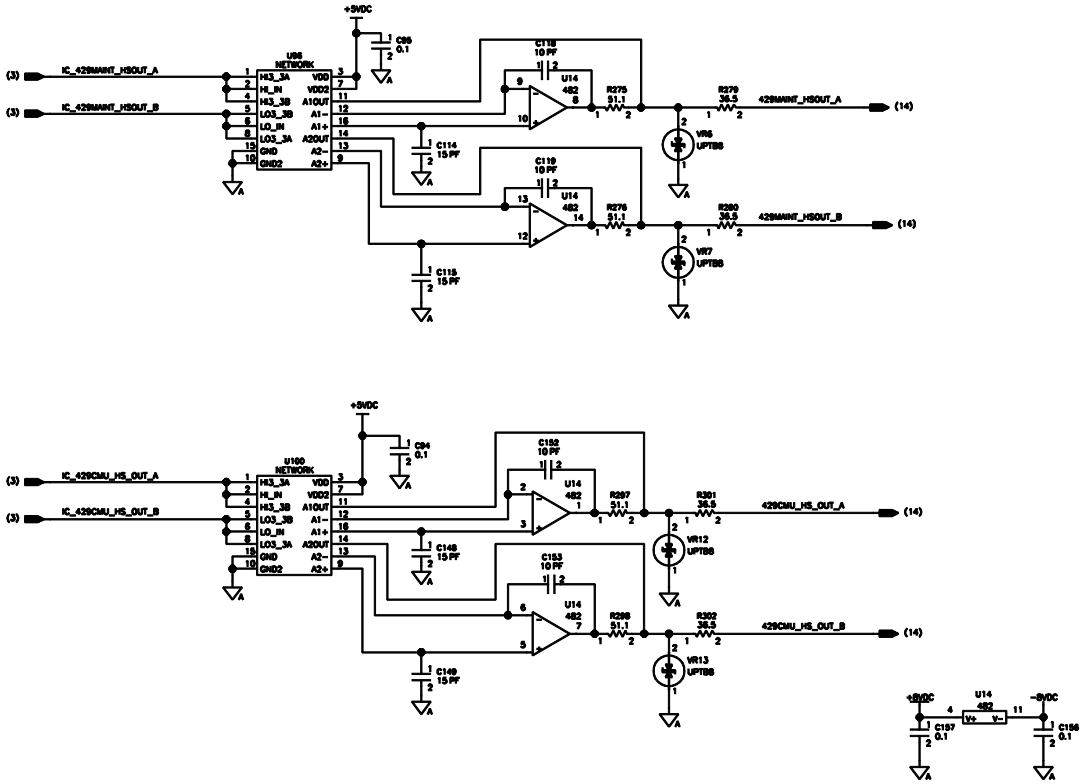
DIGITAL DATA ONLY NO MASTER PRINTING


BIT MULTIPLEXER
U49
AD9408BP
FILTER_CLK
MIC_AUDIO_IN
MIC_AUDIO_FILT
3V pk-pk signal
BIT_MUX_OUT
PA_TEMP
VOLTMETER_1
VOLTMETER_2
VOLTMETER_3
VOCODER INPUTS
VOLTMETER_4
BIT_A0
BIT_A1
BIT_A2
BIT_A3
28VDC_CLAMPED
+5VDC_DEC
LTC1068-6
CR2 UPS819
CR12 UPS819

DSP.5

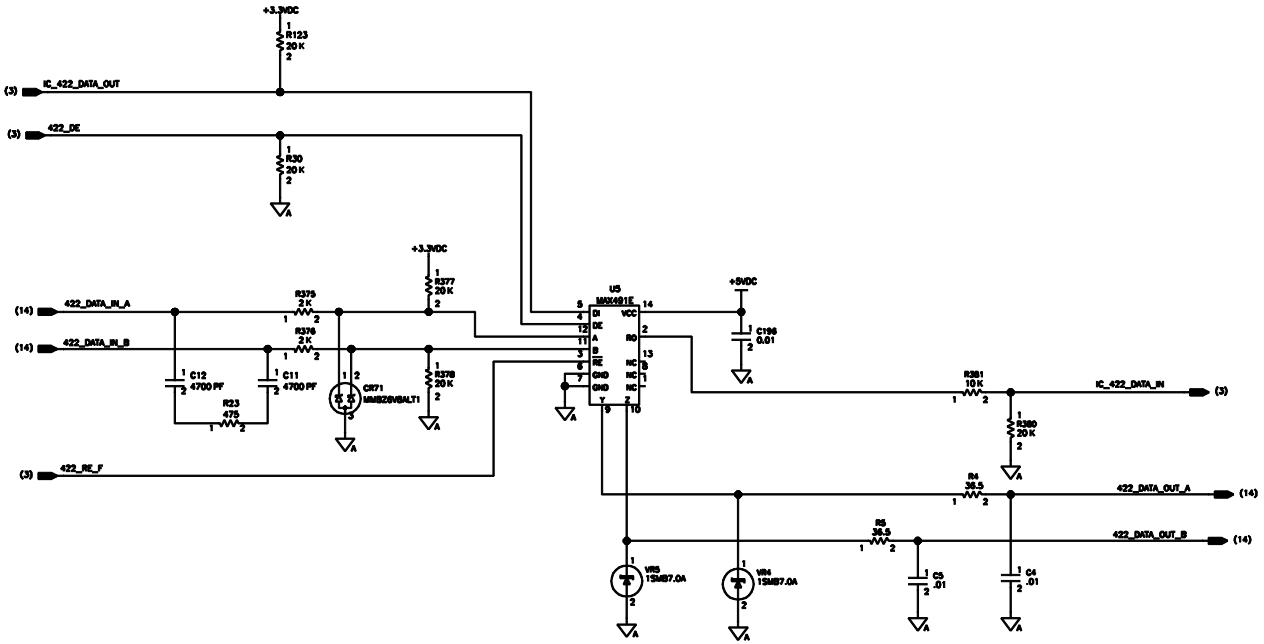

(14) 429CMU_HS_IN_B_A
(14) 429CMU_HS_IN_B_B
(14) 429MAINT_IN_A
(14) 429MAINT_IN_B
R568 12.1 K
R569 12.1 K
R570 12.1 K
R571 12.1 K
C326 100 PF
C327 100 PF
C83 0.1
+5VDC
U76 NETWORK
VDD
IN_HA
IN_LA
IN_HB
NC
NC
IN_LB
GND
A1+
A1-
A2-
A2+
B1+
B1-
B2-
B2+
R578 24.3 K
R581 24.3 K
R582 24.3 K
R583 24.3 K
R586 3.92 K
R587 3.92 K
R588 3.92 K
R589 3.92 K
+3.3VDC
U77 2901
IC_429CMU_HS_IN_B_A
IC_429CMU_HS_IN_B_B
IC_429MAINT_IN_A
IC_429MAINT_IN_B
(3)
C330 0.1
U77 2901 VCC VEE/GND
U71 2901
(14) 429CMU_HS_IN_A_A
(14) 429CMU_HS_IN_A_B
R555 12.1 K
R556 12.1 K
C322 100 PF
C40 0.1
U74 NETWORK
R561 24.3 K
R560 24.3 K
R544 3.92 K
R543 3.92 K
IC_429CMU_HS_IN_A_A
IC_429CMU_HS_IN_A_B
C319 0.1

DSP.6



429 TRANSMITTERS

DSP.7



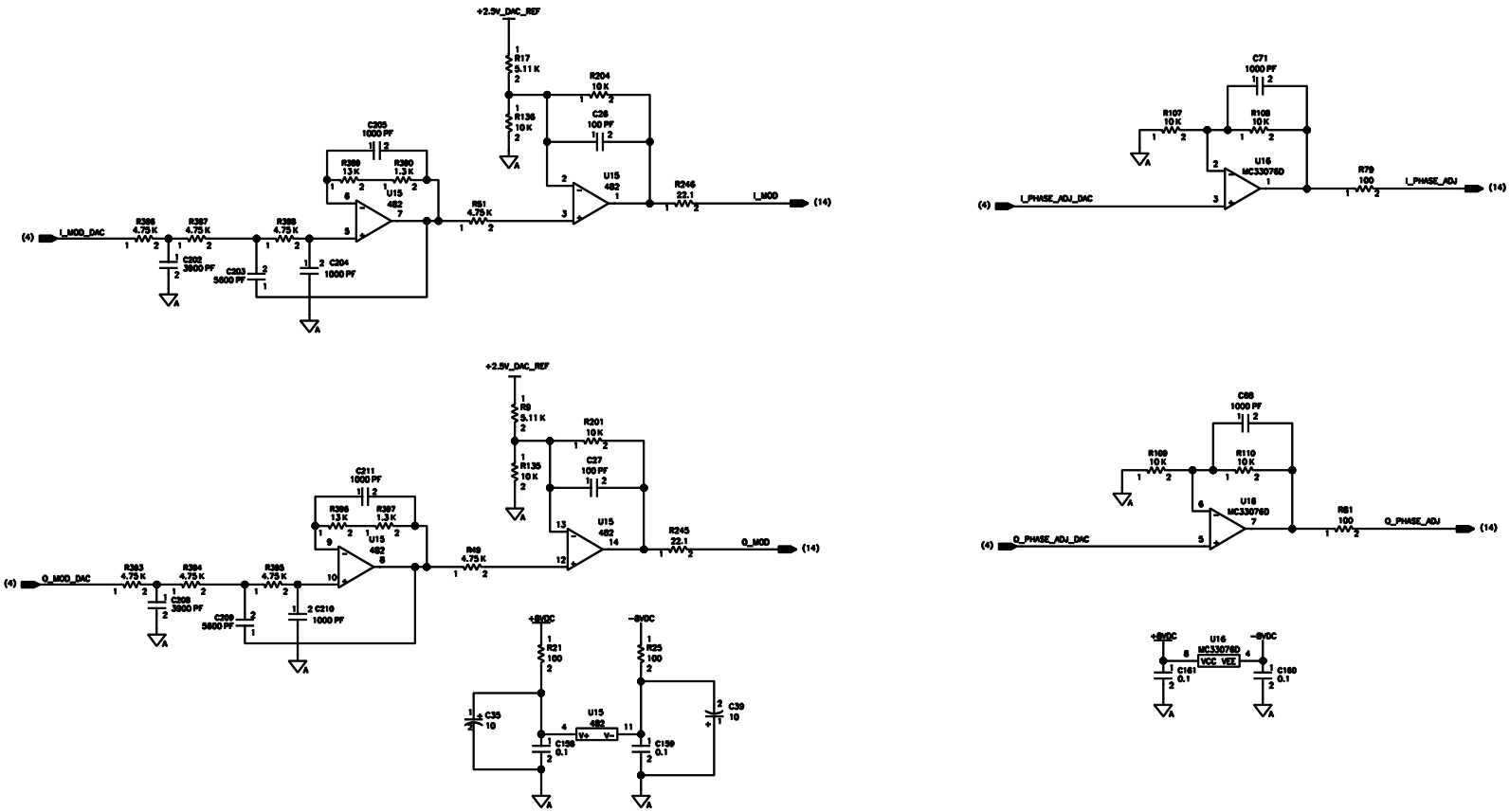
422 TRANSCEIVERS

DSP.8

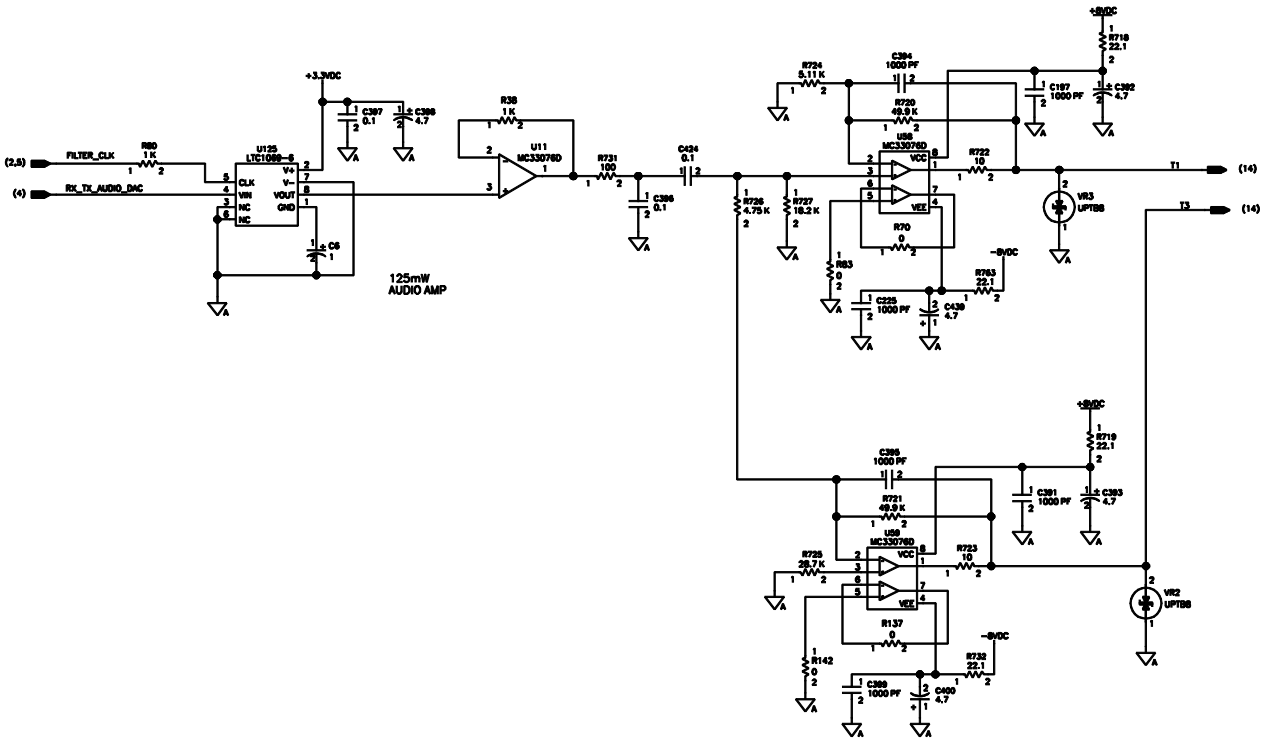
design.8

Plotted 09/06/01 15:57

SIZE	CAGE CODE	DWG NO.	REV LTR
D	4V792	828-8711-002	-
SCALE NONE		SHEET 8	


+2.5V_DAC_REF
R17 5.11 K
R136 10 K
R204 10 K
C28 100 PF
C205 1000 PF
R389 13 K
R390 1.3 K
U15 482
R51 4.75 K
R246 22.1
I_MOD
(14)
(4)
I_MOD_DAC
R386 4.75 K
R387 4.75 K
R388 4.75 K
C202 3900 PF
C203 5600 PF
C204 1000 PF
C71 1000 PF
R107 10 K
R108 10 K
U16 MC33076D
R79 100
I_PHASE_ADJ
(14)
(4)
I_PHASE_ADJ_DAC
+2.5V_DAC_REF
R9 5.11 K
R135 10 K
R201 10 K
C27 100 PF
C211 1000 PF
R396 13 K
R397 1.3 K
U15 482
R49 4.75 K
R245 22.1
Q_MOD
(14)
(4)
Q_MOD_DAC
R383 4.75 K
R384 4.75 K
R385 4.75 K
C208 3900 PF
C209 5600 PF
C210 1000 PF
C85 1000 PF
R109 10 K
R110 10 K
U16 MC33076D
R81 100
Q_PHASE_ADJ
(14)
(4)
Q_PHASE_ADJ_DAC
+8VDC
-8VDC
R21 100
R25 100
C35 10
C39 10
U15 482
C158 0.1
C159 0.1
U16 MC33076D
VCC VEE
C161 0.1
C160 0.1

DSP.9



DSP.10

THIS DRAWING IS CREATED FROM DIGITAL DATA

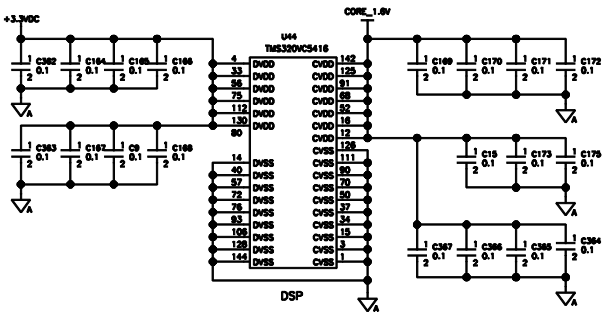
design.10

Plotted 09/06/01 15:57

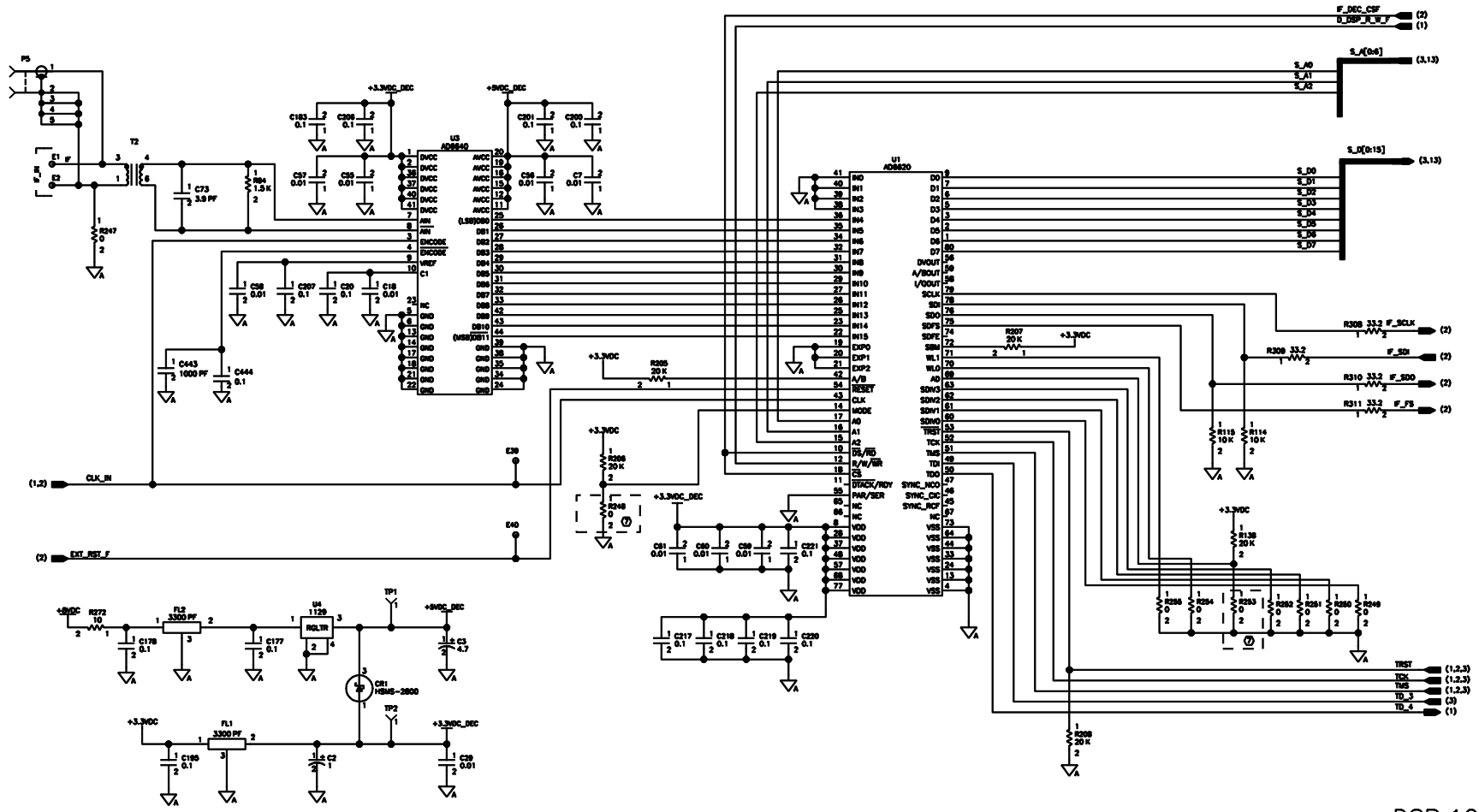
DIGITAL DATA ONLY NO MASTER PRINTING

ROCKWELL COLLINS
PROPRIETARY INFORMATION.

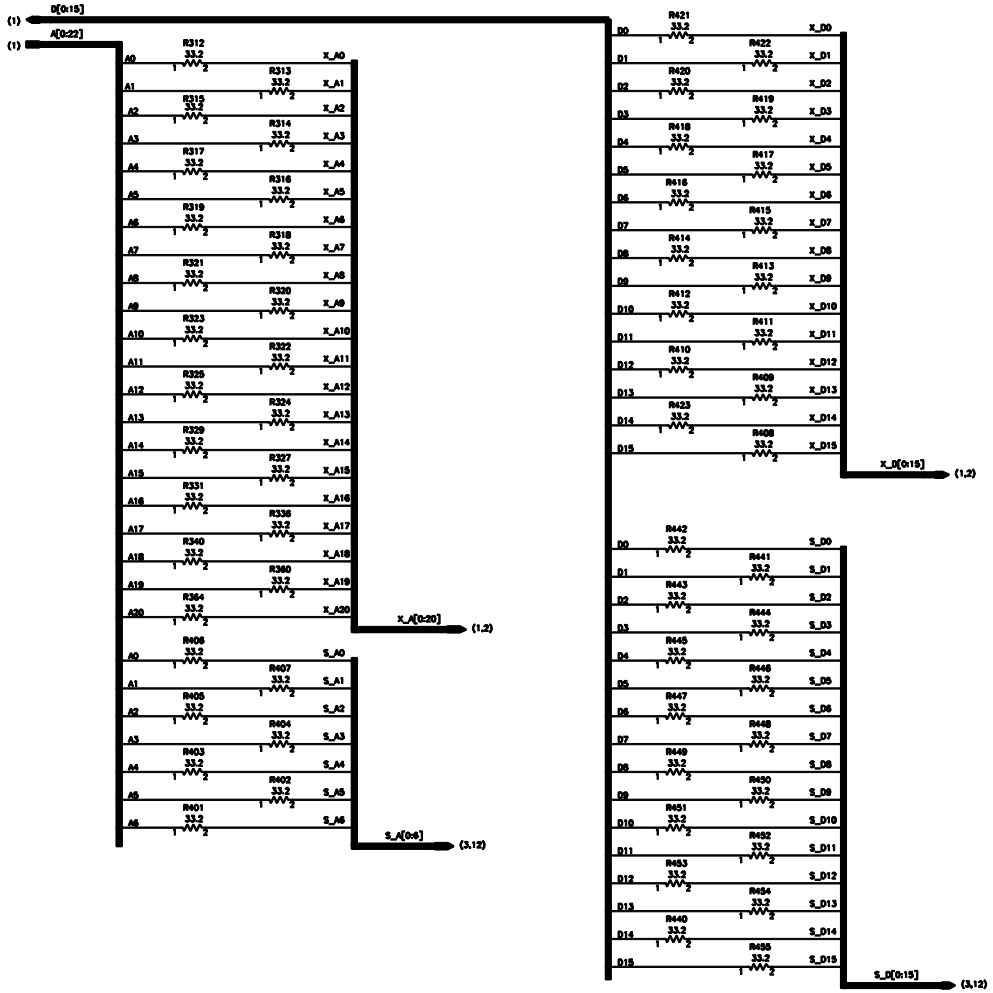
SIZE	CAGE CODE	DWG NO.	REV LTR
D	4V792	828-8711-002	-
SCALE NONE			SHEET 10


+3.3VDC
CORE_1.8V
U44
TMS320VC5416
DVDD
DVSS
CVDD
CVSS
C362
C164
C166
C168
C363
C167
C9
C169
C170
C171
C172
C15
C173
C175
C367
C366
C365
C364
DSP

DSP.11


P5
T2
U3
AD6640
U1
AD9620
+3.3VDC_DEC
+5VDC_DEC
+3.3VDC
CLK_IN
EXT_RST_F
F_DEC_CSF
D_DSP_R_W_F
S_A[0:6]
S_D[0:15]
IF_SCLK
IF_SDI
IF_SDO
IF_FS
TRST
TCK
TMS
TD_3
TD_4
FL2
3300 PF
FL1
3300 PF
U4
1129
RGLTR
CR1
HSMS-2800
TP1
TP2

DSP.12



X_A and X_D connect to the FLASH address and Data bus

X_A and X_D connect to the FPGA address and Data bus

S_A and S_D connect to the Snoopy ASIC address and Data bus

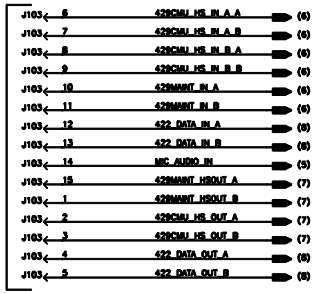
S_A and S_D connect to the Decimator address and Data bus

DSP.13

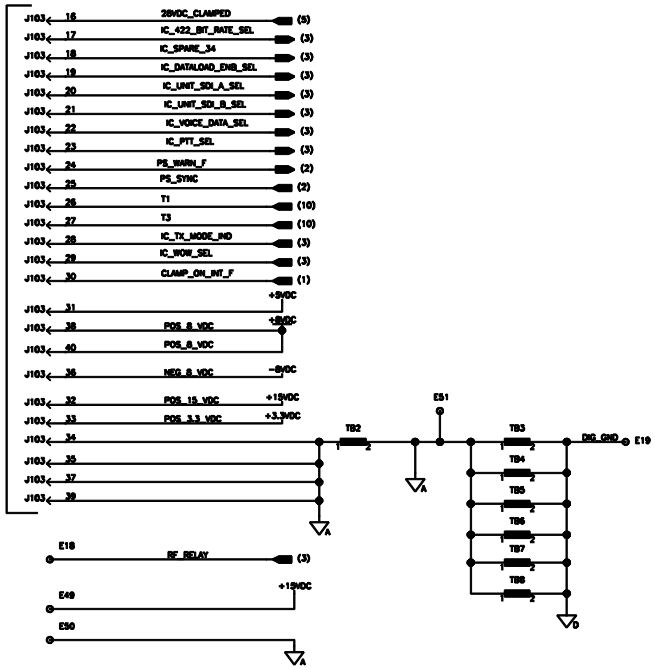
SIZE	CAGE CODE	DWG NO.	REV LTR
D	4V792	828-8711-002	-
SCALE	NONE		SHEET 13

A2J103 CONNECTS THROUGH
A3 INTERCONNECT

TO A3J1
OF INTERCONNECT
(EXT CONNECTOR)

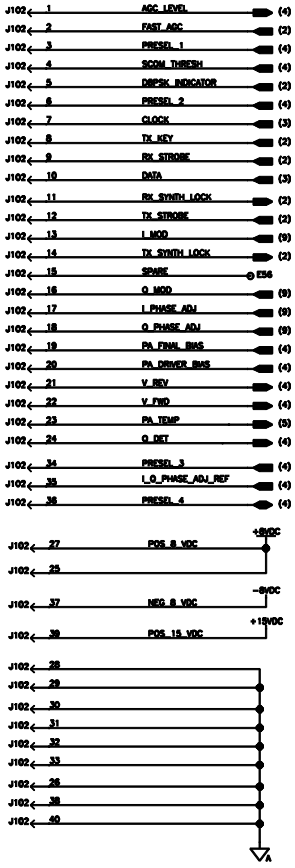


THROUGH A3 INTERCONNECT
TO A4J104 OF PS



Hard Wire to RF Relay

A2J102 CONNECTS THROUGH A5
TO A1J101



DSP.14