Exhibit 2 – Technical Report

2.1 Name and Address (Section 2.1033 (c) (1))

The name and address of the manufacturer of the SRT-2000 Satellite Communications System and applicant for certification is Rockwell Collins, Inc., 1300 Wilson Boulevard, Suite 200, Arlington, Virginia 22209.

2.2 FCC Identifier (Section 2.1033 (c) (2))

FCC ID **AJK8221349** is the FCC ID for all part numbers of the SRT-2000 with configurations of 1-6 channel modules.

2.3 Installation and Operation Manuals (Section 2.1033 (c) (3))

See **Exhibit 3**.

2.4 Type or Types of Emission (Section 2.1033 (c) (4))

The following table shows the measured bandwidths for each of the data rates supported by the SRT-2000. Each measured bandwith falls within the 25 kHz bandwidth limit specified in Section 87.137(a) for 21K0G1D, 21K0G1E, and 21K0G1W transmission. This data was obtained while transmitting at the maximum output power of 25 watts.

Data Rate (BPS)	Low-Band (1626.5 MHz) BW (kHz)	Mid-Band (1643.5 MHz) BW (kHz)	High-Band (1660.5 MHz) BW (kHz)
600	1.125	1.125	1.125
1200	1.750	1.625	1.875
8400	5.375	5.375	5.375
10500	6.625	6.625	6.625
21000	16.500	16.250	16.250

2.5 Frequency Range (Section 2.1033 (c) (5))

The SRT-2000 frequency range is 1626.5 MHz to 1660.5 MHz when in transmit mode and 1530.0 MHz to 1559.0 MHz when in receive mode.

2.6 Range of Operating Power Values (Section 2.1033 (c) (6))

The SRT-2000 maximum transmitter output power for all transmit channels is 25 Watts / 14 dBW / 44 dBm. The output power level of each module in the transmit mode is individually controlled. The transmit output power adjustment range of each module is from 0 dB to –15dB.

2.7 Maximum Power Rating as Defined in Part 87

According to Section 87.131, UHF aircraft earth stations with emission designators G1D, G1E and G1W can have a maximum of 60 watts per carrier. The SRT-2000 provides a maximum output power of 25 Watts in multi-channel mode.

2.8 DC Voltages and Currents (Section 2.1033 (c) (8))

DC Supply Voltage	Maximum DC Supply Current	Typical Measured DC Supply Current
+25 VDC	4.80 Amps	4.65 Amps
+15 VDC	0.45 Amps	0.34 Amps
-15 VDC	0.15 Amps	0.08 Amps
+5 VDC	0.015 Amps	.007 Amps

2.9 Tune Up Procedures (Section 2.1033 (c) (9))

See **Exhibit 4**.

2.10 Schematics and Circuit Diagrams (Section 2.1033 (c) (10))

See **Exhibit 5**.

2.11 Nameplate Label Drawings (Section 2.1033 (c) (11))

See **Exhibit 6**.

2.12 Equipment Photographs: External Views (Section 2.1033 (c) (12))

See **Exhibit 7**.

2.13 Equipment Photographs: Internal Views (Section 2.1033 (c) (12))

See **Exhibit 8**.

2.14 Digital Modulation System (Section 2.1033 (c) (13))

The following describes the digital modulation techniques utilized in the SRT-2000 for each data rate per Section 2.1033 (c) (13).

600 BPS
A-BPSK with differential encoding
Square Root 40% Raised Cosine Filter
Input wavetrain formulation: The input binary data stream is first applied to a scrambler with a 15-stage shift register which has a feedback polynomial of $1 + X + X^{15}$. The output of the scrambler is then applied to a convolutional encoder. The generator polynomials are:

$$G1: \ 1 + X^2 + X^3 + X^5 + X^6$$
$$G2: \ 1 + X + X^2 + X^3 + X^6$$

The generated polynomial outputs are combined in a punctuated 1/2 rate before the encoded data stream is applied to an interleaver of block size of 384 bits in 6 columns. The output bit stream of the interleaver is organized into words of 3

blocks of 384 bits each. The 3 blocks of data are preceded by a 4 bit format identifier and a 12 bit superframe counter and is appended with a 32 bit unique word for a total word length of 1200 bits. Four (4) words are subsequently organized into a superframe before it is applied to the modulator. The binary phase shift keying (BPSK) modulator phase shifts a subcarrier by -90 or +90 degrees depending on the input word data bit being a 0 or 1, respectively. The subcarrier signal now contains the information and is upconverted for transmission.

1200 BPS

A-BPSK with differential encoding
Square Root 40% Raised Cosine Filter
Input wavetrain formulation: The input binary data stream is first applied to a scrambler with a 15-stage shift register which has a feedback polynomial of $1 + X + X^{15}$. The output of the scrambler is then applied to a convolutional encoder. The generator polynomials are:

$$G1: \ 1 + X^2 + X^3 + X^5 + X^6$$
$$G2: \ 1 + X + X^2 + X^3 + X^6$$

The generated polynomial outputs are combined in a punctuated 1/2 rate before the encoded data stream is applied to an interleaver of block size of 576 bits in 9 columns. The output bit stream of the interleaver is organized into words of 2 blocks of 576 bits each. The 2 blocks of data are preceded by a 4 bit format identifier and a 12 bit superframe counter and is appended with a 32 bit unique word for a total word length of 1200 bits. Eight (8) words are subsequently organized into a superframe before it is applied to the modulator. The binary phase shift keying (BPSK) modulator phase shifts a subcarrier signal by -90 or +90 degrees depending on the input word data bit being a 0 or 1, respectively. The subcarrier signal now contains the information and is upconverted for transmission.

8400 BPS

Aviation Quadrature Phase Shift Keying (A-QPSK)
Square Root 60% Raised Cosine Filter
Input wavetrain formulation: The input binary data stream is first applied to a scrambler with a 15-stage shift register which has a feedback polynomial of $1 + X + X^{15}$. The output of the scrambler is then applied to a convolutional encoder. The generator polynomials are:

$$G1: \ 1 + X^2 + X^3 + X^5 + X^6$$
$$G2: \ 1 + X + X^2 + X^3 + X^6$$

The generated polynomial outputs are combined in a punctuated 2/3 rate before the encoded data stream is applied to an interleaver of block size of 256 bits in 4 columns. The bit stream of the output of the interleaver is organized into words of 16 blocks of 256 bits each. The 16 blocks of data are preceded by a 104 bit long unique word for a total word length of 4200 bits. The quadrature phase shift

keying (QPSK) modulator phase shifts a subcarrier signal by 45, 135, -135, or -45 degrees depending on the state of each 2-bits of the input. The subcarrier signal now contains the information and is upconverted for transmission.

10500 BPS

Aviation Quadrature Phase Shift Keying (A-QPSK) with differential encoding
Square Root 100% Raised Cosine Filter
Input wavetrain formulation: The input binary data stream is first applied to a scrambler with a 15-stage shift register which has a feedback polynomial of $1 + X + X^{15}$. The output of the scrambler is then applied to a convolutional encoder. The generator polynomials are:

$$G1: \ 1 + X^2 + X^3 + X^5 + X^6$$
$$G2: \ 1 + X + X^2 + X^3 + X^6$$

The generated polynomial outputs are combined in a punctuated 1/2 rate before the encoded data stream is applied to an interleaver of block size of 4992 bits in 78 columns. The output bit stream of the interleaver is organized into a single block. The block of data is preceded by a 4 bit format identifier, a 12 bit superframe counter, and 178 dummy bits and is appended with a 64 bit unique word for a total word length of 1200 bits. Sixteen (16) words are subsequently organized into a superframe before it is applied to the modulator. The quadrature phase shift keying (QPSK) modulator phase shifts a subcarrier signal by 45, 135, -135, or -45 degrees depending on the state of each 2-bits of the input. The subcarrier signal now contains the information and is upconverted for transmission.

21000 BPS

Aviation Quadrature Phase Shift Keying (A-QPSK) with coherent filtering
Square Root 100% Raised Cosine Filter
Input wavetrain formulation: The input binary data stream is first applied to a scrambler with a 15-stage shift register which has a feedback polynomial of $1 + X + X^{15}$. The output of the scrambler is then applied to a convolutional encoder. The generator polynomials are:

$$G1: \ 1 + X^2 + X^3 + X^5 + X^6$$
$$G2: \ 1 + X + X^2 + X^3 + X^6$$

The generated polynomial outputs are combined in a punctuated 1/2 rate before the encoded data stream is applied to an interleaver of block size of 384 bits in 6 columns. The bit stream of the output of the interleaver is organized into words of 27 blocks of 384 bits each. The 27 blocks of data are preceded by an 840 bit preamble, an 88 bit long unique word, and 44 dummy bits for a total word length of 11,340 bits. The quadrature phase shift keying (QPSK) modulator phase shifts a subcarrier signal by 45, 135, -135, or -45 degrees depending on the state of each 2-bits of the input. The subcarrier signal now contains the information and is upconverted for transmission.

Bit Rate	Symbol Rate	Modulation Type
600	600	A-BPSK
1200	1200	A-BPSK
4800	2400	A-QPSK
8400	4200	A-QPSK
10500	5250	A-QPSK
21000	10500	A-QPSK

2.15 Required Measurements (Section 2.1033 (c) (14))

See **Exhibit 9**.