tain LQI value. Since the packet error rate is a statistical value, the PER shown in Section 8-6 "Conditional Packet Error Rate versus LQI" on page 99 is based on a huge number of transactions. A reliable estimation of the packet error rate cannot be based on a single or a small number of LQI values.

8.6.2   Request an LQI Measurement

The LQI byte can be obtained after a frame has been received by the radio transceiver. One additional byte is automatically attached to the received frame containing the LQI value. This information can also be read via Frame Buffer read access, see Section 6.2.2 "Frame Buffer Access Mode" on page 20. The LQI byte can be read after IRQ_3 (TRX_END) interrupt.

8.6.3   Data Interpretation

According to IEEE 802.15.4 a low LQI value is associated with low signal strength and/or high signal distortions. Signal distortions are mainly caused by interference signals and/or multipath propagation. High LQI values indicate a sufficient high signal power and low signal distortions.

Note, the received signal power as indicated by received signal strength indication (RSSI) value or energy detection (ED) value of the AT86RF231 do not characterize the signal quality and the ability to decode a signal.

As an example, a received signal with an input power of about 6 dB above the receiver sensitivity likely results in a LQI value close to 255 for radio channels with very low signal distortions. For higher signal power the LQI value becomes independent of the actual signal strength. This is because the packet error rate for these scenarios tends towards zero and further increased signal strength, i.e. increasing the transmission power does not decrease the error rate any further. In this case RSSI or ED can be used to evaluate the signal strength and the link margin.

ZigBee networks often require the identification of the "best" routing between two nodes. Both, the LQI and the RSSI/ED can be used for this, dependent on the optimization criteria. If a low packet error rate (corresponding to high throughput) is the optimization criteria then the LQI value should be taken into consideration. If a low transmission power or the link margin is the optimization criteria then the RSSI/ED value is also helpful.

Combinations of LQI, RSSI and ED are possible for routing decisions. As a rule of thumb RSSI and ED values are useful to differentiate between links with high LQI values. Transmission links with low LQI values should be discarded for routing decisions even if the RSSI/ED values are high. This is because RSSI/ED does not say anything about the possibility to decode a signal. It is only an information about the received signal strength whereas the source can be an interferer.
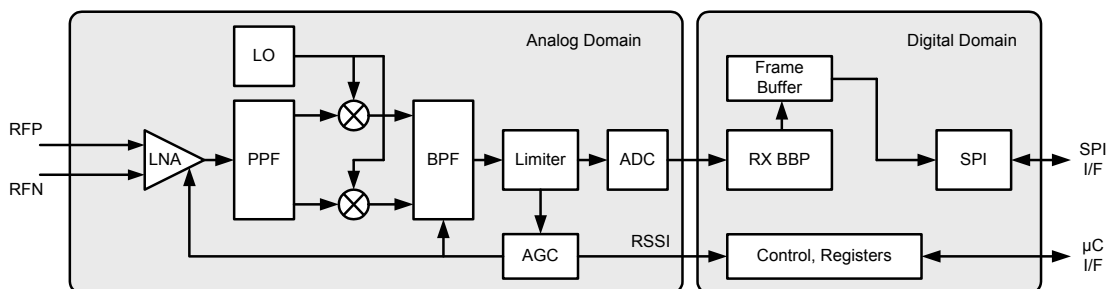
9. Module Description

9.1 Receiver (RX)

9.1.1 Overview

The AT86RF231 receiver is split into an analog radio front end and a digital base band processor (RX BBP), see Figure 9-1 on page 101.

Figure 9-1. Receiver Block Diagram

The differential RF signal is amplified by a low noise amplifier (LNA), filtered (PPF) and down converted to an intermediate frequency by a mixer. Channel selectivity is performed using an integrated band pass filter (BPF). A limiting amplifier (Limiter) provides sufficient gain to overcome the DC offset of the succeeding analog-to-digital converter (ADC) and generates a digital RSSI signal. The ADC output signal is sampled and processed further by the digital base band receiver (RX BBP).

The RX BBP performs additional signal filtering and signal synchronization. The frequency offset of each frame is calculated by the synchronization unit and is used during the remaining receive process to correct the offset. The receiver is designed to handle frequency and symbol rate deviations up to ±120 ppm, caused by combined receiver and transmitter deviations. For details refer to Section 12.5 "General RF Specifications" on page 158 parameter 12.5.8. Finally the signal is demodulated and the data are stored in the Frame Buffer.

In Basic Operating Mode, refer to Section 7.1 "Basic Operating Mode" on page 33, the reception of a frame is indicated by an interrupt IRQ_2 (RX_START). Accordingly its end is signalized by an interrupt IRQ_3 (TRX_END). Based on the quality of the received signal a link quality indicator (LQI) is calculated and appended to the frame, refer to Section 8.6 "Link Quality Indication (LQI)" on page 99. Additional signal processing is applied to the frame data to provide further status information like ED value (register 0x07, ED_LEVEL) and FCS correctness (register 0x06, PHY_RSSI).

Beyond these features the Extended Operating Mode of the AT86RF231 supports address filtering and pending data indication. For details refer to Section 7.2 "Extended Operating Mode" on page 47.

9.1.2 Frame Receive Procedure

The frame receive procedure including the radio transceiver setup for reception and reading PSDU data from the Frame Buffer is described in Section 10.1 "Frame Receive Procedure" on page 126.

9.1.3 Configuration

In Basic Operating Mode the receiver is enabled by writing command RX_ON to register bits TRX_CMD (register 0x02, TRX_STATE) in states TRX_OFF or PLL_ON. Similarly in Extended Operating Mode, the receiver is enabled for RX_AACK operation from states TRX_OFF or PLL_ON by writing the command RX_AACK_ON. There is no additional configuration required to receive IEEE 802.15.4 compliant frames when using the Basic Operating Mode. However, the frame reception in the Extended Operating Mode requires further register configurations, for details refer to Section 7.2 "Extended Operating Mode" on page 47.

The AT86RF231 receiver has an outstanding sensitivity performance of -101 dBm. At certain environmental conditions or for High Data Rate Modes, refer to Section 11.3 "High Data Rate Modes" on page 137, it may be useful to manually decrease this sensitivity. This is achieved by adjusting the synchronization header detector threshold using register bits RX_PDT_LEVEL (register 0x15, RX_SYN). Received signals with an RSSI value below the threshold do not activate the demodulation process.

Furthermore, it may be useful to protect a received frame against overwriting by subsequent received frames.

A Dynamic Frame Buffer Protection is enabled with register bit RX_SAFE_MODE (register 0x0C, TRX_CTRL_2) set, see Section 11.8 "Dynamic Frame Buffer Protection" on page 154. The receiver remains in RX_ON or RX_AACK_ON state until the whole frame is read by the microcontroller, indicated by /SEL = H during the SPI Frame Receive Mode. The Frame Buffer content is only protected if the FCS is valid.

A Static Frame Buffer Protection is enabled with register bit RX_PDT_DIS (register 0x15, RX_SYN) set. The receiver remains in RX_ON or RX_AACK_ON state and no further SHR is detected until the register bit RX_PDT_DIS is set back.

9.1.4   Register Description

Register 0x15 (RX_SYN):

This register controls the sensitivity threshold of the receiver.

Bit	7	6	5	4	3	2	1	0	
+0x15	RX_PDT_DIS		Reserved			RX_PDT_LEVEL			RX_SYN
Read/Write	R/W	R	R	R	R/W	R/W	R/W	R/W	
Reset Value	0	0	0	0	0	0	0	0	

- **Bit 7 - RX_PDT_DIS**

RX_PDT_DIS = 1 prevents the reception of a frame even if the radio transceiver is in receive modes. An ongoing frame reception is not affected. This operation mode is independent of the setting of register bits RX_PDT_LEVEL.

- **Bit [6:4] - Reserved**

- **Bit [3:0] - RX_ PDT_LEVEL**

These register bits desensitize the receiver such that frames with an RSSI level below the RX_PDT_LEVEL threshold level (if RX_PDT_LEVEL > 0) are not received. The threshold level can be calculated according to the following formula:

RX_THRES = RSSI_BASE_VAL + 3 * (RX_PDT_LEVEL -1), for RX_PDT_LEVEL > 0

Examples for certain register settings are given in Table 9-1 on page 103

Table 9-1.   Receiver Desensitization Threshold Level - RX_PDT_LEVEL

Value [Register]	RX Input Threshold Level	Value [dBm]
0x0	≤ RSSI_BASE_VAL (reset value)	RSSI value not considered
0x1	> RSSI_BASE_VAL + 0 * 3	> -90
...		
0xE	> RSSI_BASE_VAL + 13 * 3	> -51
0xF	> RSSI_BASE_VAL + 14 * 3	> -48

If register bits RX_PDT_LEVEL > 0 the current consumption of the receiver in states RX_ON and RX_AACK_ON is reduced by 500 µA, refer to Section 12.8 "Current Consumption Specifications" on page 161 parameter 12.8.4.
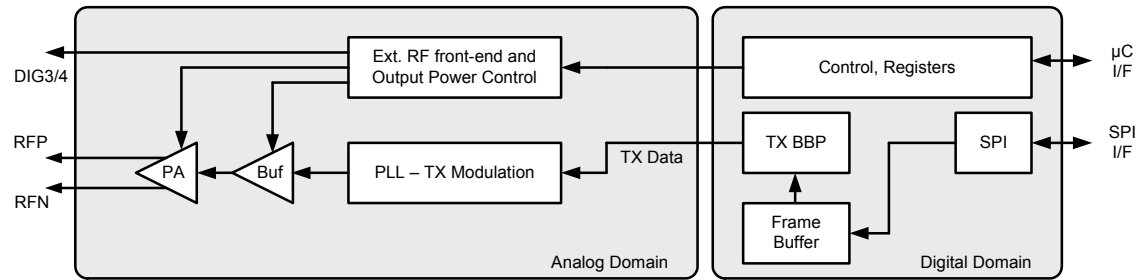
If register bits RX_PDT_LEVEL = 0 (reset value) all frames with a valid SHR and PHR are received, independently of their signal strength.

9.2 Transmitter (TX)

9.2.1 Overview

The AT86RF231 transmitter consists of a digital base band processor (TX BBP) and an analog radio front end, see Figure 9-2 on page 104.

Figure 9-2. Transmitter Block Diagram

The TX BBP reads the frame data from the Frame Buffer and performs the bit-to-symbol and symbol-to-chip mapping as specified by IEEE 802.15.4 in section 6.5.2. The O-QPSK modulation signal is generated and fed into the analog radio front end.

The fractional-N frequency synthesizer (PLL) converts the baseband transmit signal to the RF signal, which is amplified by the power amplifier (PA). The PA output is internally connected to bidirectional differential antenna pins (RFP, RFN), so that no external antenna switch is needed.

9.2.2 Frame Transmit Procedure

The frame transmit procedure including writing PSDU data in the Frame Buffer and initiating a transmission is described in Section 10.2 "Frame Transmit Procedure" on page 127, Frame Transmit Procedure.

9.2.3 Configuration

The maximum output power of the transmitter is typically +3 dBm. The output power can be configured via register bits TX_PWR (register 0x05, PHY_TX_PWR). The output power of the transmitter can be controlled over a range of 20 dB.

A transmission can be started from PLL_ON or TX_ARET_ON state by a rising edge of pin SLP_TR or by writing TX_START command to register bits TRX_CMD (register 0x02, TRX_STATE).

9.2.4 TX Power Ramping

To optimize the output power spectral density (PSD), the PA buffer and PA are enabled sequentially. This is illustrated by a timing example using default settings, shown in Figure 9-3 on page 105. In this example the transmission is initiated with the rising edge of pin 11 (SLP_TR). The radio transceiver state changes from PLL_ON to BUSY_TX. The modulation starts 16 µs after SLP_TR.

Figure 9-3. TX Power Ramping
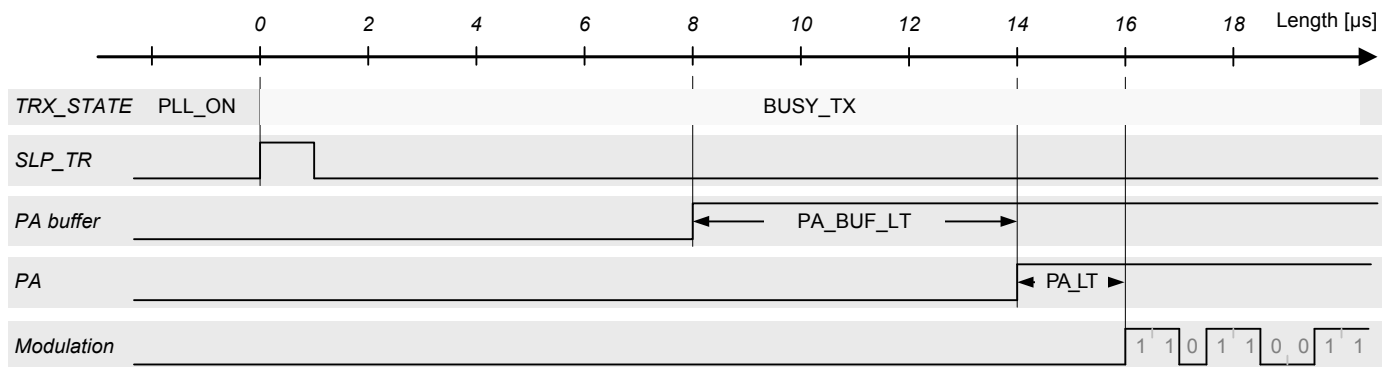
When using an external RF front-end (refer to Section 11.5 "RX/TX Indicator" on page 147) it may be required to adjust the startup time of the external PA relative to the internal building blocks to optimize the overall PSD. This can be achieved using register bits PA_BUF_LT and PA_LT.

9.2.5 Register Description

Register 0x05 (PHY_TX_PWR):

This register controls the output power and the ramping of the transmitter.

Bit	7	6	5	4	3	2	1	0	
+0x05	PA_BUF_LT		PA_LT		TX_PWR				PHY_TX_PWR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset Value	1	1	0	0	0	0	0	0	

- **Bit [7:6] - PA_BUF_LT**

These register bits control the enable lead time of the internal PA buffer relative to the enable time of the internal PA. This time is further used to derive a control signal for an external RF front-end to switch between receive and transmit, for details refer to Section 11.5.

Table 9-2. PA Buffer Enable Time Relative to the PA

Register Bits	Value	PA Buffer Lead Time [µs]
PA_BUF_LT	0	0
	1	2
	2	4
	3	6

- **Bit [5:4] - PA_LT**

These register bits control the enable lead time of the internal PA relative to the beginning of the transmitted frame.

Table 9-3. PA Enable Time Relative to the Start of the Frame (SHR)

Register Bits	Value	PA Lead Time [µs]
PA_LT	<u>0</u>	2
	1	4
	2	6
	3	8

- **Bit [3:0] - TX_PWR**

These register bits determine the TX output power of the AT86RF231.

Table 9-4. AT86RF231 TX Output Power Setting

Register Bits	Value	TX Output Power [dBm]
TX_PWR	<u>0x0</u>	3.0
	0x1	2.8
	0x2	2.3
	0x3	1.8
	0x4	1.3
	0x5	0.7
	0x6	0.0
	0x7	-1
	0x8	-2
	0x9	-3
	0xA	-4
	0xB	-5
	0xC	-7
	0xD	-9
	0xE	-12
	0xF	-17

9.3   Frame Buffer

The AT86RF231 contains a 128 byte dual port SRAM. One port is connected to the SPI interface, the other to the internal transmitter and receiver modules. For data communication, both ports are independent and simultaneously accessible.

The Frame Buffer uses the address space 0x00 to 0x7F for RX and TX operation of the radio transceiver and can keep one IEEE 802.15.4 RX or one TX frame of maximum length at a time.

Frame Buffer access modes are described in Section 6.6.2 "Register Description" on page 30. Frame Buffer access conflicts are indicated by an under run interrupt IRQ_6 (TRX_UR). Note that this interrupt also occurs on the attempt to write frames longer than 127 octets to the Frame Buffer. In that case the content of the Frame Buffer cannot be guaranteed.

Frame Buffer access is only possible if the digital voltage regulator is turned on. This is valid in all device states except in SLEEP state. An access in P_ON state is possible if pin 17 (CLKM) provides the 1 MHz master clock.

9.3.1   Data Management

Data in Frame Buffer (received data or data to be transmitted) remains valid as long as:

- No new frame or other data are written into the buffer over SPI
- No new frame is received (in any BUSY_RX state)
- No state change into SLEEP state is made
- No RESET took place

By default there is no protection of the Frame Buffer against overwriting. Therefore, if a frame is received during Frame Buffer read access of a previously received frame, interrupt IRQ_6 (TRX_UR) is issued and the stored data might be overwritten.

Even so, the old frame data can be read, if the SPI data rate is higher than the effective over air data rate. For a data rate of 250 kb/s a minimum SPI clock rate of 1 MHz is recommended. Finally the microcontroller should check the transferred frame data integrity by an FCS check.

To protect the Frame Buffer content against being overwritten by newly incoming frames the radio transceiver state should be changed to PLL_ON state after reception. This can be achieved by writing immediately the command PLL_ON to register bits TRX_CMD (register 0x02, TRX_STATE) after receiving the frame, indicated by IRQ_3 (TRX_END).

Alternatively Dynamic Frame Buffer Protection can be used to protect received frames against overwriting, for details refer to Section 11.8 "Dynamic Frame Buffer Protection" on page 154.

Both procedures do not protect the Frame Buffer from overwriting by the microcontroller.

In Extended Operating Mode during TX_ARET operation, see Section 7.2.4 "TX_ARET_ON - Transmit with Automatic Retry and CSMA-CA Retry" on page 64, the radio transceiver switches to receive, if an acknowledgement of a previously transmitted frame was requested. During this period received frames are evaluated, but not stored in the Frame Buffer. This allows the radio transceiver to wait for an acknowledgement frame and retry the frame transmission without writing them again.

A radio transceiver state change, except a transition to SLEEP state or a reset, does not affect the Frame Buffer contents. If the radio transceiver is forced into SLEEP, the Frame Buffer is powered off and the stored data gets lost.

9.3.2   User accessible Frame Content

The AT86RF231 supports an IEEE 802.15.4 compliant frame format as shown in Figure 9-4 on page 108.

Figure 9-4.   AT86RF231 Frame Structure
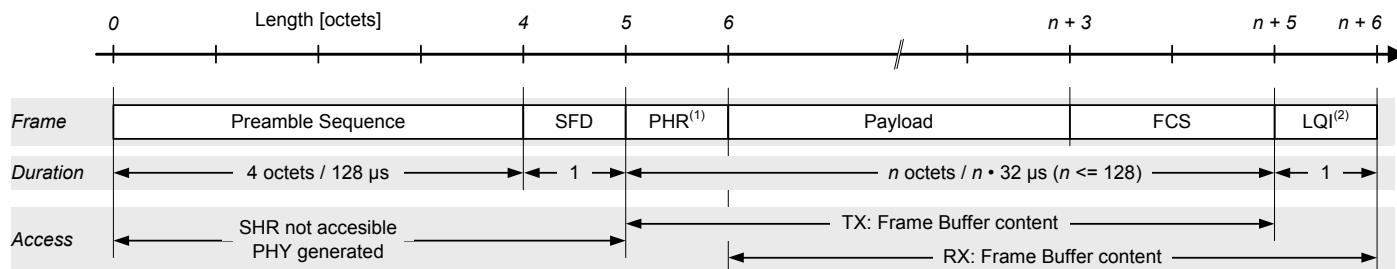
Notes: 1. Stored into Frame Buffer for TX operation
         2. Stored into Frame Buffer during frame reception.

A frame comprises two sections, the radio transceiver internally generated SHR field and the user accessible part stored in the Frame Buffer. The SHR contains the preamble and the SFD field. The variable frame section contains the PHR and the PSDU including the FCS, see Section 8.2 "Frame Check Sequence (FCS)" on page 85.

The Frame Buffer content differs depending on the direction of the communication (receive or transmit). To access the data follow the procedures described in Section 6.2.2 "Frame Buffer Access Mode" on page 20.

During frame reception, the payload and the link quality indicator (LQI) value of a successfully received frame are stored in the Frame Buffer. The radio transceiver appends the LQI value to the frame data after the last received octet. The frame length information is not stored in the Frame Buffer. When using the Frame Buffer access mode to read the Frame Buffer content, the frame length information is placed before the payload.

If the SRAM read access is used to read an RX frame, the frame length field (PHR) cannot be accessed. The SHR (except the SFD used to generate the SHR) can generally not be read by the microcontroller.

For frame transmission, the PHR and the PSDU needs to be stored in the Frame Buffer. The PHR byte is the first byte in the Frame Buffer and must be calculated based on the PHR and the PSDU. The maximum frame size supported by the radio transceiver is 128 bytes. If the TX_AUTO_CRC_ON bit is set in register 0x05 (PHY_TX_PWR), the FCS field of the PSDU is replaced by the automatically calculated FCS during frame transmission. That's why there is no need to write the FCS field when using the automatic FCS generation.

To manipulate individual bytes of the Frame Buffer a SRAM write access can be used instead.

For non IEEE 802.15.4 compliant frames, the minimum frame length supported by the radio transceiver is one byte (Frame Length Field + 1 byte of data).

9.3.3 Interrupt Handling

Access conflicts may occur when reading and writing data simultaneously at the two independent ports of the Frame Buffer, TX/RX BBP and SPI. Both of these ports have their own address counter that points to the Frame Buffer's current address.

Access violations occurs during concurrent Frame Buffer read or write accesses, when the SPI port's address counter value becomes higher than or equal to that of TX/RX BBP port.

While receiving a frame, primarily the data needs to be stored in the Frame Buffer before reading it. This can be ensured by accessing the Frame Buffer 32 µs after IRQ_2 (RX_START) at the earliest. When reading the frame data continuously the SPI data rate shall be lower than 250 kb/s to ensure no under run interrupt occurs. To avoid access conflicts and to simplify the Frame Buffer read access Frame Buffer Empty indication may be used, for details refer to Section 11.7 "Frame Buffer Empty Indicator" on page 152.

While transmitting an access violation occurs during a Frame Buffer write access, when the SPI port's address counter value becomes less than or equal to that of TX BBP port.

Both these access violations may cause data corruption and are indicated by IRQ_6 (TRX_UR) interrupt when using the Frame Buffer access mode. Access violations are not indicated when using the SRAM access mode.

Notes

- Interrupt IRQ_6 (TRX_UR) is valid 64 µs after IRQ_2 (RX_START). The occurrence of the interrupt can be disregarded when reading the first byte of the Frame Buffer between 32 µs and 64 µs after the RX_START interrupt.
- If a Frame Buffer read access is not finished until a new frame is received, a TRX_UR interrupt occurs. Nevertheless the old frame data can be read, if the SPI data rate is higher than the effective PHY data rate. A minimum SPI clock rate of 1 MHz is recommended in this case. Finally, the microcontroller should check the integrity of the transferred frame data by calculating the FCS.
- When writing data to the Frame Buffer during frame transmission, the SPI data rate shall be higher than the PHY data rate to ensure no under run interrupt. The first byte of the PSDU data must be available in the Frame Buffer before SFD transmission is complete, which takes 176 µs (16 µs PA ramp up + 160 µs SHR) from the rising edge of SLP_TR pin (see Figure 7-2 on page 39).

9.4 Voltage Regulators (AVREG, DVREG)

The main features of the Voltage Regulator blocks are:

- Bandgap stabilized 1.8V supply for analog and digital domain
- Low dropout (LDO) voltage regulator
- Configurable for usage of external voltage regulator

9.4.1 Overview

The internal voltage regulators supply a stabilized voltage to the AT86RF231. The AVREG provides the regulated 1.8V supply voltage for the analog section and the DVREG supplies the 1.8V supply voltage for the digital section.

A simplified schematic of the internal voltage regulator is shown in Figure 9-5 on page 110.

Figure 9-5. Simplified Schematic of AVREG/DVREG
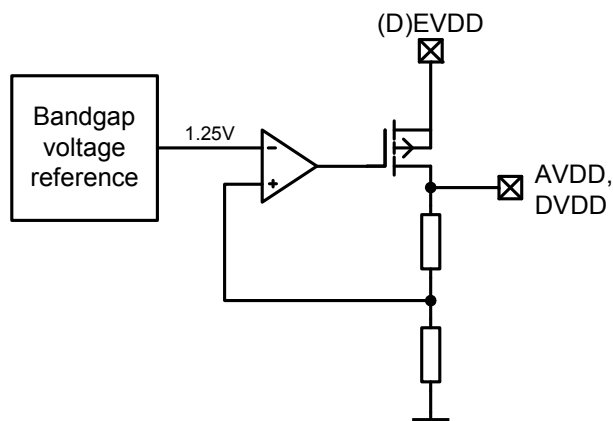
The voltage regulators require bypass capacitors for stable operation. The value of the bypass capacitors determine the settling time of the voltage regulators. The bypass capacitors shall be placed as close as possible to the pins and shall be connected to ground with the shortest possible traces.

9.4.2 Configuration

The voltage regulators can be configured by the register 0x10 (VREG_CTRL).

It is recommended to use the internal regulators, but it is also possible to supply the low voltage domains by an external voltage supply. For this configuration, the internal regulators need to be switched off by setting the register bits to the values AVREG_EXT = 1 and DVREG_EXT = 1. A regulated external supply voltage of 1.8V needs to be connected to the pins 13, 14 (DVDD) and pin 29 (AVDD). When turning on the external supply, ensure a sufficiently long stabilization time before interacting with the AT86RF231.

9.4.3 Data Interpretation

The status bits AVDD_OK = 1 and DVDD_OK = 1 of register 0x10 (VREG_CTRL) indicate an enabled and stable internal supply voltage. Reading value 0 indicates a disabled or internal supply voltage not settled to the final value.

9.4.4   Register Description

Register 0x10 (VREG_CTRL):

This register controls the use of the voltage regulators and indicates the status of these.

Bit	7	6	5	4	3	2	1	0	
+0x10	AVREG_EXT	AVDD_OK	Reserved		DVREG_EXT	DVDD_OK	Reserved		VREG_CTRL
Read/Write	R/W	R	R/W	R/W	R/W	R	R/W	R/W	
Reset Value	0	0	0	0	0	0	0	0	

- **Bit 7 - AVREG_EXT**

If set this register bit disables the internal analog voltage regulator to apply an external regulated 1.8V supply for the analog building blocks.

Table 9-5.   Regulated Voltage Supply Control for Analog Building Blocks

Register Bit	Value	Description
AVREG_EXT	<u>0</u>	Internal voltage regulator enabled, analog section
	1	Internal voltage regulator disabled, use external regulated 1.8V supply voltage for the analog section

- **Bit 6 - AVDD_OK**

This register bit indicates if the internal 1.8V regulated voltage supply AVDD has settled. The bit is set to logic high, if AVREG_EXT = 1.

Table 9-6.   Regulated Voltage Supply Control for Analog Building Blocks

Register Bit	Value	Description
AVDD_OK	<u>0</u>	Analog voltage regulator disabled or supply voltage not stable
	1	Analog supply voltage has settled

- **Bit [5:4] - Reserved**

- **Bit 3 - DVREG_EXT**

If set this register bit disables the internal digital voltage regulator to apply an external regulated 1.8V supply for the digital building blocks.

Table 9-7.   Regulated Voltage Supply Control for Digital Building Blocks

Register Bit	Value	Description
DVREG_EXT	<u>0</u>	Internal voltage regulator enabled, digital section
	1	Internal voltage regulator disabled, use external regulated 1.8V supply voltage for the digital section

- **Bit 2 - DVDD_OK**

This register bit indicates if the internal 1.8V regulated voltage supply DVDD has settled. The bit is set to logic high, if DVREG_EXT = 1.

Table 9-8. Regulated Voltage Supply Control for Digital Building Blocks

Register Bit	Value	Description
DVDD_OK	<u>0</u>	Digital voltage regulator disabled or supply voltage not stable
	1	Digital supply voltage has settled

Note

- While the reset value of this bit is 0, any practical access to the register is only possible when DVREG is active. So this bit is normally always read out as 1.

- **Bit [1:0] - Reserved**

9.5 Battery Monitor (BATMON)

The main features of the battery monitor are:

- Configurable voltage threshold range: 1.7V to 3.675V
- Generates an interrupt when supply voltage drops below a threshold

9.5.1 Overview

The battery monitor (BATMON) detects and indicates a low supply voltage of the external supply voltage at pin 28 (EVDD). This is done by comparing the voltage on the external supply pin 28 (EVDD) with a configurable internal threshold voltage. A simplified schematic of the BATMON with the most important input and output signals is shown in Figure 9-6 on page 113.

Figure 9-6. Simplified Schematic of BATMON
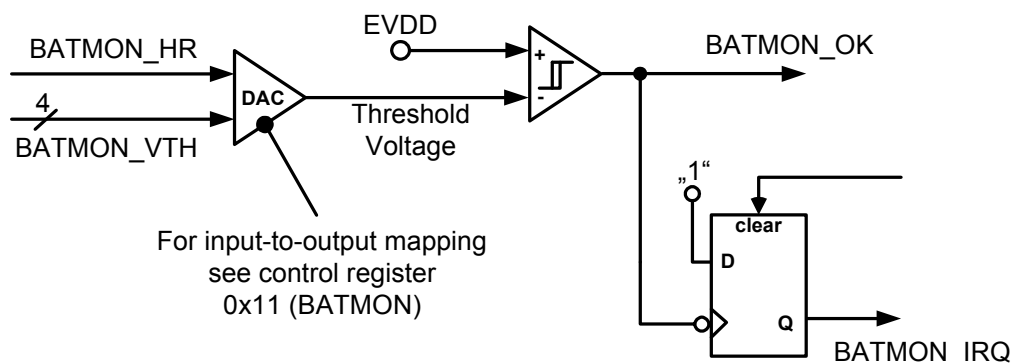
9.5.2 Configuration

The BATMON can be configured using the register 0x11 (BATMON). Register subfield BATMON_VTH sets the threshold voltage. It is configurable with a resolution of 75 mV in the upper voltage range (BATMON_HR = 1) and with a resolution of 50 mV in the lower voltage range (BATMON_HR = 0), for details refer to register 0x11 (BATMON).

9.5.3 Data Interpretation

The signal bit BATMON_OK of register 0x11 (BATMON) monitors the current value of the battery voltage:

- If BATMON_OK = 0, the battery voltage is lower than the threshold voltage
- If BATMON_OK = 1, the battery voltage is higher than the threshold voltage

After setting a new threshold, the value BATMON_OK should be read out to verify the current supply voltage value.

Note, the battery monitor is inactive during P_ON and SLEEP states, see status register 0x01 (TRX_STATUS).

9.5.4 Interrupt Handling

A supply voltage drop below the configured threshold value is indicated by an interrupt IRQ_7 (BAT_LOW), see Section 6.6 "Interrupt Logic" on page 29. Note that the interrupt is issued only if BATMON_OK changes from 1 to 0.

No interrupt is generated when:

- The battery voltage is under the default 1.8V threshold at power up (BATMON_OK was never 1), or
- A new threshold is set, which is still above the current supply voltage (BATMON_OK remains 0).

When the battery voltage is close to the programmed threshold voltage, noise or temporary voltage drops may generate unwanted interrupts. To avoid this:

- Disable the IRQ_7 (BAT_LOW) in register 0x0E (IRQ_MASK) and treat the battery as empty, or
- Set a lower threshold value.

9.5.5 Register Description

Register 0x11 (BATMON):

This register configures the battery monitor to compare the supply voltage at pin 28 (EVDD) to the threshold BATMON_VTH. Additionally the supply voltage status at pin 28 (EVDD) is accessible by reading register bit BATMON_OK according to the actual BATMON settings.

Bit	7	6	5	4	3	2	1	0	
+0x11	Reserved		BATMON_OK	BATMON_HR	BATMON_VTH				BATMON
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Reset Value	0	0	0	0	0	0	1	0	

- **Bit [7:6] - Reserved**

- **Bit 5 - BATMON_OK**

The register bit BATMON_OK indicates the level of the external supply voltage with respect to the programmed threshold BATMON_VTH.

Table 9-9. Battery Monitor Status

Register Bit	Value	Description
BATMON_OK	0	The battery voltage is below the threshold.
	1	The battery voltage is above the threshold.

- **Bit 4 - BATMON_HR**

BATMON_HR sets the range and resolution of the battery monitor.

Table 9-10. Battery Monitor Range Selection

Register Bit	Value	Description
BATMON_HR	0	Enables the low range, see BATMON_VTH
	1	Enables the high range, see BATMON_VTH

• **Bit [3:0] - BATMON_VTH**

The threshold values for the battery monitor are set by register bits BATMON_VTH:

Table 9-11. Battery Monitor Threshold Voltage

Value BATMON_VTH[3:0]	Voltage [V] BATMON_HR = 1	Voltage [V] BATMON_HR = 0
0x0	2.550	1.70
0x1	2.625	1.75
0x2	2.700	1.80
0x3	2.775	1.85
0x4	2.850	1.90
0x5	2.925	1.95
0x6	3.000	2.00
0x7	3.075	2.05
0x8	3.150	2.10
0x9	3.225	2.15
0xA	3.300	2.20
0xB	3.375	2.25
0xC	3.450	2.30
0xD	3.525	2.35
0xE	3.600	2.40
0xF	3.675	2.45

9.6 Crystal Oscillator (XOSC)

The main crystal oscillator features are:

- 16 MHz amplitude controlled crystal oscillator
- 330 µs typical settling time after leaving SLEEP state
- Configurable trimming capacitance array
- Configurable clock output (CLKM)

9.6.1 Overview

The crystal oscillator generates the reference frequency for the AT86RF231. All other internally generated frequencies of the radio transceiver are derived from this unique frequency. Therefore, the overall system performance is mainly determined by the accuracy of crystal reference frequency. The external components of the crystal oscillator should be selected carefully and the related board layout should be done with caution (see Section 5. "Application Circuits" on page 12).

The register 0x12 (XOSC_CTRL) provides access to the control signals of the oscillator. Two operating modes are supported. It is recommended to use the integrated oscillator setup as described in Figure 9-7 on page 116; nevertheless a reference frequency can be fed to the internal circuitry by using an external clock reference as shown in Figure 9-8 on page 117.

9.6.2 Integrated Oscillator Setup

Using the internal oscillator, the oscillation frequency depends on the load capacitance between the crystal pins XTAL1 and XTAL2. The total load capacitance C_L must be equal to the specified load capacitance of the crystal itself. It consists of the external capacitors CX and parasitic capacitances connected to the XTAL nodes.

Figure 9-7 on page 116 shows all parasitic capacitances, such as PCB stray capacitances and the pin input capacitance, summarized to C_{PAR}.

Figure 9-7. Simplified XOSC Schematic with External Components
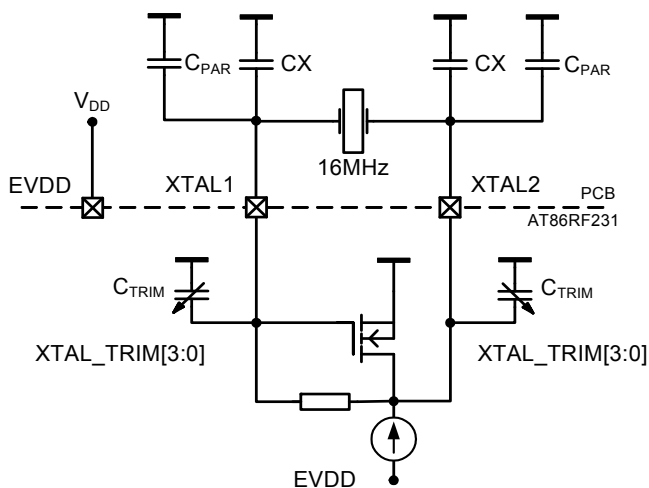
Additional internal trimming capacitors C_{TRIM} are available. Any value in the range from 0 pF to 4.5 pF with a 0.3 pF resolution is selectable using XTAL_TRIM of register 0x12 (XOSC_CTRL).

To calculate the total load capacitance, the following formula can be used:

$C_L = 0.5 * (CX + C_{TRIM} + C_{PAR})$.

The trimming capacitors provide the possibility of reducing frequency deviations caused by production process variations or by external components tolerances. Note that the oscillation frequency can only be reduced by increasing the trimming capacitance. The frequency deviation caused by one step of C_{TRIM} decreases with increasing crystal load capacitor values.

An amplitude control circuit is included to ensure stable operation under different operating conditions and for different crystal types. Enabling the crystal oscillator in P_ON state and after leaving SLEEP state causes a slightly higher current during the amplitude build-up phase to guarantee a short start-up time. At stable operation, the current is reduced to the amount necessary for a robust operation. This also keeps the drive level of the crystal low.

Generally, crystals with a higher load capacitance are less sensitive to parasitic pulling effects caused by external component variations or by variations of board and circuit parasitics. On the other hand, a larger crystal load capacitance results in a longer start-up time and a higher steady state current consumption.

9.6.3   External Reference Frequency Setup

When using an external reference frequency, the signal must be connected to pin 26 (XTAL1) as indicated in Figure 9-8 on page 117 and the register bits XTAL_MODE (register 0x12, XOSC_CTRL) need to be set to the external oscillator mode. The oscillation peak-to-peak amplitude shall be between 100 mV and 500 mV, the optimum range is between 400 mV and 500 mV. Pin 25 (XTAL2) should not be wired.

Figure 9-8.   Setup for Using an External Frequency Reference
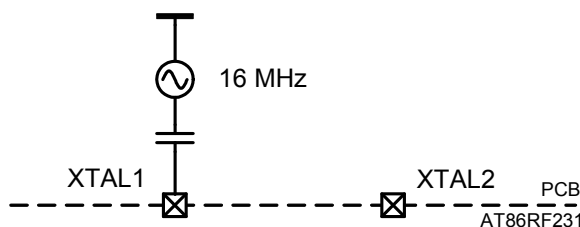
9.6.4   Master Clock Signal Output (CLKM)

The generated reference clock signal can be fed to a microcontroller using pin 17 (CLKM). The internal 16 MHz raw clock can be divided by an internal prescaler. Thus, clock frequencies of 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, 250 kHz, or 62.5 kHz can be supplied by pin CLKM.

The CLKM frequency, update scheme, and pin driver strength is configurable using register 0x03 (TRX_CTRL_0). There are two possibilities how a CLKM frequency change gets effective. If CLKM_SHA_SEL = 0 and/or CLKM_CTRL = 0, changing the register bits CLKM_CTRL immediately affects the CLKM clock rate. Otherwise (CLKM_SHA_SEL = 1 and CLKM_CTRL > 0 before changing the register bits CLKM_CTRL) the new clock rate is supplied when leaving the SLEEP state the next time.

To reduce power consumption and spurious emissions, it is recommended to turn off the CLKM clock when not in use or to reduce its driver strength to a minimum, refer to Section 1.3 "Digital Pins" on page 7.

Note:
- During reset procedure, see Section 7.1.2.8 "RESET State" on page 37, register bits CLKM_CTRL are shadowed. Although the clock setting of CLKM remains after reset, a read access to register bits CLKM_CTRL delivers the reset value 1. For that reason it is recommended to write the previous configuration (before reset) to register bits CLKM_CTRL (after reset) to align the radio transceiver behavior and register configuration. Otherwise the CLKM clock rate is set back to the reset value (1 MHz) after the next SLEEP cycle.
- For example, if the CLKM clock rate is configured to 16 MHz the CLKM clock rate remains at 16 MHz after a reset, however the register bits CLKM_CTRL are set back to 1. Since CLKM_SHA_SEL reset value is 1, the CLKM clock rate changes to 1 MHz after the next SLEEP cycle if the CLKM_CTRL setting is not updated after reset.

9.6.5   Register Description
Register 0x03 (TRX_CTRL_0):

Bit	7	6	5	4	3	2	1	0	
+0x03	PAD_IO		PAD_IO_CLKM		CLKM_SHA_SEL	CLKM_CTRL			TRX_CTRL_0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	1	1	0	0	1	

The TRX_CTRL_0 register controls the drive current of the digital output pads and the CLKM clock rate. It is recommended to use the lowest value for the drive current to reduce the current consumption and the emission of signal harmonics.

- **Bit [7:6] - PAD_IO**

Refer to Section 1.3 "Digital Pins" on page 7.

- **Bit [5:6] - PAD_IO_CLKM**

These register bits set the output driver current of pin CLKM. It is recommended to reduce the current capability to PAD_IO_CLKM = 0 (2 mA) if possible. This reduces power consumption and spurious emissions.

Table 9-12.   CLKM Driver Strength

Register Bit	Value	Description
PAD_IO_CLKM	0	2 mA
	1	4 mA
	2	6 mA
	3	8 mA

- **Bit 3 - CLKM_SHA_SEL**

Register bit CLKM_SHA_SEL defines if a new clock rate, defined by CLKM_CTRL, is set immediately or after the next SLEEP cycle.

Table 9-13.   CLKM Clock Rate Update Scheme

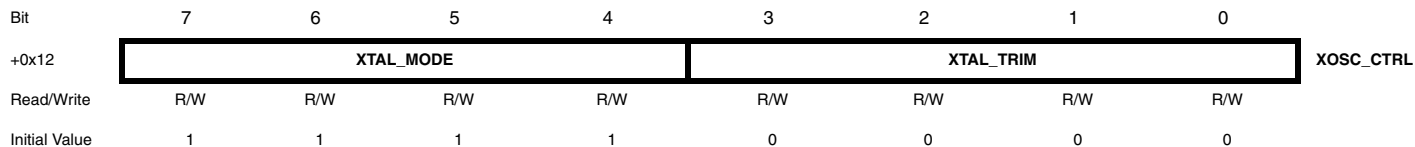| Register Bit	Value	Description
CLKM_SHA_SEL	0	CLKM clock rate change appears immediately
	1	CLKM clock rate change appears after SLEEP cycle

- **Bit [2:0] - CLKM_CTRL**

These register bits set clock rate of pin 17 (CLKM).

Table 9-14. Clock Rate Setting at pin CLKM

Register Bit	Value	Description
CLKM_CTRL	0	No clock at pin 17 (CLKM), pin set to logic low
	<u>1</u>	1 MHz
	2	2 MHz
	3	4 MHz
	4	8 MHz
	5	16 MHz
	6	250 kHz
	7	62.5 kHz (IEEE 802.15.4 symbol rate)

Register 0x12 (XOSC_CTRL):

The register XOSC_CTRL controls the operation of the crystal oscillator.

Bit	7	6	5	4	3	2	1	0	
+0x12			XTAL_MODE				XTAL_TRIM		XOSC_CTRL
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	0	0	0	0	

- **Bit [7:4] - XTAL_MODE**

These register bits set the operating mode of the crystal oscillator. For normal operation the default value is set to XTAL_MODE = <u>0xF</u> after reset. Using an external clock source it is recommended to set XTAL_MODE = 0x4.

Table 9-15. Crystal Oscillator Operating Mode

Register Bit	Value	Description
XTAL_MODE	0x4	Internal crystal oscillator disabled, use external reference frequency
	<u>0xF</u>	Internal crystal oscillator enabled XOSC voltage regulator enabled

• **Bit [3:0] - XTAL_TRIM**

The register bits XTAL_TRIM control two internal capacitance arrays connected to pins XTAL1 and XTAL2. A capacitance value in the range from 0 pF to 4.5 pF is selectable with a resolution of 0.3 pF.

Table 9-16. Crystal Oscillator Trimming Capacitors

Register Bit	Value	Description
XTAL_TRIM	0x0	0.0 pF, trimming capacitors disconnected
	0x1	0.3 pF trimming capacitor switched on
	...	
	0xF	4.5 pF trimming capacitor switched on

9.7   Frequency Synthesizer (PLL)

The main PLL features are:

- Generate RX/TX frequencies for all IEEE 802.15.4 - 2.4 GHz channels
- Autonomous calibration loops for stable operation within the operating range
- Two PLL-interrupts for status indication
- Fast PLL settling to support frequency hopping

9.7.1   Overview

The PLL generates the RF frequencies for the AT86RF231. During receive operation the frequency synthesizer works as a local oscillator on the radio transceiver receive frequency, during transmit operation the voltage-controlled oscillator (VCO) is directly modulated to generate the RF transmit signal. The frequency synthesizer is implemented as a fractional-N PLL.

Two calibration loops ensure correct PLL functionality within the specified operating limits.

9.7.2   RF Channel Selection

The PLL is designed to support 16 channels in the 2.4 GHz ISM band with a channel spacing of 5 MHz according to IEEE 802.15.4. The center frequency of these channels is defined as follows:

$F_c = 2405 + 5 (k - 11)$ in [MHz], for k = 11, 12,..., 26

where k is the channel number.

The channel k is selected by register bits CHANNEL (register 0x08, PHY_CC_CA).

9.7.3   Frequency Agility

When the PLL is enabled during state transition from TRX_OFF to PLL_ON, the settling time is typically t_{TR4} = 110 μs, including settling of the analog voltage regulator (AVREG) and PLL self calibration, refer to and . A lock of the PLL is indicated with an interrupt IRQ_0 (PLL_LOCK).

Switching between 2.4 GHz ISM band channels in PLL_ON or RX_ON states is typically done within t_{TR20} = 11 μs. This makes the radio transceiver highly suitable for frequency hopping applications.

When starting the transmit procedure the PLL frequency is changed to the transmit frequency within a period of t_{TR23} = 16 μs before starting the transmission. After the transmission the PLL settles back to the receive frequency within a period of t_{TR24} = 32 μs. This frequency step does not generate an interrupt IRQ_0 (PLL_LOCK) or IRQ_1 (PLL_UNLOCK) within these periods.

9.7.4   Calibration Loops

Due to variation of temperature, supply voltage and part-to-part variations of the radio transceiver the VCO characteristics may vary.

To ensure a stable operation, two automated control loops are implemented, center frequency (CF) tuning and delay cell (DCU) calibration. Both calibration loops are initiated automatically when the PLL is enabled during state transition from TRX_OFF to PLL_ON state. Additionally, center frequency calibration is initiated when the PLL changes to a different channel center frequency.

If the PLL operates for a long time on the same channel, e.g. more than 5 min, or the operating temperature changes significantly, it is recommended to initiate the calibration loops manually.

Both calibration loops can be initiated manually by setting PLL_CF_START = 1 (register 0x1A, PLL_CF) and register bit PLL_DCU_START = 1 (register 0x1B, PLL_DCU). To start the calibration the device must be in PLL_ON or RX_ON state. The completion of the center frequency tuning is indicated by a PLL_LOCK interrupt.

Both calibration loops may be run simultaneously.

9.7.5   Interrupt Handling

Two different interrupts indicate the PLL status (refer to register 0x0F). IRQ_0 (PLL_LOCK) indicates that the PLL has locked. IRQ_1 (PLL_UNLOCK) interrupt indicates an unexpected unlock condition. A PLL_LOCK interrupt clears any preceding PLL_UNLOCK interrupt automatically and vice versa.

A PLL_LOCK interrupt is supposed to occur in the following situations:

  • State change from TRX_OFF to PLL_ON / RX_ON / TX_ARET_ON / RX_AACK_ON
  • Channel change in states PLL_ON / RX_ON / TX_ARET_ON / RX_AACK_ON

Any other occurrences of PLL interrupts indicate erroneous behavior and require checking of the actual device status.

The state transition from BUSY_TX to PLL_ON after successful transmission does not generate an IRQ_0 (PLL_LOCK) within the settling period.

9.7.6   Register Description

Register 0x08 (PHY_CC_CCA):

This register sets the IEEE 802.15.4 - 2.4 GHz channel number

Bit	7	6	5	4	3	2	1	0	
+0x08	CCA_REQUEST	CCA_MODE		CHANNEL					PHY_CC_CCA
Read/Write	W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset Value	0	0	1	0	1	0	1	1	

  • **Bit 7 - CCA_REQUEST**
Refer to Section 8.5 "Clear Channel Assessment (CCA)" on page 94.

  • **Bit [6:5] - CCA_MODE**
Refer to Section 8.5 "Clear Channel Assessment (CCA)" on page 94.

  • **Bit [4:0] - CHANNEL**
The register bits CHANNEL define the RX/TX channel. The channel assignment is according to IEEE 802.15.4.

Table 9-17. Channel Assignment for IEEE 802.15.4 - 2.4 GHz Band

Register Bit	Value	Channel Number k	Center Frequency [MHz]
CHANNEL	0x0B	11	2405
	0x0C	12	2410
	0x0D	13	2415
	0x0E	14	2420
	0x0F	15	2425
	0x10	16	2430
	0x11	17	2435
	0x12	18	2440
	0x13	19	2445
	0x14	20	2450
	0x15	21	2455
	0x16	22	2460
	0x17	23	2465
	0x18	24	2470
	0x19	25	2475
	0x1A	26	2480

Register 0x1A (PLL_CF):

This register controls the operation of the center frequency calibration loop.

Bit	7	6	5	4	3	2	1	0	
+0x1A	PLL_CF_START				Reserved				PLL_CF
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset Value	0	1	0	1	0	1	1	1	

- **Bit 7 - PLL_CF_START**

PLL_CF_START = 1 initiates the center frequency calibration. The calibration cycle has finished after t_{TR21} = 35 µs (typ.). The register bit is cleared immediately after finishing the calibration.

- **Bit [6:0] - Reserved**

Register 0x1B (PLL_DCU):

This register controls the operation of the delay cell calibration loop.

Bit	7	6	5	4	3	2	1	0	
+0x1B	PLL_DCU_START				Reserved				PLL_DCU
Read/Write	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	
Reset Value	0	0	1	0	0	0	0	0	

- **Bit 7 - PLL_DCU_START**

PLL_DCU_START = 1 initiates the delay cell calibration. The calibration cycle has finished after at most t_{TR22} = 6 µs, the register bit is set to 0. The register bit is cleared immediately after finishing the calibration.

- **Bit [6:0] - Reserved**

9.8 Automatic Filter Tuning (FTN)

9.8.1 Overview

The FTN is incorporated to compensate device tolerances for temperature, supply voltage variations as well as part-to-part variations of the radio transceiver. The filter-tuning result is used to correct the analog baseband filter transfer function and the PLL loop-filter time constant, refer to Section 4. "General Circuit Description" on page 10.

An FTN calibration cycle is initiated automatically when entering the TRX_OFF state from the SLEEP, RESET or P_ON states.

Although receiver and transmitter are very robust against these variations, it is recommended to initiate the FTN manually if the radio transceiver does not use the SLEEP state. If necessary, a calibration cycle is to be initiated in states TRX_OFF, PLL_ON or any receive state. This applies in particular for the High Data Rate Modes with a much higher sensitivity against BPF transfer function variations. The recommended calibration interval is 5 min or less.

9.8.2 Register Description

Register 0x18 (FTN_CTRL):

This register controls the operation of the filter tuning network calibration loop.

Bit	7	6	5	4	3	2	1	0	
+0x18	FTN_START	Reserved							FTN_CTRL
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset Value	0	1	0	1	1	0	0	0	

- **Bit 7 - FTN_START**

FTN_START = 1 initiates the filter tuning network calibration. When the calibration cycle has finished after at most 25 µs the register bit is automatically reset to 0.

- **Bit [6:0] - Reserved**

10. Radio Transceiver Usage

This section describes basic procedures to receive and transmit frames using the AT86RF231. For a detailed programming description refer to reference [6].

10.1 Frame Receive Procedure

A frame reception comprises of two actions: The PHY listens for, receives and demodulates the frame to the Frame Buffer and signalizes the reception to the microcontroller. After or while that the microcontroller read the available frame data from the Frame Buffer via the SPI interface.

While in state RX_ON or RX_AACK_ON the radio transceiver searches for incoming frames on the selected channel. Assuming the appropriate interrupts are enabled, a detection of an IEEE 802.15.4 compliant frame is indicated by interrupt IRQ_2 (RX_START) first. The frame reception is completed when issuing interrupt IRQ_3 (TRX_END).

Different Frame Buffer read access scenarios are recommended for:

- Non-time critical applications   read access starts after IRQ_3 (TRX_END)
- Time-critical applications   read access starts after IRQ_2 (RX_START)

Waiting for IRQ_3 (TRX_END) interrupt before starting a Frame Buffer read access is recommended for operations considered to be none time critical. Figure 10-1 on page 126 illustrates the frame receive procedure using IRQ_3 (TRX_END).

Figure 10-1. Transactions between AT86RF231 and Microcontroller during Receive
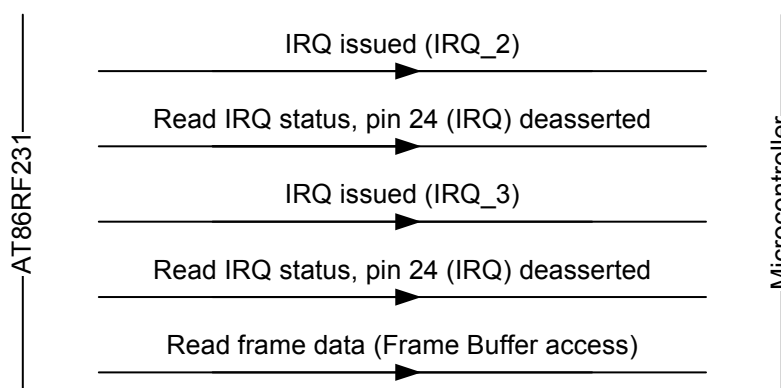
Critical protocol timing could require starting the Frame Buffer read access after interrupt IRQ_2 (RX_START). The first byte of the frame data can be read 32 µs after the IRQ_2 (RX_START) interrupt. The microcontroller must ensure to read slower than the frame is received. Otherwise a Frame Buffer under run occurs, IRQ_6 (TRX_UR) is issued, and the frame data may be not valid. To avoid this, the Frame Buffer read access can be controlled by using a Frame Buffer Empty indicator, refer to Section 11.7 "Frame Buffer Empty Indicator" on page 152.

10.2 Frame Transmit Procedure

A frame transmission comprises of two actions, a Frame Buffer write access and the transmission of the Frame Buffer content. Both actions can be run in parallel if required by critical protocol timing.

Figure 10-2 on page 127 illustrates the frame transmit procedure, when writing and transmitting the frame consecutively. After a Frame Buffer write access, the frame transmission is initiated by asserting pin 11 (SLP_TR) or writing command TX_START to register 0x02 (TRX_STATE), while the radio transceiver is in state PLL_ON or TX_ARET_ON. The completion of the transaction is indicated by interrupt IRQ_3 (TRX_END).

Figure 10-2. Transaction between AT86RF231 and Microcontroller during Transmit
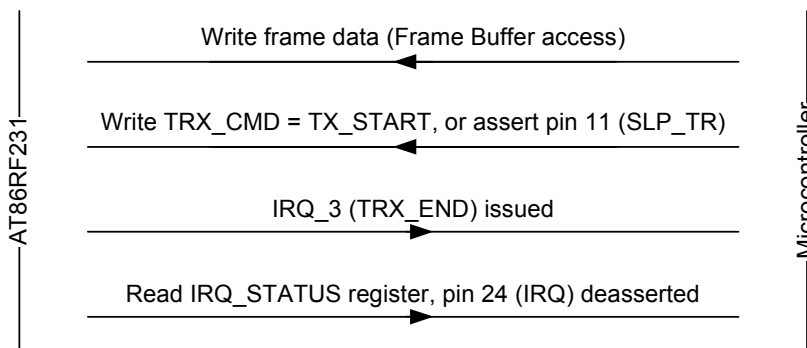
Alternatively a frame transmission can be started first, followed by the Frame Buffer write access (PSDU data); refer to Figure 10-3 on page 127. This is applicable for time critical applications.

Initiating a transmission, either by asserting pin 11 (SLP_TR) or command TX_START to register bits TRX_CMD (register 0x02, TRX_STATE), the radio transceiver starts transmitting the SHR, which is internally generated.

This first phase requires 16 µs for PLL settling and 160 µs for SHR transmission. The PHR must be available in the Frame Buffer before this time elapses. Furthermore the SPI data rate must be higher than the PHY data rate selected by register bits OQPSK_DATA_RATE (register 0x0C, TRX_CTRL_2) to ensure that no Frame Buffer under run occurs, indicated by IRQ_6 (TRX_UR), refer to Section 11.3 "High Data Rate Modes" on page 137.

Figure 10-3. Time Optimized Frame Transmit Procedure
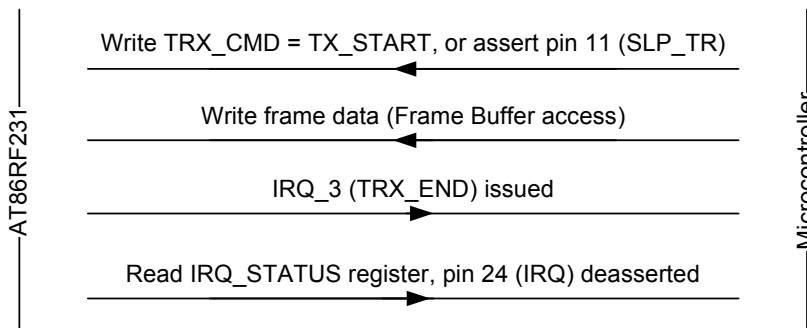
11. AT86RF231 Extended Feature Set

11.1 Security Module (AES)

The security module (AES) is characterized by:

- Hardware accelerated encryption and decryption
- Compatible with AES-128 standard (128-bit key and data block size)
- ECB (encryption/decryption) mode and CBC (encryption) mode support
- Stand-alone operation, independent of other blocks

11.1.1 Overview

The security module is based on an AES-128 core according to FIPS197 standard, refer to [5]. The security module works independent of other building blocks of the AT86RF231, encryption and decryption can be performed in parallel to a frame transmission or reception.

Controlling the security block is implemented as an SRAM access to address space 0x82 to 0x94. A Fast SRAM access mode allows simultaneously writing new data and reading data from previously processed data within the same SPI transfer. This access procedure is used to reduce the turnaround time for ECB mode, see Section 11.1.5 "Data Transfer - Fast SRAM Access" on page 132.

In addition, the security module contains another 128-bit register to store the initial key used for security operations. This initial key is not modified by the security module.

11.1.2 Security Module Preparation

The use of the security module requires a configuration of the security engine before starting a security operation. The following steps are required:

Table 11-1. AES Engine Configuration Steps

Step	Description	Description	Section
1	Key Setup	Write encryption or decryption key to SRAM	Section 11.1.3
2	AES Mode	Select AES mode: ECB or CBC Select encryption or decryption	Section 11.1.4.1 Section 11.1.4.2
3	Write Data	Write plaintext or cipher text to SRAM	Section 11.1.5
4	Start Operation	Start AES operation	
5	Read Data	Read cipher text or plaintext from SRAM	Section 11.1.5

Before starting any security operation a key must be written to the security engine, refer to Section 11.1.3 "Security Key Setup" on page 129. The key set up requires the configuration of the AES engine KEY mode using register bits AES_MODE (SRAM address 0x83, AES_CTRL).

The following step selects the AES mode, either electronic code book (ECB) or cipher block chaining (CBC). These modes are explained more in detail in sections Section 11.1.4 "Security Operation Modes" on page 129. Further, encryption or decryption must be selected with register bit AES_DIR (SRAM address 0x83, AES_CTRL).

As next the 128-bit plain text or ciphertext data has to be provided to the AES hardware engine. The data uses the SRAM address range 0x84 - 0x93.

The encryption or decryption is initiated with register bit AES_REQUEST = 1 (SRAM address 0x83, AES_CTRL or the mirrored version with SRAM address 0x94, AES_CTRL_MIRROR).

The AES module control registers are only accessible using SRAM read and write accesses on address space 0x82 to 0x94. A configuration of the AES mode, providing the data and the start of the operation can be combined within one SRAM access.

Notes

- No additional register access is required to operate the security block.
- Using AES in TRX_OFF state requires an activated clock at pin 17 (CLKM), i.e. register bits CLKM_CTRL!= 0. For further details refer to Section 9.6.4 "Master Clock Signal Output (CLKM)" on page 117.
- Access to the security block is not possible while the radio transceiver is in state SLEEP.
- All configurations of the security module, the SRAM content and keys are reset during SLEEP or RESET states.

11.1.3 Security Key Setup

The setup of the key is prepared by setting register bits AES_MODE = 0x1 (SRAM address 0x83, AES_CTRL). Afterwards the 128 bit key must be written to SRAM addresses 0x84 through 0x93 (registers AES_KEY). It is recommended to combine the setting of control register 0x83 (AES_CTRL) and the 128 bit key transfer using only one SRAM access starting from address 0x83.

The address space for the 128-bit key and 128-bit data is identical from programming point of view. However, both use different pages which are selected by register bit AES_MODE before storing the data.

A read access to registers AES_KEY (0x84 - 0x93) returns the last round key of the preceding security operation. After an ECB encryption operation, this is the key that is required for the corresponding ECB decryption operation. However, the initial AES key, written to the security module in advance of an AES run, see step 1 in Table 11-1 on page 128, is not modified during an AES operation. This initial key is used for the next AES run even it cannot be read from AES_KEY.

Note

- ECB decryption is not required for IEEE 802.15.4 or ZigBee security processing. The AT86RF231 provides this functionality as an additional feature.

11.1.4 Security Operation Modes

11.1.4.1 *Electronic Code Book (ECB)*

ECB is the basic operating mode of the security module. After setting up the initial AES key, register bits AES_MODE = 0 (SRAM address 0x83, AES_CTRL) sets up ECB mode. Register bit AES_DIR (SRAM address 0x83, AES_CTRL) selects the direction, either encryption or decryption. The data to be processed has to be written to SRAM addresses 0x84 through 0x93 (registers AES_STATE).

An example for a programming sequence is shown in Figure 11-1 on page 130. This example assumes a suitable key has been loaded before.

A security operation can be started within one SRAM access by appending the start command AES_REQUEST = 1 (register 0x94, AES_CTRL_MIRROR) to the SPI sequence. Register AES_CTRL_MIRROR is a mirrored version of register 0x83 (AES_CTRL).

Figure 11-1. ECB Programming SPI Sequence - Encryption
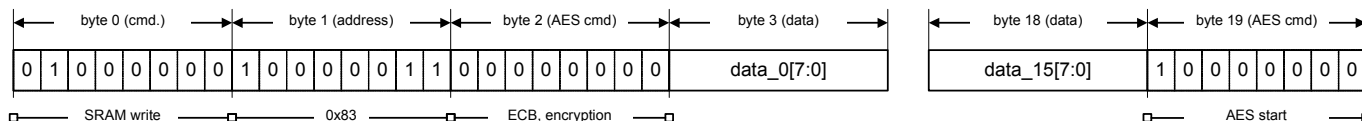
Summarizing, the following steps are required to perform a security operation using only one SPI access:

1. Configure SPI Access	a) SRAM Write, refer to Section 6.2.3
	b) Start Address 0x83
2. Configure AES Operation	Address 0x83: select ECB mode, direction
3. Write 128-bit data block	Addresses 0x84 - 0x93: either plain or ciphertext
4. Start AES Operation	Addresses 0x94: start AES operation, ECB mode

This sequence is recommended because the security operation is configured and started within one SPI transaction.

The ECB encryption operation is illustrated in Figure 11-2 on page 130. Figure 11-3 on page 130 shows the ECB decryption mode, which is supported in a similar way.

Figure 11-2. ECB Mode - Encryption
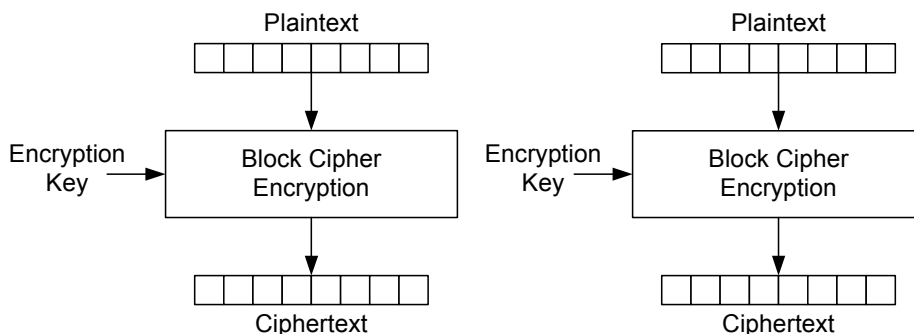
Figure 11-3. ECB Mode - Decryption
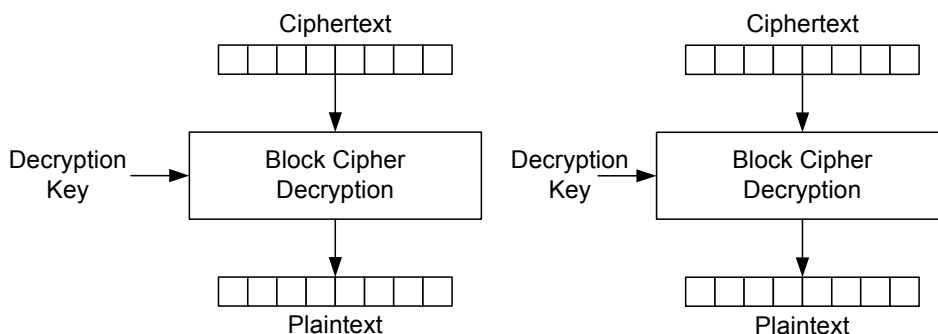
When decrypting, due to the nature of AES algorithm, the initial key to be used is not the same as the one used for encryption, but rather the last round key instead. This last round key is the content of the key address space stored after running one full encryption cycle, and must be saved for decryption. If the decryption key has not been saved, it has to be recomputed by first running a dummy encryption (of an arbitrary plaintext) using the original encryption key, then fetching the resulting round key from the key memory, and writing it back into the key memory as the decryption key.

ECB decryption is not used by either IEEE 802.15.4 or ZigBee frame security. Both of these standards do not directly encrypt the payload, but rather a nonce instead, and protect the payload by applying an XOR operation between the resulting (AES-) cipher text and the original payload. As the nonce is the same for encryption and decryption only ECB encryption is required. Decryption is performed by XORing the received cipher text with its own encryption result respectively, which results in the original plaintext payload upon success.

11.1.4.2 Cipher Block Chaining (CBC)

In CBC mode, the result of a previous AES operation is XORed with the new incoming vector, forming the new plaintext to encrypt, see Figure 11-4 on page 131. This mode is used for the computation of a cryptographic checksum (message integrity code, MIC).

Figure 11-4. CBC Mode - Encryption
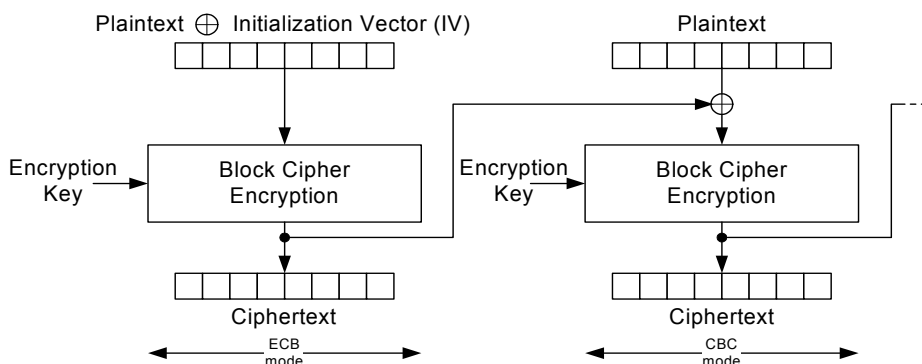
After preparing the AES key, and defining the AES operation direction using SRAM register bit AES_DIR, the data has to be provided to the AES engine and the CBC operation can be started.

The first CBC run has to be configured as ECB to process the initial data (plaintext XORed with an initialization vector provided by the microcontroller). All succeeding AES runs are to be configured as CBC by setting register bits AES_MODE = 0x2 (register 0x83, AES_CTRL). Register bit AES_DIR (register 0x83, AES_CTRL) must be set to AES_DIR = 0 to enable AES encryption. The data to be processed has to be transferred to the SRAM starting with address 0x84 to 0x93 (register AES_STATE). Setting register bit AES_REQUEST = 1 (register 0x94, AES_CTRL_MIRROR) as described in Section 11.1.4 "Security Operation Modes" on page 129 starts the first encryption within one SRAM access. This causes the next 128 bits of plaintext data to be XORed with the previous cipher text data, see Figure 11-4 on page 131.

According to IEEE 802.15.4 the input for the very first CBC operation has to be prepared by a XORing a plaintext with an initialization vector (IV). The value of the initialization vector is 0. However, for non-compliant usage any other initialization vector can be used. This operation has to be prepared by the microcontroller.

Note that IEEE 802.15.4-2006 standard MIC algorithm requires CBC mode encryption only, as it implements a one-way hash function.

11.1.5   Data Transfer - Fast SRAM Access

The ECB and CBC modules including the AES core are clocked with 16 MHz. One AES operation takes 24 µs to execute, refer to parameter 12.4.15 in Section 12.4 "Digital Interface Timing Characteristics" on page 157. That means that the processing of the data is usually faster than the transfer of the data via the SPI interface.

To reduce the overall processing time the AT86RF231 provides a Fast SRAM access for the address space 0x82 to 0x94.

Figure 11-5.   Packet Structure - Fast SRAM Access Mode
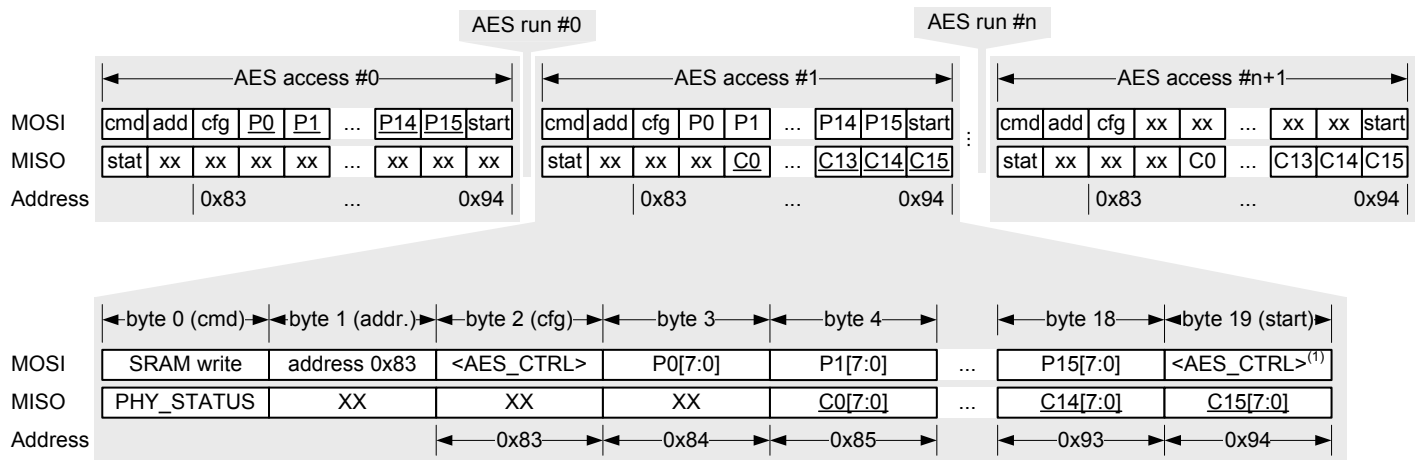
Note: Byte 19 is the mirrored version of register AES_CTRL on SRAM address 0x94, see register description AES_CTRL_MIRROR for details.

In contrast to a standard SRAM access, refer to Section 6.2.3 "SRAM Access Mode" on page 22, the Fast SRAM access allows writing and reading of data simultaneously during one SPI access for consecutive AES operations *(AES run)*.

For each byte P0 transferred to pin 22 (MOSI) for example in *"AES access #1"*, see Figure 11-5 on page 132 (lower part), the previous content of the respective AES register C0 is clocked out at pin 20 (MISO) with an offset of one byte.

In the example shown in Figure 11-5 on page 132 the initial plaintext P0 - P15 is written to the SRAM within *"AES access #0"*. The last command on address 0x94 (AES_CTRL_MIRROR) starts the AES operation (*"AES run #0"*). In the next *"AES access #1"* new plaintext data P0 - P15 is written to the SRAM for the second AES run, in parallel the ciphertext C0 - C15 from the first AES run is clocked out at pin MISO. To read the ciphertext from the last *"AES run #(n)"* one dummy *"AES access #(n+1)"* is needed.

Note that the SRAM write access always overwrites the previous processing result.

The Fast SRAM access automatically applies to all write operations to SRAM addresses 0x82 to 0x94.

11.1.6   Start of Security Operation and Status

A security operation is started within one SRAM access by appending the start command AES_REQUEST = 1 (register 0x94, AES_CTRL_MIRROR) to the SPI sequence. Register AES_CTRL_MIRROR is a mirrored version of register 0x83 (AES_CTRL).

The status of the security processing is indicated by register 0x82 (AES_STATUS). After 24 µs AES processing time register bit AES_DONE changes to 1 (register 0x82, AES_STATUS) indicating that the security operation has finished, see parameter 12.4.15 in Section 12.4 "Digital Interface Timing Characteristics" on page 157.

11.1.7   SRAM Register Summary

The following registers are required to control the security module:

Table 11-2.   SRAM Security Module Address Space Overview

SRAM-Addr.	Register Name	Description
0x80 - 0x81		Reserved, not available
0x82	AES_STATUS	AES Status
0x83	AES_CTRL	Security Module Control, AES Mode
0x84 - 0x93	AES_KEY AES_STATE	Depends on AES_MODE setting: AES_MODE = 1: - Contains AES_KEY (key) AES_MODE = 0 | 2: - Contains AES_STATE (128-bit data block)
0x94	AES_CTRL_MIRROR	Mirror of register 0x83 (AES_CTRL)
0x95 - 0xFF		Reserved, not available

These registers are only accessible using SRAM write and read accesses, for details refer to Section 6.2.3 "SRAM Access Mode" on page 22. Note, that the SRAM register are reset when entering the SLEEP state.

11.1.8   AES SRAM Configuration Register

Register 0x82 (AES_STATUS):

This read-only register signals the status of the security module and operation.

Bit	7	6	5	4	3	2	1	0	
+0x82	**AES_ER**			Reserved				**AES_DONE**	AES_STATUS
Read/Write	R	R	R	R	R	R	R	R	
Reset Value	0	0	0	0	0	0	0	0	

- **Bit 7 - AES_ER**

This SRAM register bit indicates an error of the AES module. An error may occur for instance after an access to SRAM register 0x83 (AES_CTRL) while an AES operation is running or after reading less than 128 bits from SRAM register space 0x84 - 0x93 (AES_STATE).

Table 11-3. AES Core Operation Status

Register Bit	Value	Description
AES_ER	<u>0</u>	No error of the AES module
	1	AES module error

- **Bit [6:1] -Reserved**

- **Bit 0 - AES_DONE**

Table 11-4. AES Core Operation Status

Register Bit	Value	Description
AES_DONE	<u>0</u>	AES Module is not finished
	1	AES module has finished

Register 0x83 (AES_CTRL):

This register controls the operation of the security module. Do not access this register during AES operation to read the AES core status. A read or write access during AES operation stops the actual processing.

To read the AES status use register bit AES_DONE (register 0x82, AES_STATUS).

Bit	7	6	5	4	3	2	1	0	
+0x83	AES_REQUEST	AES_MODE			AES_DIR	Reserved			AES_CTRL
Read/Write	W	R/W	R/W	R/W	R/W	R	R	R	
Reset Value	0	0	0	0	0	0	0	0	

- **Bit 7 - AES_REQUEST**
A write access with AES_REQUEST = 1 initiates the AES operation.

Table 11-5. AES Core Status

Register Bit	Value	Description
AES_REQUEST	<u>0</u>	Security module, AES core idle
	1	Write access: Start security module

- **Bit [6:4] - AES_MODE**
This register bit sets the AES operation mode.

Table 11-6. AES Mode

Register Bit	Value	Description
AES_MODE	<u>0</u>	ECB mode, refer to Section 11.1.4.1
	1	KEY mode, refer to Section 11.1.3
	2	CBC mode, refer to Section 11.1.4.2
	3 - 7	Reserved

• **Bits 3 - AES_DIR**

This register bit sets the AES operation direction, either encryption or decryption.

Table 11-7. AES Direction

Register Bit	Value	Description
AES_DIR	<u>0</u>	AES encryption (ECB, CBC)
	1	AES decryption

• **Bit [2:0] - Reserved**

Register 0x94 (AES_CTRL_MIRROR):

Register 0x94 is a mirrored version of register 0x83 (AES_CTRL), for details refer to register 0x83 (AES_CTRL).

Bit	7	6	5	4	3	2	1	0	
+0x83	AES_REQUEST	AES_MODE			AES_DIR	Reserved			AES_CTRL
Read/Write	W	R/W	R/W	R/W	R/W	R	R	R	
Reset Value	0	0	0	0	0	0	0	0	

This register could be used to start a security operation within a single SRAM access by appending it to the data stream and setting register bit AES_REQUEST = 1.

11.2 Random Number Generator

11.2.1 Overview

The AT86RF231 incorporates a 2-bit truly random number generator by observation of noise. This random number can be used to:

- Generate random seeds for CSMA-CA algorithm   see Section 7.2
- Generate random values for AES key generation   see Section 11.1

The random number is updated every $t_{TR29} = 1$ µs in Basic Operation Mode receive states. The values are stored in register bits RND_VALUE (register 0x06, PHY_RSSI).

11.2.2 Register Description

Register 0x06 (PHY_RSSI):

Register 0x06 (PHY_RSSI) is a multi purpose register to indicate FCS validity, to provide random numbers and an RSSI value.

Bit	7	6	5	4	3	2	1	0	
+0x06	RX_CRC_VALID	RND_VALUE		RSSI					PHY_RSSI
Read/Write	R	R	R	R	R	R	R	R	
Reset Value	0	0	0	0	0	0	0	0	

- **Bit 7 - RX_CRC_VALID**

Refer to register description in Section 8.2.5 "Register Description" on page 87.

- **Bit [6:5] - RND_VALUE**

The 2-bit random value can be retrieved by reading register bits RND_VALUE. Note that the radio transceiver shall be in Basic Operating Mode receive state. The values are updated each $t_{TR29} = 1$ µs.

- **Bit [4:0] - RSSI**

Refer to register description in Section 8.3.4 "Register Description" on page 90.

Note: Ensure that register bit RX_PDT_DIS (register 0x15, RX_SYN) is set to 0 at least 1 µs before reading a random value.

11.3 High Data Rate Modes

The main features are:

- High Data Rate Transmission up to 2 Mb/s.
- Support of Basic and Extended Operating Mode
- Support of other features of the Extended Feature Set
- Reduced ACK timing (optional)

11.3.1 Overview

The AT86RF231 also supports alternative data rates, higher than 250 kb/s for applications beyond IEEE 802.15.4 compliant networks.

The selection of a data rate does not affect the remaining functionality. Thus it is possible to run all features and operating modes of the radio transceiver in various combinations.

The data rate can be selected by writing to register bits OQPSK_DATA_RATE (register 0x0C, TRX_CTRL_2).

The High Data Rate Modes occupy the same RF channel bandwidth as the IEEE 802.15.4-2.4 GHz 250 kb/s standard mode. Due to the decreased spreading factor, the sensitivity of the receiver is reduced accordingly. Table 11-8 on page 137 shows typical values of the sensitivity for different data rates.

Table 11-8. High Data Rate Sensitivity

High Data Rate	Sensitivity	Comment
250 kb/s	-101 dBm	PER $\leq$ 1%, PSDU length of 20 octets
500 kb/s	-97 dBm	PER $\leq$ 1%, PSDU length of 20 octets
1000 kb/s	-95 dBm	PER $\leq$ 1%, PSDU length of 20 octets
2000 kb/s	-89 dBm	PER $\leq$ 1%, PSDU length of 20 octets

By default there is no header based signaling of the data rate within a transmitted frame. Thus nodes using a data rate other than the default IEEE 802.15.4 data rate of 250 kb/s are to be configured in advance and consistently. Alternatively the configurable start of frame delimiter (SFD) could be used as an indicator of the PHY data rate, see Section 11.9 "Configurable Start-Of-Frame Delimiter" on page 155.

11.3.2 High Data Rate Packet Structure

In order to allow appropriate frame synchronization, higher data rate modulation is restricted to the payload octets only. The SHR and the PHR field are transmitted with the IEEE 802.15.4 compliant data rate of 250 kb/s, refer to Section 8.1.1 "PHY Protocol Layer Data Unit (PPDU)" on page 79.

A comparison of the general packet structure for different data rates with an example PSDU length of 80 octets is shown in Figure 11-6 on page 138.

Figure 11-6. High Data Rate Frame Structure
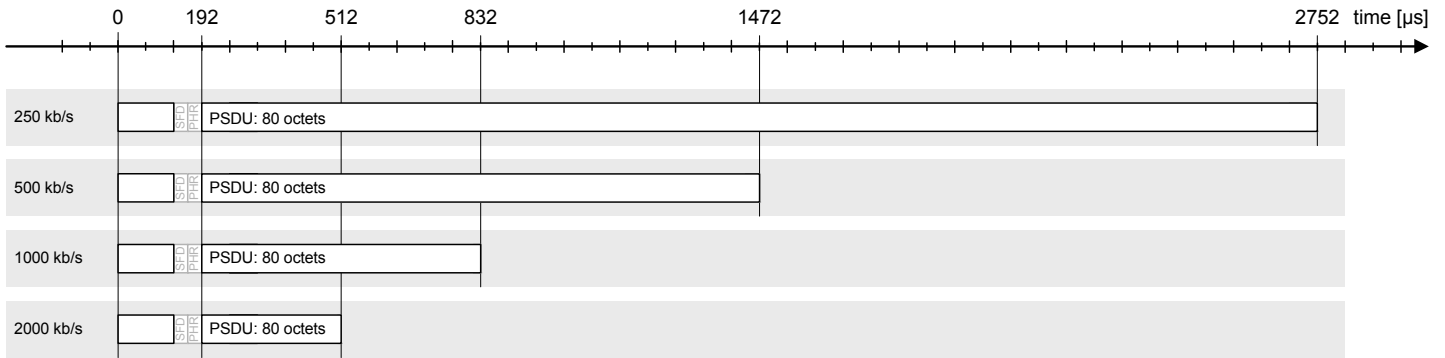
Due to the overhead caused by the SHR, PHR as well as the FCS, the effective data rate is lower than the selected data rate. This is also affected by the length of the PSDU. A graphical representation of the effective PSDU data rate is shown in Figure 11-7 on page 138.

Figure 11-7. Effective Data Rate "B" for High Data Rate Mode
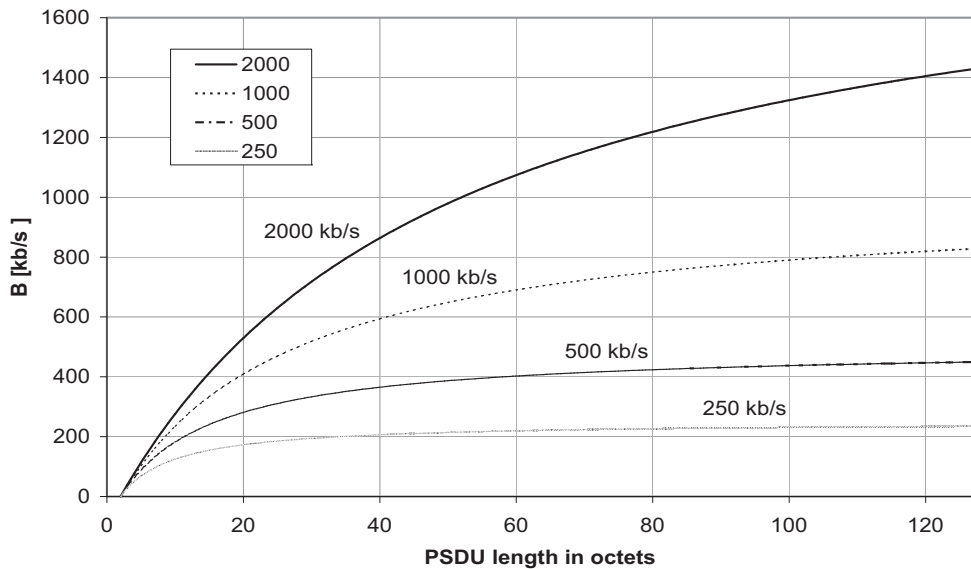
The effective throughput is further affected by the MAC overhead, the acknowledgment scheme as well as the MCU processing capability. Consequently, High Data Rate transmission and reception is useful for large PSDU lengths due to the higher effective data rate, or to reduce the power consumption of the system. When using High Data Rate Modes the active on-air time is significantly reduced.

11.3.3 High Data Rate Frame Buffer Access

The Frame Buffer access to read or write frames for High Data Rate transmission is similar to the procedure described in Section 6.2.2 "Frame Buffer Access Mode" on page 20. However,

during Frame Buffer read access the last byte transferred after the PSDU data is the ED value rather than the LQI value.

Figure 11-8 on page 139 illustrates the packet structure of a High Data Rate Frame Buffer read access.

Figure 11-8. Packet Structure - High Data Rate Frame Buffer Read Access

	byte 1 (command byte)	byte 2 (data byte)	byte 3 (data byte)		byte n-1 (data byte)	byte n (data byte)
MOSI	0 0 1 reserved[5:0]	XX	XX	...	XX	XX
MISO	PHY_STATUS	PHR[7:0]	PSDU[7:0]	...	PSDU[7:0]	ED[7:0]
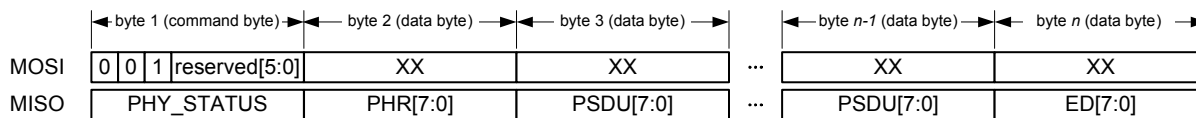
11.3.4 High Data Rate Energy Detection

According to IEEE 802.15.4 the ED measurement duration is 8 symbol periods. For frames operated at higher data rates the automated ED measurement duration is reduced to 32 µs to take the reduced frame length into account, refer to Section 8.4 "Energy Detection (ED)" on page 91.

During Frame Buffer read access the ED value is appended to the PSDU data, refer to Section 11.3.3 "High Data Rate Frame Buffer Access" on page 138.

11.3.5 High Data Rate Mode Options

Receiver Sensitivity Control

The different data rates between PPDU header (SHR and PHR) and PHY payload (PSDU) cause a different sensitivity between header and payload. This can be adjusted by defining sensitivity threshold levels of the receiver. With a sensitivity threshold level set (register bits RX_PDT_LEVEL > 0), the receiver does not receive frames with an RSSI level below that threshold. Under these operating conditions the receiver current consumption is reduced by about 500 µA, refer to Section 12.8 "Current Consumption Specifications" on page 161 parameter 12.8.4.

Enabling receiver sensitivity control with at least RX_PDT_LEVEL = 1 is recommended for the 2 Mb/s rate with a PSDU sensitivity of -89 dBm. In the case of receiving with the default setting of RX_PDT_LEVEL, a high data rate frame may be detected even if the PSDU sensitivity is above the received signal strength. In this case the frame is rejected.

A description of the settings to control the sensitivity threshold with register 0x15 (RX_SYN) can be found in Section 9.1.4 "Register Description" on page 103.

Reduced Acknowledgment Timing

On higher data rates the IEEE 802.15.4 compliant acknowledgment frame response time of 192 µs significantly reduces the effective data rate of the network. To minimize this influence in Extended Operating Mode RX_AACK, refer to Section 7.2.3 "RX_AACK_ON - Receive with Automatic ACK" on page 51, the acknowledgment frame response time can be reduced to 32 µs. Figure 11-9 on page 140 illustrates an example for a reception and acknowledgement of a frame with a data rate of 2000 kb/s and a PSDU length of 80 symbols. The PSDU length of the acknowledgment frame is 5 octets according to IEEE 802.15.4.

Figure 11-9. High Data Rate AACK Timing
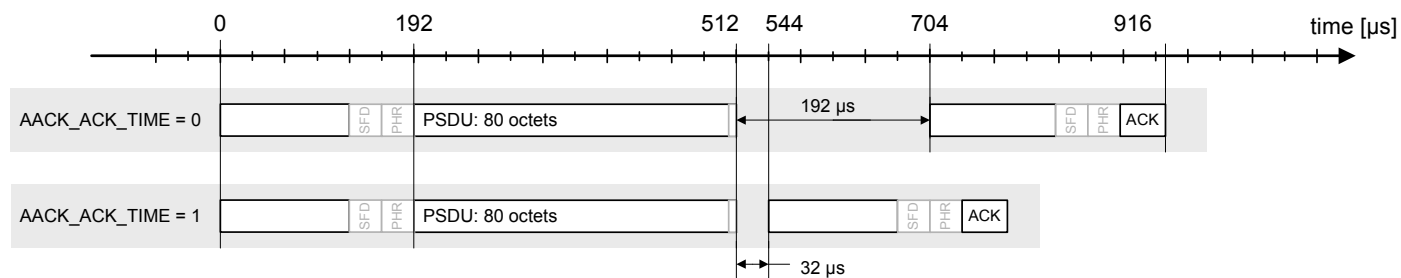
If register bit AACK_ACK_TIME (register 0x17, XAH_CTRL_1) is set the acknowledgment time is reduced from 192 µs to 32 µs.

11.3.6 Register Description

Register 0x0C (TRX_CTRL_2):

The TRX_CTRL_2 register controls the data rate setting

Bit	7	6	5	4	3	2	1	0	
+0x0C	RX_SAFE_MODE	Reserved					OQPSK_DATA_RATE		TRX_CTRL_2
Read/Write	R/W	R	R	R	R	R	R/W	R/W	
Reset Value	0	0	0	0	0	0	0	0	

- **Bit 7 - RX_SAFE_MODE**
Refer to Section 11.8.2 "Register Description" on page 154.

- **Bit [6:2] - Reserved**

- **Bit [1:0] - OQPSK_DATA_RATE**
A write access to these register bits sets the OQPSK PSDU data rate used by the radio transceiver. The reset value OQPSK_DATA_RATE = 0 is the PSDU data rate according to IEEE 802.15.4.

Table 11-9. OQPSK Data Rate

Register Bits	Value	OQPSK Data Rate	Comment
OQPSK_DATA_RATE	0	250 kb/s	IEEE 802.15.4 compliant
	1	500 kb/s	
	2	1000 kb/s	
	3	2000 kb/s	

Register 0x17 (XAH_CTRL_1):

The XAH_CTRL_1 register is a multi-purpose control register for various RX_AACK settings.

Bit	7	6	5	4	3	2	1	0	
+0x17	Reserved		AACK_FLTR_RES_FT	AACK_UPLD_RES_FT	Reserved	AACK_ACK_TIME	AACK_PROM_MODE	Reserved	XAH_CTRL_1
Read/Write	R/W	R	R/W	R/W	R	R/W	R/W	R	
Reset Value	0	0	1	0	0	0	0	0	

- **Bit [7:6] - Reserved**

- **Bit 5 - AACK_FLTR_RES_FT**

Refer to 7.2.7 "Register Description - Control Registers" on page 68.

- **Bit 4 - AACK_UPLD_RES_FT**

Refer to Section 7.2.7 "Register Description - Control Registers" on page 68.

- **Bit 3 - Reserved**

- **Bit 2 - AACK_ACK_TIME**

According to IEEE 802.15.4, section 7.5.6.4.2 the transmission of an acknowledgment frame shall commence 12 symbol periods *(aTurnaroundTime)* after the reception of the last symbol of a data or MAC command frame. This is fulfilled with the reset value of the register bit [2] (AACK_ACK_TIME).

If AACK_ACK_TIME = 1 an acknowledgment frame is sent 32 µs after the reception of the last symbol of a data or MAC command frame. This may be applied to proprietary networks including networks using the High Data Rate Modes to improve the overall data throughput.

- **Bit 1 - AACK_PROM_MODE**

Refer to Section 7.2.7 "Register Description - Control Registers" on page 68.

- **Bit 0 - Reserved**

11.4 Antenna Diversity

The Antenna Diversity implementation is characterized by:

- Improves signal path robustness between nodes
- AT86RF231 self-contained antenna diversity algorithm
- Direct register based antenna selection

11.4.1 Overview

Due to multipath propagation effects between network nodes, the receive signal strength may vary and affect the link quality, even for small changes of the antenna location. These fading effects can result in an increased error floor or loss of the connection between devices.

To improve the reliability of an RF connection between network nodes Antenna Diversity can be applied to reduce effects of multipath propagation and fading. Antenna Diversity uses two antennas to select the most reliable RF signal path. This is done by the radio transceiver during preamble field search without the need for microcontroller interaction. To ensure highly independent receive signals on both antennas, the antennas should be carefully separated from each other.

If a preamble field is detected on one antenna, this antenna is selected for reception. Otherwise the search is continued on the other antenna and vice versa.

Antenna Diversity can be used in Basic and Extended Operating Modes and can also be combined with other features and operating modes like High Data Rate Mode and RX/TX Indication.

11.4.2 Antenna Diversity Application Example

A block diagram for an application using an antenna switch is shown in .

Figure 11-10. Antenna Diversity - Block Diagram
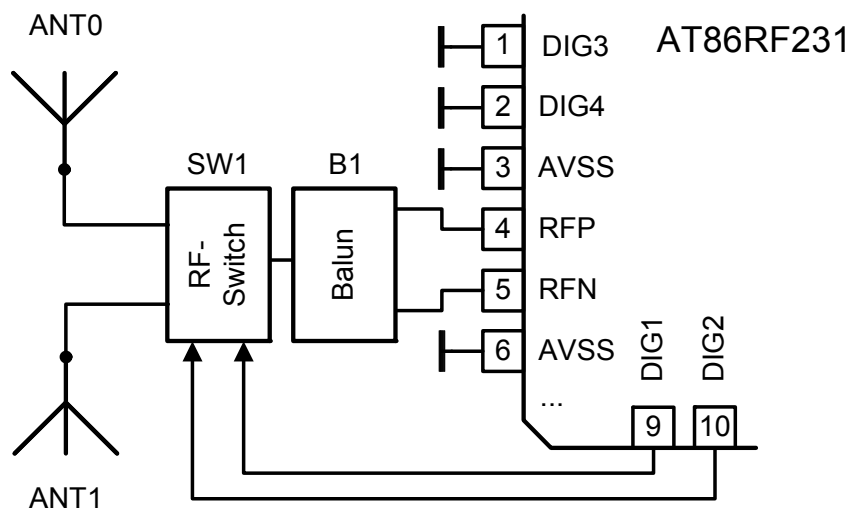
Generally, the Antenna Diversity algorithm is enabled with register bit ANT_DIV_EN (register 0x0D, ANT_DIV) set. In this case the control of an antenna diversity switch must be enabled by register bit ANT_EXT_SW_EN (register 0x0D, ANT_DIV). The internal connection to digital ground of the control pins pin 9 (DIG1) and pin 10 (DIG2) is disabled (refer to section 4.2), and they feed the antenna switch signal and its inverse to the differential inputs of the RF Switch (SW1).

Upon reception of a frame the AT86RF231 selects one antenna during preamble field detection. The selected antenna is then indicated by register bit ANT_SEL (register 0x0D, ANT_DIV). After the frame reception is completed, the antenna selection continues searching for new frames on both antennas. However, the register bit ANT_SEL maintains its previous value (from the last received frame) until a new SHR has been found, and the selection algorithm locked into one antenna again. At this time the register bit ANT_SEL is updated again.

For transmission the antenna defined by register bits ANT_CTRL (register 0x0D, ANT_DIV) is selected. If for example the same antenna is to be used for transmission as being selected for reception, the antenna must be set using register bits ANT_CTRL, based on the value read from register bit ANT_SEL. It is recommended to read register bit ANT_SEL after IRQ_2 (RX_START).

The autonomous search and selection allows the use of Antenna Diversity during reception even if the microcontroller does currently not control the radio transceiver, for instance in Extended Operating Mode.

A microcontroller defined selection of a certain antenna can be done by disabling the automated Antenna Diversity algorithm (ANT_DIV_EN = 0) and selecting one antenna using register bit ANT_CTRL.

If the AT86RF231 is not in a receive or transmit state, it is recommended to disable register bit ANT_EXT_SW_EN to reduce the power consumption or avoid leakage current of an external RF switch, especially during SLEEP state. If register bit ANT_EXT_SW_EN = 0, output pins DIG1/DIG2 are pulled-down to digital ground.

11.4.3 Antenna Diversity Sensitivity Control

Due to a different receive algorithm used by the Antenna Diversity algorithm, the correlator threshold of the receiver has to be adjusted. It is recommended to set register bits PDT_THRES (register 0x0A, RX_CTRL) to 3.

11.4.4 Register Description

Register 0x0A (RX_CTRL):

The RX_CTRL controls the sensitivity of the Antenna Diversity Mode

Bit	7	6	5	4	3	2	1	0	
+0x0A	Reserved				PDT_THRES				RX_CTRL
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset Value	1	0	1	1	0	1	1	1	

- **Bit [7:4] - Reserved**

- **Bit [3:0] - PDT_THRES**

These register bits control the sensitivity of the receiver correlation unit. If the Antenna Diversity algorithm is enabled (ANT_DIV_EN = 1), the value shall be set to PDT_THRES = 3, otherwise it shall be set back to the reset value. This is not automatically done by the hardware.

Table 11-10. Receiver Sensitivity Control

Register Bit	Value	Description
PDT_THRES	0x7	Reset value, to be used if Antenna Diversity algorithm is disabled
	0x3	Recommended correlator threshold for Antenna Diversity operation
	Other	Reserved

Register 0x0D (ANT_DIV):

The ANT_DIV register controls Antenna Diversity.

Bit	7	6	5	4	3	2	1	0	
+0x0D	ANT_SEL	Reserved			ANT_DIV_EN	ANT_EXT_SW_EN	ANT_CTRL		ANT_DIV
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Reset Value	0	0	0	0	0	0	1	1	

- **Bit 7 - ANT_SEL**

This register bit signals the currently selected antenna path. The selection may be based either on the last antenna diversity cycle (ANT_DIV_EN = 1) or on the content of register bits ANT_CTRL, for details refer to Section 11.4.2 "Antenna Diversity Application Example" on page 142.

Table 11-11. Antenna Diversity - Antenna Status

Register Bit	Value	Description
ANT_SEL	0	Antenna 0
	1	Antenna 1

- **Bit [6:4] - Reserved**

- **Bit 3 - ANT_DIV_EN**

If register bit ANT_DIV_EN is set, the Antenna Diversity algorithm is enabled. On reception of a frame the algorithm selects an antenna autonomously during SHR search. This selection is kept until:

- A new SHR search starts
- Leaving receive states
- Manually programmed register bits ANT_CTRL

Table 11-12. Antenna Diversity Control

Register Bit	Value	Description
ANT_DIV_EN	<u>0</u>	Antenna Diversity algorithm disabled
	1	Antenna Diversity algorithm enabled

Note: If ANT_DIV_EN = 1 register bit ANT_EXT_SW_EN shall be set to 1, too. This is not automatically done by the hardware.

- **Bit 2 - ANT_EXT_SW_EN**

If enabled, pin 9 (DIG1) and pin 10 (DIG2) become output pins and provide a differential control signal for an Antenna Diversity switch. The selection of a specific antenna is done either by the automated Antenna Diversity algorithm (ANT_DIV_EN = 1), or according to register bits ANT_CTRL if Antenna Diversity algorithm is disabled.

Do not enable Antenna Diversity RF switch control (ANT_EXT_SW_EN = 1) and RX Frame Time Stamping (IRQ_2_EXT_EN = 1) at the same time, see Section 11.6 "RX Frame Time Stamping" on page 150.

If the register bit is set the control pins DIG1/DIG2 are activated in all radio transceiver states as long as register bit ANT_EXT_SW_EN is set. If the AT86RF231 is not in a receive or transmit state, it is recommended to disable register bit ANT_EXT_SW_EN to reduce the power consumption or avoid leakage current of an external RF switch, especially during SLEEP state. If register bit ANT_EXT_SW_EN = 0, output pins DIG1 and DIG2 are pulled-down to digital ground.

Table 11-13. Antenna Diversity RF Switch Enable

Register Bit	Value	Description
ANT_EXT_SW_EN	<u>0</u>	Antenna Diversity RF Switch Control disabled
	1	Antenna Diversity RF Switch Control enabled

Note: If ANT_EXT_SW_EN = 0, register bit ANT_DIV_EN shall be set to 0 and register bits ANT_CTRL to 3. This is not automatically done by the hardware.

- **Bit [1:0] - ANT_CTRL**

These register bits provide a static control of an Antenna Diversity switch. Setting ANT_DIV_EN = 0 (Antenna Diversity disabled), this register setting defines the selected antenna. Although it is possible to change register bits ANT_CTRL in state TRX_OFF, this change will be effective at pins DIG1 and DIG2 in state PLL_ON as well as all receive and transmit states.

Table 11-14. Antenna Diversity Switch Control

Register Bit	Value	Description

Table 11-14. Antenna Diversity Switch Control

ANT_CTRL	0	Reserved
	1	Antenna 1 DIG1 = L DIG2 = H
	2	Antenna 0 DIG1 = H DIG2 = L
	<u>3</u>	Default value for ANT_EXT_SW_EN = 0. Mandatory setting for applications not using Antenna Diversity.

Note: Register values 1 and 2 are valid for ANT_EXT_SW_EN = 1.

11.5 RX/TX Indicator

The main features are:

- RX/TX Indicator to control an external RF Front-End
- Microcontroller independent RF Front-End Control
- Provide TX Timing Information

11.5.1 Overview

While IEEE 802.15.4 is a low cost, low power standard, solutions supporting higher transmit output power are occasionally desirable. To simplify the control of an optional external RF front-end, a differential control pin pair can indicate that the AT86RF231 is currently in transmit mode.

The control of an external RF front-end is done via digital control pins DIG3/DIG4. The function of this pin pair is enabled with register bit PA_EXT_EN (register 0x04, TRX_CTRL_1). While the transmitter is turned off pin 1 (DIG3) is set to low level and pin 2 (DIG4) to high level. If the radio transceiver starts to transmit, the two pins change the polarity. This differential pin pair can be used to control PA, LNA, and RF switches.

If the AT86RF231 is not in a receive or transmit state, it is recommended to disable register bit PA_EXT_EN (register 0x04, TRX_CTRL_1) to reduce the power consumption or avoid leakage current of external RF switches and other building blocks, especially during SLEEP state. If register bits PA_EXT_EN = 0, output pins DIG3/DIG4 are pulled-down to analog ground.

11.5.2 External RF-Front End Control

Using an external RF front-end including a power amplifier (PA) it may be required to adjust the setup time of the external PA relative to the internal building blocks to optimize the overall power spectral density (PSD) mask.

Figure 11-11. TX Power Ramping Control for RF Front-Ends
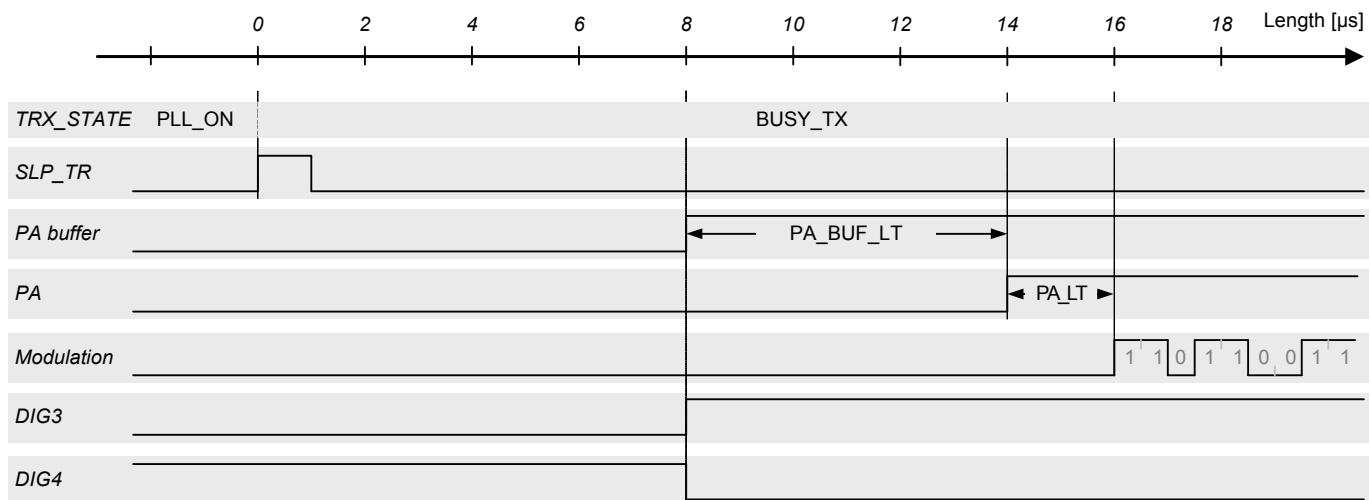
The start-up sequence of the individual building blocks of the internal transmitter is shown in Figure 11-11 on page 147, where transmission is actually initiated by the rising edge of pin 11 (SLP_TR). The radio transceiver state changes from PLL_ON to BUSY_TX and the PLL settles

to the transmit frequency within 16 µs. The modulation starts 16 µs after the rising edge of SLP_TR. During this time, the PA buffer and the internal PA are enabled.

The control of an external PA is done via differential pin pair DIG3/DIG4. DIG3 = H / DIG4 = L indicates that the transmission starts and can be used to enable an external PA. The timing of pins DIG3/DIG4 can be adjusted relative to the start of the frame and the activation of the internal PA buffer. This is controlled using register bits PA_BUF_LT and PA_LT. For details refer to Section 9.2.4 "TX Power Ramping" on page 104.

11.5.3   Register Description

Register 0x04 (TRX_CTRL_1):

The TRX_CTRL_1 register is a multi purpose register to control various operating modes and settings of the radio transceiver.

Bit	7	6	5	4	3	2	1	0	
+0x04	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL	SPI_CMD_MODE		IRQ_MASK_MODE	IRQ_POLARITY	TRX_CTRL_1
Read/Write	R/W	R/W	R/W	R/W	R/W		R/W	R/W	
Reset Value	0	0	1	0	0		0	0	

- **Bit 7 - PA_EXT_EN**

This register bit enables pin 1 (DIG3) and pin 2 (DIG4) to indicate the transmit state of the radio transceiver.

Table 11-15.   RF Front-End Control Pins

PA_EXT_EN	State	Pin	Value	Description
0	n/a	DIG3	L	External RF front-end control disabled
		DIG4	L	
1[(1)]	TX_BUSY	DIG3	H	External RF front-end control enabled
		DIG4	L	
	Other	DIG3	L	
		DIG4	H	

Note: 1. It is recommended to set PA_EXT_EN = 1 only in receive or transmit states to reduce the power consumption or avoid leakage current of external RF switches or other building blocks, especially during SLEEP state.

- **Bit 6 - IRQ_2_EXT_EN**

Refer to Section 11.6 "RX Frame Time Stamping" on page 150.

- **Bit 5 - TX_AUTO_CRC_ON**

Refer to Section 8.2 "Frame Check Sequence (FCS)" on page 85.

- **Bit 4 - RX_BL_CTRL**

Refer to Section 11.7 "Frame Buffer Empty Indicator" on page 152.

- **Bit [3:2] - SPI_CMD_MODE**

Refer to Section 6.3 "Radio Transceiver Status information" on page 24.

- **Bit 1 - IRQ_MASK_MODE**

Refer to Section 6.6 "Interrupt Logic" on page 29.

- **Bit 0 - IRQ_POLARITY**

Refer to Section 6.6 "Interrupt Logic" on page 29.

11.6 RX Frame Time Stamping

11.6.1 Overview

To determine the exact timing of an incoming frame, e.g. for beaconing networks, the reception of this frame can be signaled to the microcontroller via pin 10 (DIG2). The pin turns from L to H after a detection of a valid PHR. When enabled, DIG2 is set to DIG2 = H at the same time as IRQ_2 (RX_START), even if IRQ_2 is disabled. The pin remains high for the length of the frame receive procedure, see Figure 11-3 on page 130.

Figure 11-12. Timing of RX_START and DIG2 for RX Frame Time Stamping
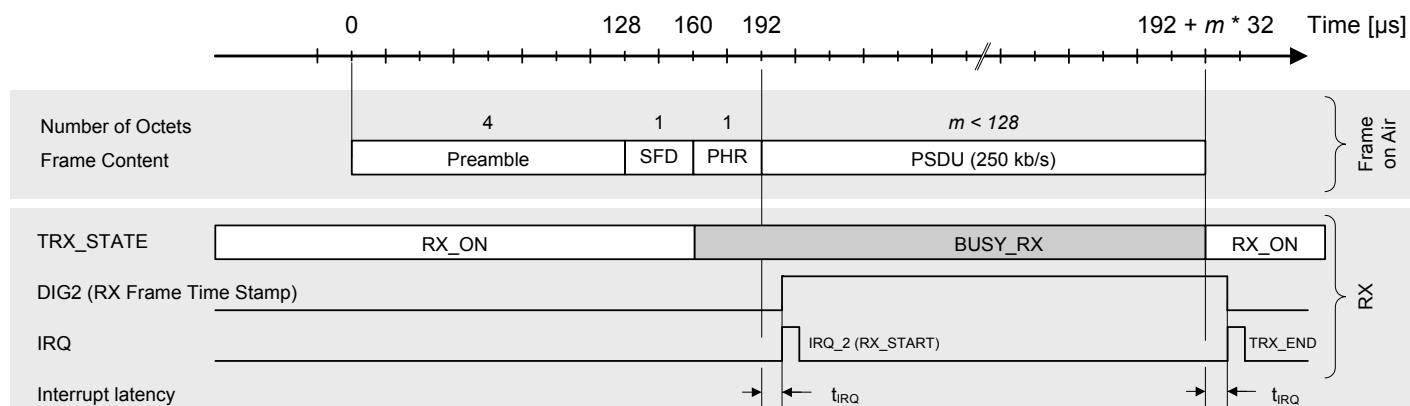
Note: Timing figures refer to 12.4 "Digital Interface Timing Characteristics" on page 157.

This function is enabled with register bit IRQ_2_EXT_EN (register 0x04) set. Pin 10 (DIG2) could be connected to a timer capture unit of the microcontroller.

If this pin is not used for RX Frame Time Stamping it can be configured for Antenna Diversity. Otherwise this pin is pulled-down to digital ground.

11.6.2 Register Description

Register 0x04 (TRX_CTRL_1):

Register 0x04 (TRX_CTRL_1) is a multi purpose register to control various operating modes and settings of the radio transceiver.

Bit	7	6	5	4	3	2	1	0	
+0x04	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL	SPI_CMD_MODE		IRQ_MASK_MODE	IRQ_POLARITY	TRX_CTRL_1
Read/Write	R/W	R/W	R/W	R/W	R/W		R/W	R/W	
Reset Value	0	0	1	0	0		0	0	

- **Bit 7 - PA_EXT_EN**

Refer to Section 11.5 "RX/TX Indicator" on page 147.

- **Bit 6 - IRQ_2_EXT_EN**

If this register bit is set the RX Frame Time Stamping Mode is enabled. An incoming frame with a valid PHR is signaled via pin 10 (DIG2). The pin remains at high level until the end of the frame receive procedure, see Figure 11-12 on page 150.

Do not enable RX Frame Time Stamping (IRQ_2_EXT_EN = 1) and Antenna Diversity (ANT_EXT_SW_EN = 1) at the same time, see Section 11.4 "Antenna Diversity" on page 142.

- **Bit 5 - TX_AUTO_CRC_ON**

Refer to Section 8.2 "Frame Check Sequence (FCS)" on page 85.

- **Bit 4 - RX_BL_CTRL**

Refer to Section 11.7 "Frame Buffer Empty Indicator" on page 152.

- **Bit [3:2] - SPI_CMD_MODE**

Refer to Section 6.3 "Radio Transceiver Status information" on page 24.

- **Bit 1 - IRQ_MASK_MODE**

Refer to Section 6.6 "Interrupt Logic" on page 29.

- **Bit 0 - IRQ_POLARITY**

Refer to Section 6.6 "Interrupt Logic" on page 29.

11.7 Frame Buffer Empty Indicator

11.7.1 Overview

For time critical applications that want to start reading the frame data as early as possible, the Frame Buffer status can be indicated to the microcontroller through a dedicated pin. This pin indicates to the microcontroller if an access to the Frame Buffer is not possible since valid PSDU data are missing.

Pin 24 (IRQ) can be configured as a Frame Buffer Empty Indicator during a Frame Buffer read access. This mode is enabled by register bit RX_BL_CTRL (register 0x04, TRX_CTRL_1). The IRQ pin turns into Frame Buffer Empty Indicator after the Frame Buffer read access command, see note *(1)* in Figure 11-13 on page 152, has been transferred on the SPI bus until the Frame Buffer read procedure has finished indicated by /SEL = H, see note *(4)*.

Figure 11-13. Timing Diagram of Frame Buffer Empty Indicator
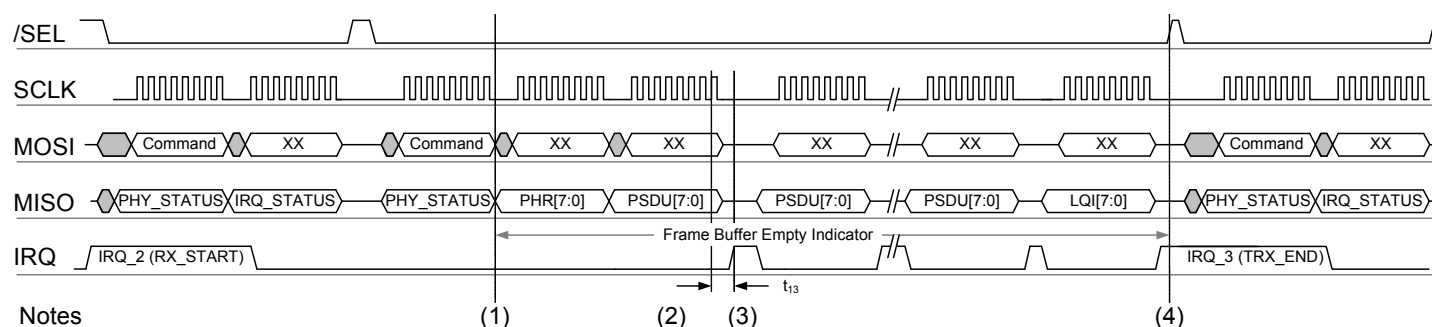
The microcontroller has to observe the IRQ pin during the Frame Buffer read procedure. A Frame Buffer read access can proceed as long as pin IRQ = L, see note *(2)*. Pin IRQ = H indicates that the Frame Buffer is currently not ready for another SPI cycle, note (3), and thus the Frame Buffer read procedure has to wait for valid data accordingly.

The access indicator pin 24 (IRQ) shows a valid access signal (either access is allowed or denied) not before t_{13} = 750 nsec after the rising edge of last SCLK clock of the Frame Buffer read command byte.

After finishing the SPI frame receive procedure, and the SPI has been released by /SEL = H, note *(4)*, pending interrupts are indicated immediately by pin IRQ. During all other SPI accesses, except during a SPI frame receive procedure with RX_BL_CTRL = 1, pin IRQ only indicates interrupts.

If a receive error occurs during the Frame Buffer read access the Frame Buffer Empty Indicator locks on 'empty' (pin IRQ = H) too. To prevent possible deadlocks, the microcontroller should impose a timeout counter that checks whether the Frame Buffer Empty Indicator remains logic high for more than 64 µs. Presuming a PHY data rate of 250 kb/s a new byte must have been arrived at the Frame Buffer during that period. If not, the Frame Buffer read access should be aborted.

11.7.2   Register Description

Register 0x04 (TRX_CTRL_1):

The TRX_CTRL_1 register is a multi purpose register to control various operating modes and settings of the radio transceiver.

Bit	7	6	5	4	3	2	1	0	
+0x04	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL	SPI_CMD_MODE		IRQ_MASK_MODE	IRQ_POLARITY	TRX_CTRL_1
Read/Write	R/W	R/W	R/W	R/W	R/W		R/W	R/W	
Reset Value	0	0	1	0	0		0	0	

- **Bit 7 - PA_EXT_EN**

Refer to Section 11.5 "RX/TX Indicator" on page 147.

- **Bit 6 - IRQ_2_EXT_EN**

Refer to Section 11.6 "RX Frame Time Stamping" on page 150.

- **Bit 5 - TX_AUTO_CRC_ON**

Refer to Section 8.2 "Frame Check Sequence (FCS)" on page 85.

- **Bit 4 - RX_BL_CTRL**

If this register bit is set the Frame Buffer Empty Indicator is enabled. After sending a Frame Buffer read command, refer to Section 6.2 "SPI Protocol" on page 19, pin 24 (IRQ) indicates to the microcontroller that an access to the Frame Buffer is not possible since valid PSDU data are missing.

Pin IRQ does not indicate any interrupts during this time.

Table 11-16. Frame Buffer Empty Indicator

Register Bit	Value	Description
RX_BL_CTRL	0	Frame Buffer Empty Indicator disabled
	1	Frame Buffer Empty Indicator enabled

- **Bit [3:2] - SPI_CMD_MODE**

Refer to Section 6.3 "Radio Transceiver Status information" on page 24.

- **Bit 1 - IRQ_MASK_MODE**

Refer to Section 6.6 "Interrupt Logic" on page 29.

- **Bit 0 - IRQ_POLARITY**

Refer to Section 6.6 "Interrupt Logic" on page 29.

11.8 Dynamic Frame Buffer Protection

11.8.1 Overview

The AT86RF231 continues the reception of incoming frames as long as it is in any receive state. When a frame was successfully received and stored into the Frame Buffer, the following frame will overwrite the Frame Buffer content again.

To relax the timing requirements for a Frame Buffer read access the Dynamic Frame Buffer Protection prevents that a new valid frame passes to the Frame Buffer until a Frame Buffer read access has ended (indicated by /SEL = H, refer to Section 6.2 "SPI Protocol" on page 19).

A received frame is automatically protected against overwriting:

- in Basic Operating Mode, if its FCS is valid
- in Extended Operating Mode, if an IRQ_3 (TRX_END) is generated

The Dynamic Frame Buffer Protection is enabled, if register bit RX_SAFE_MODE (register 0x0C, TRX_CTRL_2) is set and the transceiver state is RX_ON or RX_AACK_ON.

Note that Dynamic Frame Buffer Protection only prevents write accesses from the air interface - not from the SPI interface. A Frame Buffer or SRAM write access may still modify the Frame Buffer content.

11.8.2 Register Description

Register 0x0C (TRX_CTRL_2):

The TRX_CTRL_2 register is a multi purpose register to control various settings of the radio transceiver.

Bit	7	6	5	4	3	2	1	0	
+0x0C	RX_SAFE_MODE	Reserved					OQPSK_DATA_RATE		TRX_CTRL_2
Read/Write	R/W	R	R	R	R	R	R/W	R/W	
Reset Value	0	0	0	0	0	0	0	0	

- **Bit 7 - RX_SAFE_MODE**

If this bit is set Dynamic Frame Buffer Protection is enabled:

Table 11-17. Dynamic Frame Buffer Protection Mode

Register Bit	Value	Description
RX_SAFE_MODE[1]	0	Disable Dynamic Frame Buffer Protection
	1	Enable Dynamic Frame Buffer Protection

Note: 1. Dynamic Frame Buffer Protection is released with the rising edge of pin23 (/SEL) of a Frame Buffer read access, see Section 6.2.2 "Frame Buffer Access Mode" on page 20, or radio transceiver state changing from RX_ON or RX_AACK_ON to another state.

This operation mode is independent of the setting of register bits RX_PDT_LEVEL, refer to Section 9.1.3 "Configuration" on page 102.

- **Bit [6:2] - Reserved**

- **Bit [1:0] - OQPSK_DATA_RATE**

Refer to Section 11.3 "High Data Rate Modes" on page 137.

11.9 Configurable Start-Of-Frame Delimiter

11.9.1 Overview

The SFD is a field indicating the end of the SHR and the start of the packet data. The length of the SFD is 1 octet (2 symbols). This octet is used for byte synchronization only and is not included in the Frame Buffer.

The value of the SFD could be changed if it is needed to operate non IEEE 802.15.4 compliant networks. An IEEE 802.15.4 compliant network node does not synchronize to frames with a different SFD value.

Due to the way the SHR is formed, it is not recommended to set the low-order 4 bits to 0. The LSB of the SFD is transmitted first, i.e. right after the last bit of the preamble sequence.

11.9.2 Register Description

Register 0x0B (SFD_VALUE):

This register contains the one octet start-of-frame delimiter (SFD) to synchronize to a received frame.

Bit	7	6	5	4	3	2	1	0	
+0x0B				SFD_VALUE[7:0]					SFD_VALUE
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset Value	1	0	1	0	0	1	1	1	

- **Bit [7:0] - SFD_VALUE**

For compliant IEEE 802.15.4 networks set SFD_VALUE = 0xA7, as specified by [1] and [2]. This is the default value of the register.

To establish non IEEE 802.15.4 compliant networks the SFD value can be changed to any other value. If enabled an IRQ_2 (RX_START) is issued only if the received SFD matches the register content of register SFD_VALUE and a valid PHR is received.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 12-1. Absolute Maximum Ratings

No.	Symbol	Parameter	Condition	Min.	Typ.	Max	Units
12.1.1	T_{STOR}	Storage temperature		-50		150	°C
12.1.2	T_{LEAD}	Lead temperature	T = 10s, (soldering profile compliant with IPC/JEDEC J STD 020B)			260	°C
12.1.3	V_{ESD}	ESD robustness	Compl. to [3], Compl. to [4]	5000 1500			V V
12.1.4	P_{RF}	Input RF level				+10	dBm
12.1.5	V_{DIG}	Voltage on all pins (except pins 4, 5, 13, 14, 29)		-0.3		V_{DD}+0.3	V
12.1.6	V_{ANA}	Voltage on pins 4, 5, 13, 14, 29		-0.3		2.0	V

12.2 Recommended Operating Range

Table 12-2. Recommended Operating Range

No.	Symbol	Parameter	Condition	Min.	Typ.	Max	Units
12.2.1	T_{OP}	Operating temperature range		-40		+85	°C
12.2.2	V_{DD}	Supply voltage	Voltage on pins 15, 28[1]	1.8	3.0	3.6	V
12.2.3	$V_{DD1.8}$	Supply voltage	External voltage supply on pins 13, 14, 29[2]	1.7	1.8	1.9	V

Notes: 1. Even if an implementation uses the external 1.8V voltage supply $V_{DD1.8}$ it is required to connect V_{DD}.

2. Register 0x10 (VREG_CTRL) needs to be programmed to disable internal voltage regulators and supply blocks by an external 1.8V supply, refer to "Voltage Regulators (AVREG, DVREG)" on page 110.

12.3 Digital Pin Characteristics

.Test Conditions: T_{OP} = 25°C (unless otherwise stated)

Table 12-3. Digital Pin Characteristics

No.	Symbol	Parameter	Condition	Min.	Typ.	Max	Units
12.3.1	V_{IH}	High level input voltage[1]		V_{DD} - 0.4			V
12.3.2	V_{IL}	Low level input voltage[1]				0.4	V
12.3.3	V_{OH}	High level output voltage[1]	For all output driver strengths defined in TRX_CTRL_0	V_{DD} - 0.4			V
12.3.4	V_{OL}	Low level output voltage[1]	For all output driver strengths defined in TRX_CTRL_0			0.4	V

Note: 1. The capacitive load should not be larger than 50 pF for all I/Os when using the default driver strength settings, refer to Section 1.3.1 "Driver Strength Settings" on page 7. Generally, large load capacitances increase the overall current consumption.

12.4 Digital Interface Timing Characteristics

Test Conditions: T_{OP} = 25°C, V_{DD} = 3.0V, C_L = 50 pF (unless otherwise stated).

Table 12-4. Digital Interface Timing Characteristics

No.	Symbol	Parameter	Condition	Min.	Typ.	Max	Units
12.4.1	f_{sync}	SCLK frequency	synchronous operation			8	MHz
12.4.2	f_{async}	SCLK frequency	asynchronous operation			7.5	MHz
12.4.3	t_1	/SEL low to MISO active				180	ns
12.4.4	t_2	SCLK to MISO out	data hold time	10			ns
12.4.5	t_3	MOSI setup time		10			ns
12.4.6	t_4	MOSI hold time		10			ns
12.4.7	t_5	LSB last byte to MSB next byte		250[2]			ns
12.4.8	t_6	/SEL high to MISO tri state				10	ns
12.4.9	t_7	SLP_TR pulse width	TX start trigger	62.5		Note[1]	ns
12.4.10	t_8	SPI idle time (SEL rising to falling edge)	SPI read/write, standard SRAM and Frame Buffer access modes, Idle time between consecutive SPI accesses	250			ns
12.4.11	t_8	SPI idle time (SEL rising to falling edge)	SPI Fast SRAM read/write access mode, refer to Section 11.1.5, Idle time between consecutive SPI accesses	500			ns
12.4.12	t_9	Last SCLK to /SEL high			250		ns
12.4.13	t_{10}	Reset pulse width	□ 10 clock cycles at 16 MHz	625			ns
12.4.14	t_{11}	SPI access latency after reset	□ 10 clock cycles at 16 MHz	625			ns
12.4.15	t_{12}	AES core cycle time			24		µs

Table 12-4. Digital Interface Timing Characteristics (Continued)

12.4.15	t_{13}	BFBP IRQ latency			750		ns
12.4.17	t_{IRQ}	Interrupt event latency	Relative to the event to be indicated		9		µs
12.4.18	f_{CLKM}	Clock frequency at pin 17 (CLKM)	Configurable in register 0x03 (TRX_CTRL_0)		0		MHz
					1		MHz
					2		MHz
					4		MHz
					8		MHz
					16		MHz
					250		kHz
					62.5		kHz

Notes: 1. Maximum pulse width less than (TX frame length + 16 µs)

2. For Fast SRAM read/write accesses on address space 0x82 - 0x94 the time t_5 (Min.) increases to 450 ns.

12.5 General RF Specifications

Test Conditions (unless otherwise stated):

V_{DD} = 3.0V, f_{RF} = 2.45 GHz, T_{OP} = 25°C, Measurement setup see Figure 5-1 on page 12.

Table 12-5. General RF Specifications

No.	Symbol	Parameter	Condition	Min.	Typ.	Max	Units
12.5.1	f_{RF}	Frequency range	As specified in [1], [2]	2405		2480	MHz
12.5.2	f_{CH}	Channel spacing	As specified in [1], [2]		5		MHz
12.5.3	f_{HDR}	Header bit rate (SHR, PHR)	As specified in [1], [2]		250		kb/s
12.5.4	f_{PSDU}	PSDU bit rate	As specified in [1], [2] OQPSK_DATA_RATE = 1 OQPSK_DATA_RATE = 2 OQPSK_DATA_RATE = 3		250 500 1000 2000		kb/s kb/s kb/s kb/s
12.5.5	f_{CHIP}	Chip rate	As specified in [1], [2]		2000		kchip/s
12.5.6	f_{CLK}	Crystal oscillator frequency	Reference oscillator		16		MHz
12.5.7	t_{XTAL}	Reference oscillator settling time	Leaving SLEEP state to clock available at pin 17 (CLKM)		330	1000	µs
12.5.8		Symbol rate deviation Reference frequency accuracy for correct functionality	PSDU bit rate 250 kb/s PSDU bit rate 500 kb/s PSDU bit rate 1000 kb/s PSDU bit rate 2000 kb/s	-60[1] -40 -40 -30		+60 +40 +40 +30	ppm ppm ppm ppm
12.5.9	B_{20dB}	20 dB bandwidth			2.8		MHz

Note: 1. A reference frequency accuracy of ±40 ppm is required by [1], [2].

12.6 Transmitter Characteristics

Test Conditions (unless otherwise stated):

V_{DD} = 3.0V, f_{RF} = 2.45 GHz, T_{OP} = 25°C, Measurement setup see Figure 5-1 on page 12.

Table 12-6. Transmitter Characteristics

No.	Symbol	Parameter	Condition	Min.	Typ.	Max	Units
12.6.1	P_{TX}	TX Output power	Maximum configurable TX output power value Register bit TX_PWR = 0	0	+3	+6	dBm
12.6.2	P_{RANGE}	Output power range	16 steps, configurable in register 0x05 (PHY_TX_PWR)		20		dB
12.6.3	P_{ACC}	Output power tolerance				±3	dB
12.6.4		TX Return loss	100Ω differential impedance, P_{TX} = +3 dBm		10		dB
12.6.5		EVM			8		%rms
12.6.6	P_{HARM}	Harmonics 2nd harmonic 3rd harmonic		-45	-45		dBm dBm
12.6.7	P_{SPUR}	Spurious Emissions 30 - ≤ 1000 MHz >1 - 12.75 GHz 1.8 - 1.9 GHz 5.15 - 5.3 GHz	Complies with EN 300 328/440, FCC-CFR-47 part 15, ARIB STD-66, RSS-210		-36 -30 -47 -47		dBm dBm dBm dBm

12.7 Receiver Characteristics

Test Conditions (unless otherwise stated):

V_{DD} = 3.0V, f_{RF} = 2.45 GHz, T_{OP} = 25°C, PSDU bit rate = 250 kb/s, Measurement setup see Figure 5-1 on page 12.

Table 12-7. Receiver Characteristics

No.	Symbol	Parameter	Condition	Min.	Typ.	Max	Units
12.7.1	P_{SENS}	Receiver sensitivity 250 kb/s 500 kb/s 1000 kb/s 2000 kb/s	AWGN channel, PER ≤ 1%, PSDU length 20 octets High Data Rate Modes: PSDU length 20 octets		-101 -97 -95 -89		dBm dBm dBm dBm
		Antenna Diversity	250 kb/s, PSDU 20 octets		-99		dBm
12.7.2	RL	Return loss	100Ω differential impedance		10		dB
12.7.3	NF	Noise figure			6		dB
12.7.4	P_{RXMX}	Maximum RX input level	PER ≤ 1%, PSDU length of 20 octets		10		dBm
12.7.5	P_{ACRN}	Adjacent channel rejection: Δf = -5 MHz	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm		32		dB
12.7.6	P_{ACRP}	Adjacent channel rejection: Δf = +5 MHz	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm		35		dB
12.7.7	P_{AACR1}	Alternate channel rejection: Δf = |10 MHz|	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm		48		dB
12.7.8	P_{AACR2}	2nd Alternate channel rejection: Δf = |15 MHz|	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm		54		dB
12.7.9	P_{SPUR}	Spurious emissions: LO leakage 30 - ≤1000 MHz >1 - 12.75 GHz			-70	 -57 -47	dBm dBm dBm
12.7.10	$f_{RXTXOFFS}$	TX/RX carrier frequency offset	Sensitivity loss < 2 dB	-300[1]		+300	kHz
12.7.11	IIP3	3rd - order intercept point	At maximum gain Offset freq. interf. 1 = 5 MHz Offset freq. interf. 2 = 10 MHz		-10		dBm
12.7.12	IIP2	2nd - order intercept point	At maximum gain Offset freq. interf. 1 = 60 MHz Offset freq. interf. 2 = 62 MHz		31		dBm
12.7.13		RSSI tolerance	Tolerance within gain step			±5	dB
12.7.14		RSSI dynamic range			81		dB
12.7.15		RSSI resolution			3		dB
12.7.16		RSSI sensitivity	Defined as RSSI_BASE_VAL		-91		dBm
12.7.17		Minimum RSSI value	P_{RF} ≤ RSSI_BASE_VAL		0		
12.7.18		Maximum RSSI value	P_{RF} > RSSI_BASE_VAL + 81 dB		28		

Note: 1.   Offset equals ±120 ppm.

12.8 Current Consumption Specifications

Test Conditions (unless otherwise stated):

V_{DD} = 3.0V, f_{RF} = 2.45 GHz, T_{OP} = 25°C, Measurement setup see Figure 5-1 on page 12.

Table 12-8. Current Consumption Specifications[1]

No.	Symbol	Parameter	Condition	Min.	Typ.	Max	Units
12.8.1	I_{BUSY_TX}	Supply current transmit state	P_{TX} = 3 dBm P_{TX} = 0 dBm P_{TX} = -17 dBm		14 11.6 7.4		mA mA mA
12.8.2	I_{RX_ON}	Supply current RX_ON state	RX_ON state - high input level		10.3		mA
12.8.3	I_{RX_ON}	Supply current RX_ON state	RX_ON state - high sensitivity		12.3		mA
12.8.4	$I_{PLL\_ON\_P}$	Supply current RX_ON state	RX_ON state, with register setting RX_PDT_LEVEL > 0[2]		11.8		mA
12.8.5	I_{PLL_ON}	Supply current PLL_ON state	PLL_ON state		5.6		mA
12.8.6	I_{TRX_OFF}	Supply current TRX_OFF state	TRX_OFF state		0.4		mA
12.8.7	I_{SLEEP}	Supply current SLEEP state	SLEEP state			0.02	µA

Note: 1. Current consumption for all operating modes is reduced at lower V_{DD}.
2. Refer to Section 9.1 "Receiver (RX)" on page 101

12.9 Crystal Parameter Requirements

Table 12-9. Crystal Parameter Requirements

No.	Symbol	Parameter	Condition	Min.	Typ.	Max	Units
12.9.1	f_0	Crystal frequency			16		MHz
12.9.2	C_L	Load capacitance		8		14	pF
12.9.3	C_0	Static capacitance				7	pF
12.9.4	R_1	Series resistance				100	Ω

13. Typical Characteristics

13.1 Active Supply Current

The following charts showing each a typical behavior of the AT86RF231. These figures are not tested during manufacturing. All power consumption measurements are performed with pin 17 (CLKM) disabled, unless otherwise stated. The measurement setup used for the measurements is shown in Figure 5-1 on page 12.

Power consumption for the microcontroller required to program the radio transceiver is not included in the measurement results.

The power consumption in SLEEP state mode is independent from CLKM master clock rate selection.

The current consumption is a function of several factors such as: operating voltage, operating frequency, loading of I/O pins, switching rate of I/O pins, and ambient temperature. The dominating factors are operating voltage and ambient temperature.

If possible the measurement results are not affected by current drawn from I/O pins. Register, SRAM or Frame Buffer read or write accesses are not performed during current consumption measurements.

13.1.1 P_ON and TRX_OFF states

Figure 13-1. Current Consumption in P_ON State
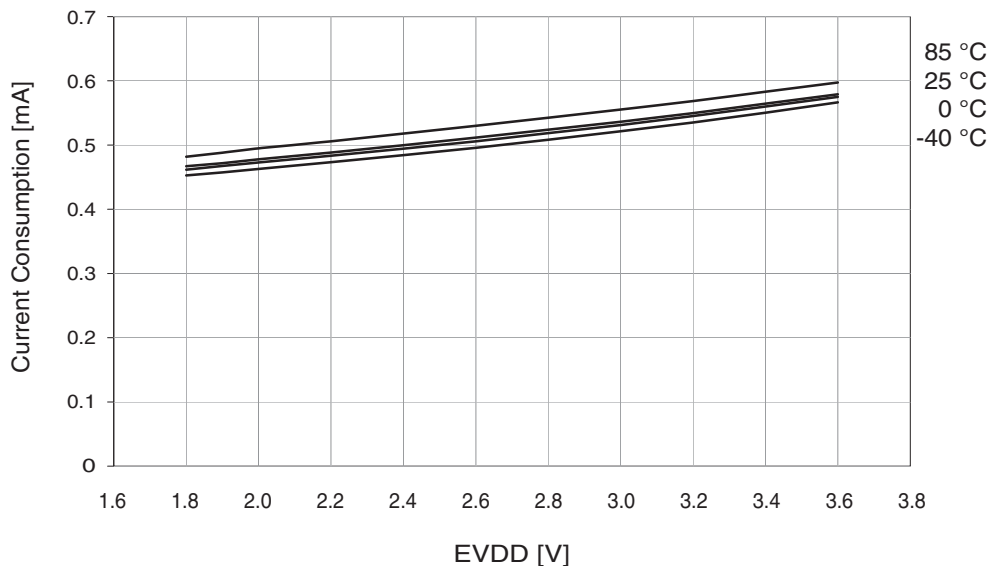
Figure 13-2. Current Consumption in TRX_OFF State
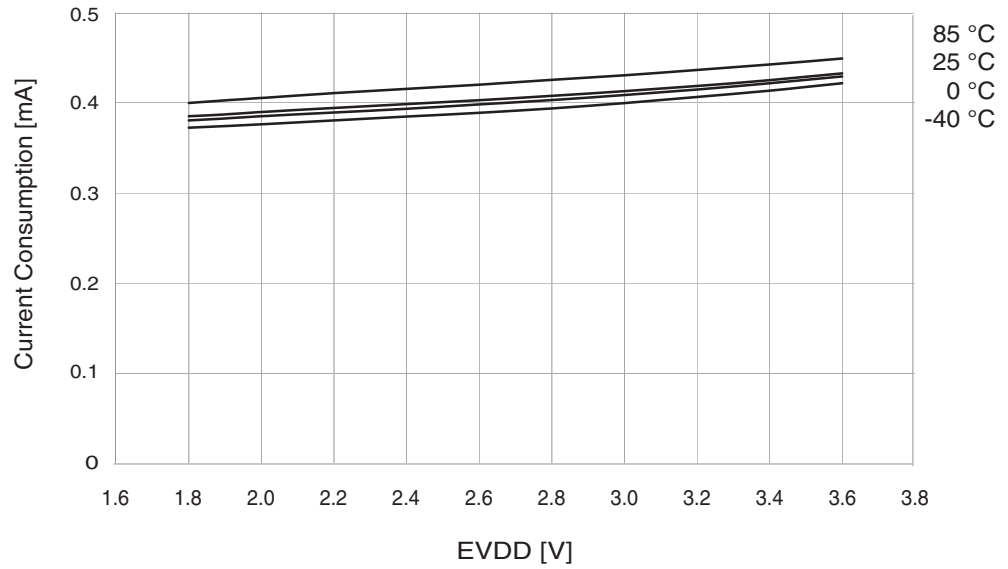
13.1.2   PLL_ON state

Figure 13-3. Current Consumption in PLL_ON State
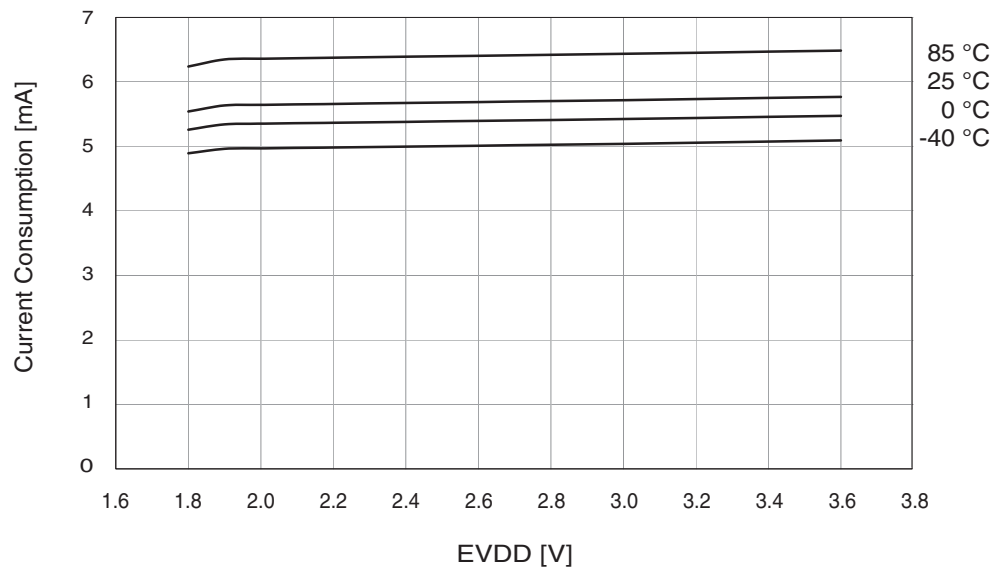
13.1.3   RX_ON state

Figure 13-4.   Current Consumption in RX_ON State - High Sensitivity
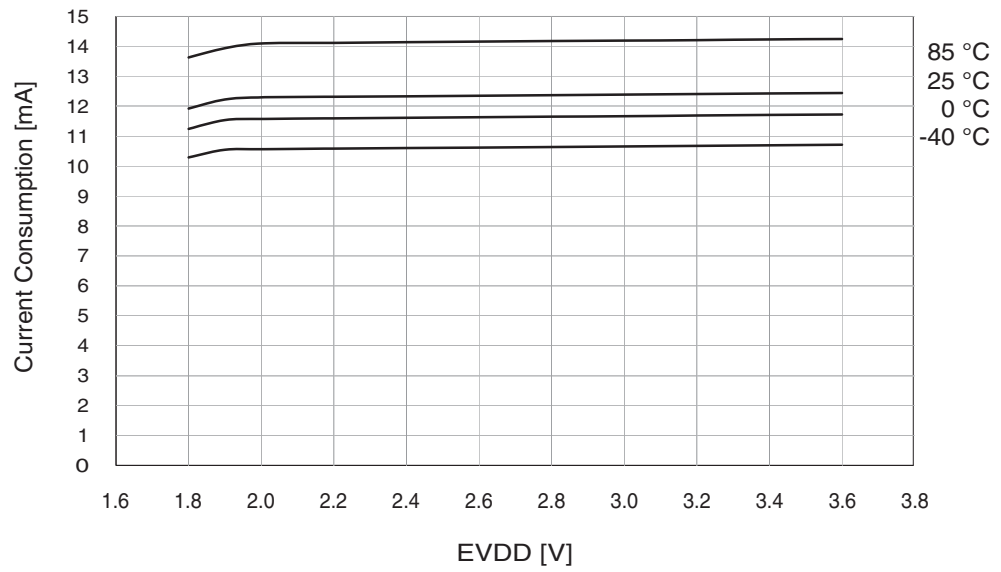
Figure 13-5.   Current Consumption in RX_ON State - High Input Level
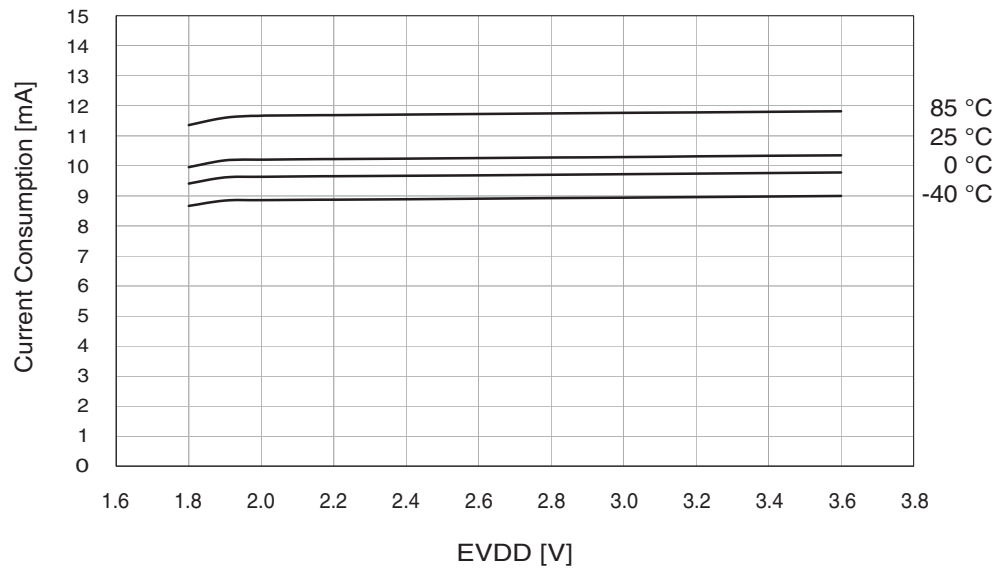
Figure 13-6. Current Consumption in RX_ON State - Reduced Sensitivity
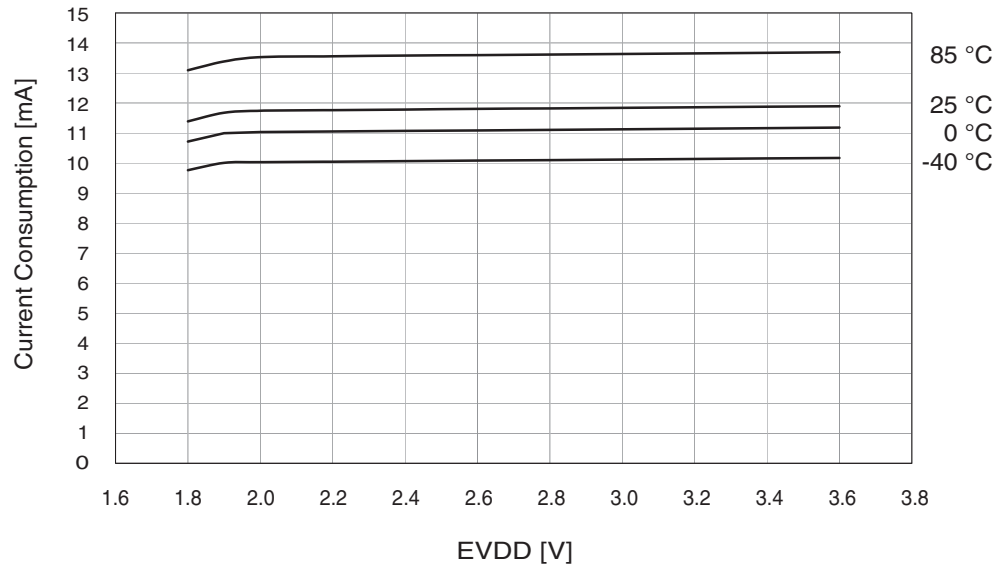
13.1.4 TX_BUSY state

Figure 13-7. Current Consumption in TX_BUSY State - Minimum Output Power
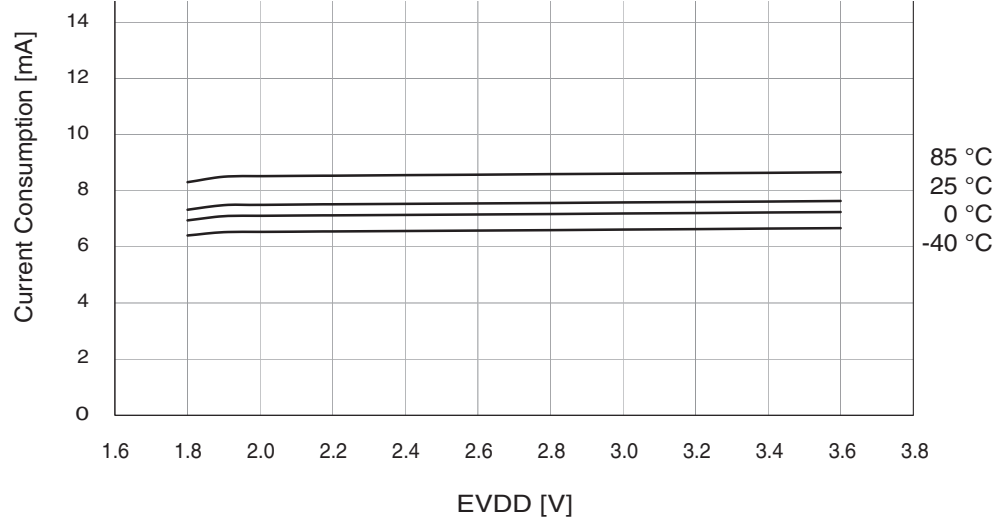
Figure 13-8. Current Consumption in TX_BUSY State - Output Power 0 dBm
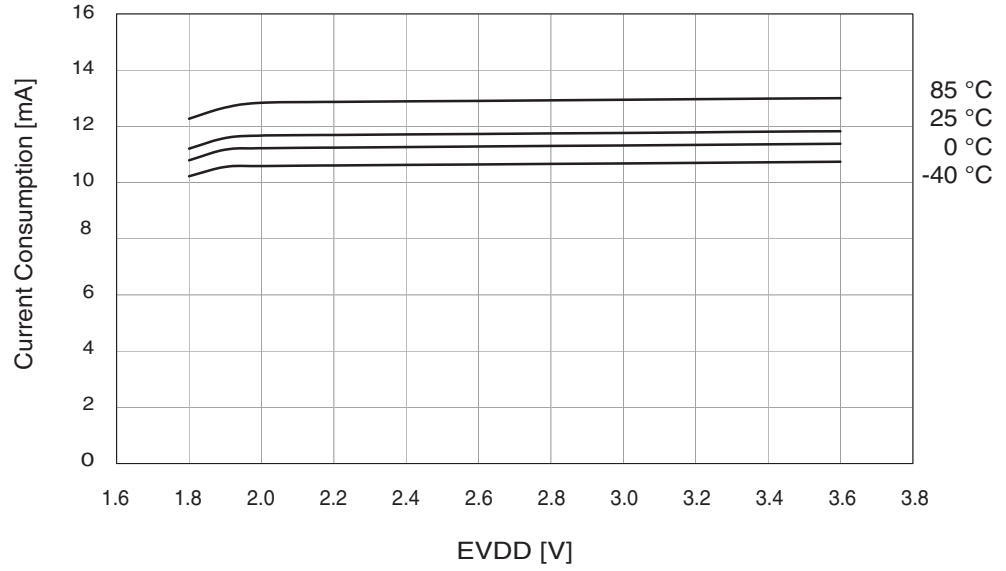
Figure 13-9. Current Consumption in TX_BUSY State - Maximum Output Power
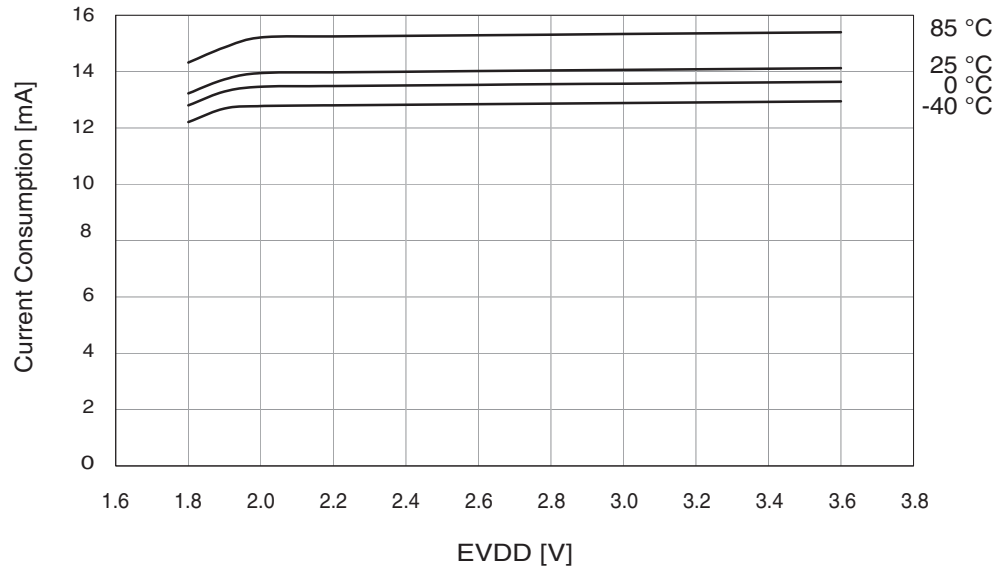
13.1.5   SLEEP

Figure 13-10. Current Consumption in SLEEP
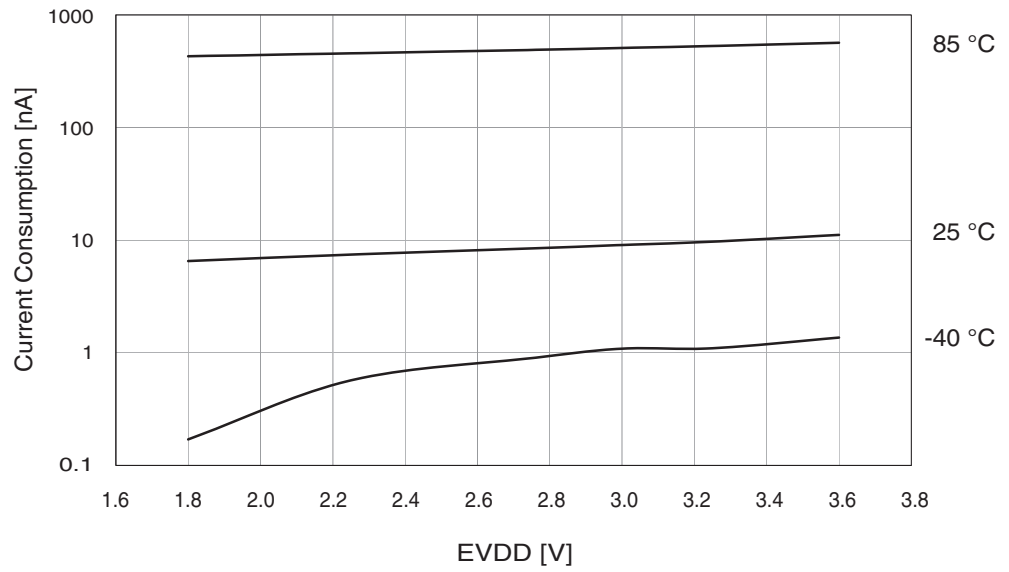
13.2   State Transition Timing

Figure 13-11. Transition Time from EVDD to P_ON (CLKM available)
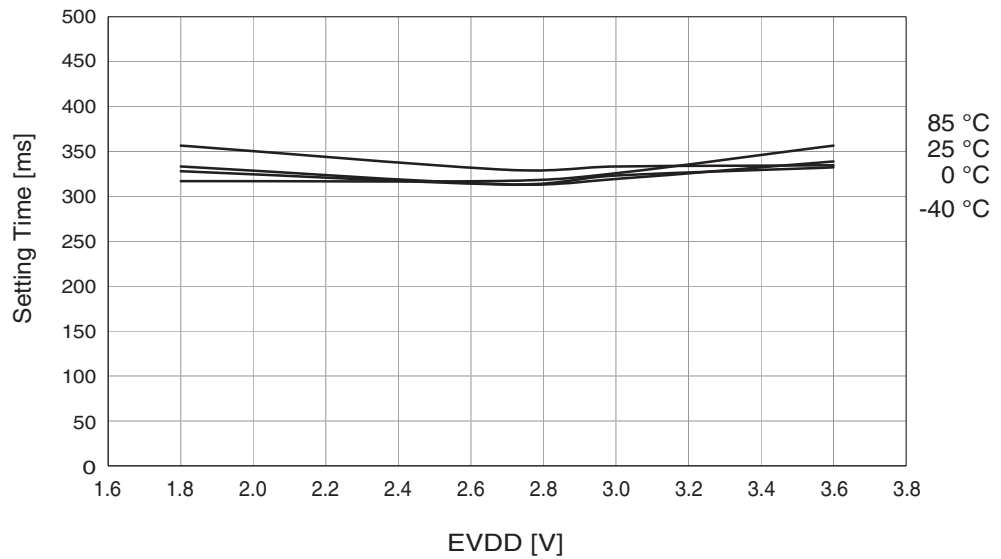
Figure 13-12. Transition Time from SLEEP to TRX_OFF (IRQ_4 (AWAKE_END))
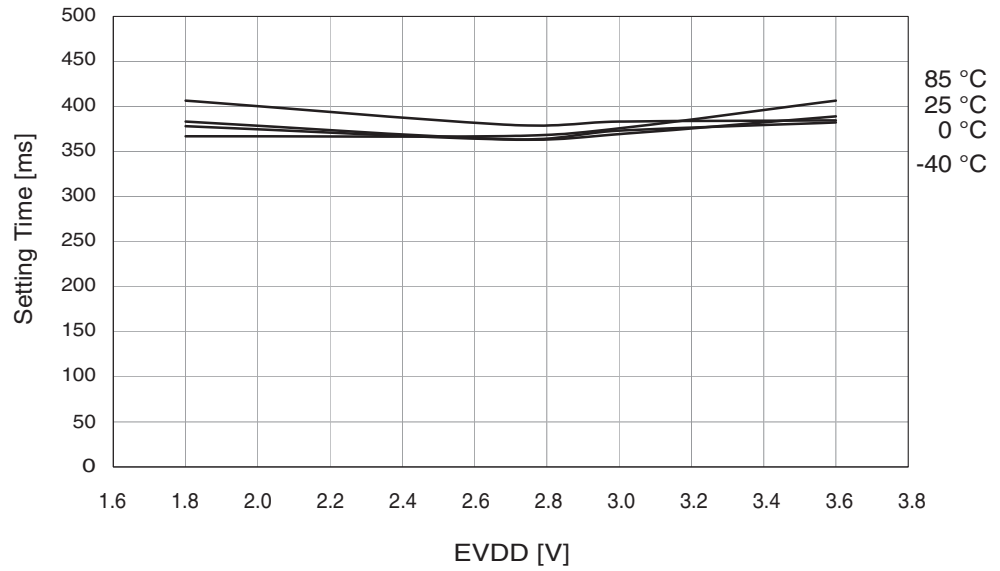
Figure 13-13. Transition Time from TRX_OFF to PLL_ON
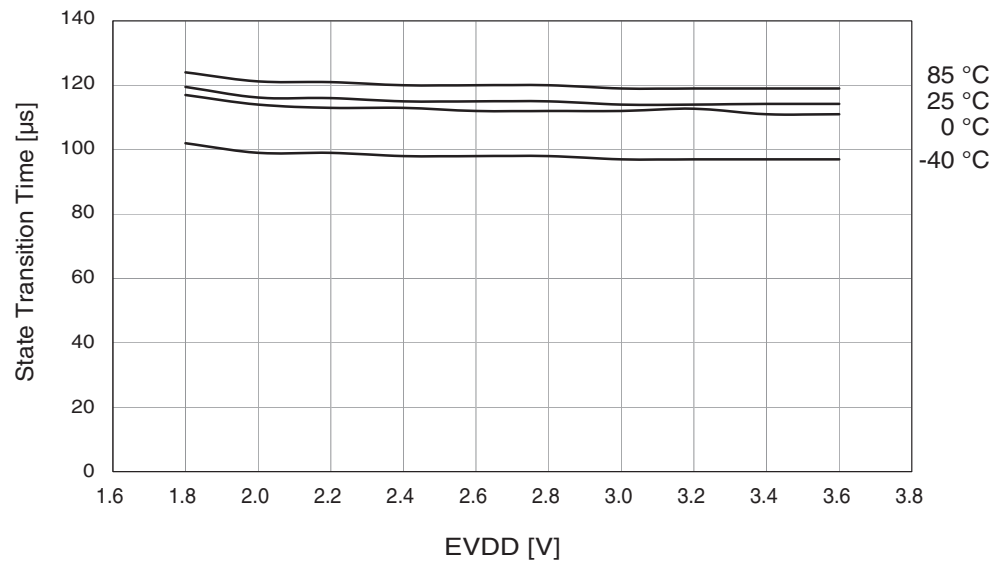
14. Register Summary

The AT86RF231 provides a register space of 64 8-bit registers, used to configure, control and monitor the radio transceiver.

Note: All registers not mentioned within the following table are reserved for internal use and must not be overwritten. When writing to a register, any reserved bits shall be overwritten only with their reset value.

Addr	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Page
0x00	-	-	-	-	-	-	-	-	-	-
0x01	TRX_STATUS	CCA_DONE	CCA_STATUS	-	TRX_STATUS[4]	TRX_STATUS[3]	TRX_STATUS[2]	TRX_STATUS[1]	TRX_STATUS[0]	44,68,97
0x02	TRX_STATE	TRAC_STATUS[2]	TRAC_STATUS[1]	TRAC_STATUS[0]	TRX_CMD[4]	TRX_CMD[3]	TRX_CMD[2]	TRX_CMD[1]	TRX_CMD[0]	33,44,68
0x03	TRX_CTRL_0	PAD_IO[1]	PAD_IO[0]	PAD_IO_CLKM[1]	PAD_IO_CLKM[0]	CLKM_SHA_SEL	CLKM_CTRL[2]	CLKM_CTRL[1]	CLKM_CTRL[0]	8,118,
0x04	TRX_CTRL_1	PA_EXT_EN	IRQ_2_EXT_EN	TX_AUTO_CRC_ON	RX_BL_CTRL	SPI_CMD_MODE[1]	SPI_CMD_MODE[0]	IRQ_MASK_MODE	IRQ_POLARITY	24,30,148
0x05	PHY_TX_PWR	PA_BUF_LT[1]	PA_BUF_LT[0]	PA_LT[1]	PA_LT[0]	TX_PWR[3]	TX_PWR[2]	TX_PWR[1]	TX_PWR[0]	105
0x06	PHY_RSSI	RX_CRC_VALID	RND_VALUE[1]	RND_VALUE[0]	RSSI[4]	RSSI[3]	RSSI[2]	RSSI[1]	RSSI[0]	90,136
0x07	PHY_ED_LEVEL	ED_LEVEL[7]	ED_LEVEL[6]	ED_LEVEL[5]	ED_LEVEL[4]	ED_LEVEL[3]	ED_LEVEL[2]	ED_LEVEL[1]	ED_LEVEL[0]	93
0x08	PHY_CC_CCA	CCA_REQUEST	CCA_MODE[1]	CCA_MODE[0]	CHANNEL[4]	CHANNEL[3]	CHANNEL[2]	CHANNEL[1]	CHANNEL[0]	97
0x09	CCA_THRES	-	-	-	-	CCA_ED_THRES[3]	CCA_ED_THRES[2]	CCA_ED_THRES[1]	CCA_ED_THRES[0]	97
0x0A	RX_CTRL	-	-	-	-	PDT_THRES[3]	PDT_THRES[2]	PDT_THRES[1]	PDT_THRES[0]	140
0x0B	SFD_VALUE	SFD_VALUE[7]	SFD_VALUE[6]	SFD_VALUE[5]	SFD_VALUE[4]	SFD_VALUE[3]	SFD_VALUE[2]	SFD_VALUE[1]	SFD_VALUE[0]	155
0x0C	TRX_CTRL_2	RX_SAFE_MODE	-	-	-	-	-	OQPSK_DATA_RATE[1]	OQPSK_DATA_RATE[0]	154
0x0D	ANT_DIV	ANT_SEL	-	-	-	ANT_DIV_EN	ANT_EXT_SW_EN	ANT_CTRL[1]	ANT_CTRL[0]	143
0x0E	IRQ_MASK	MASK_BAT_LOW	MASK_TRX_UR	MASK_AMI	MASK_CCA_ED_DONE	MASK_TRX_END	MASK_TRX_START	MASK_PLL_UNLOCK	MASK_PLL_LOCK	30
0x0F	IRQ_STATUS	BAT_LOW	TRX_UR	AMI	CCA_ED_DONE	TRX_END	RX_START	PLL_UNLOCK	PLL_LOCK	30
0x10	VREG_CTRL	AVREG_EXT	AVDD_OK	-	-	DVREG_EXT	DVDD_OK	-	-	111
0x11	BATMON	-	-	BATMON_OK	BATMON_HR	BATMON_VTH[3]	BATMON_VTH[2]	BATMON_VTH[1]	BATMON_VTH[0]	113
0x12	XOSC_CTRL	XTAL_MODE[3]	XTAL_MODE[2]	XTAL_MODE[1]	XTAL_MODE[0]	XTAL_TRIM[3]	XTAL_TRIM[2]	XTAL_TRIM[1]	XTAL_TRIM[0]	116
0x13	-	-	-	-	-	-	-	-	-	
0x14	-	-	-	-	-	-	-	-	-	
0x15	RX_SYN	RX_PDT_DIS	-	-	-	RX_PDT_LEVEL[3]	RX_PDT_LEVEL[2]	RX_PDT_LEVEL[1]	RX_PDT_LEVEL[0]	103
0x16	-	-	-	-	-	-	-	-	-	
0x17	XAH_CTRL_1	-	-	AACK_FLTR_RES_FT	AACK_UPLD_RES_FT	-	AACK_ACK_TIME	AACK_PROM_MODE	-	68,140
0x18	FTN_CTRL	FTN_START	-	-	-	-	-	-	-	125
0x19	-	-	-	-	-	-	-	-	-	
0x1A	PLL_CF	PLL_CF_START	-	-	-	-	-	-	-	122
0x1B	PLL_DCU	PLL_DCU_START	-	-	-	-	-	-	-	122
0x1C	PART_NUM	PART_NUM[7]	PART_NUM[6]	PART_NUM[5]	PART_NUM[4]	PART_NUM[3]	PART_NUM[2]	PART_NUM[1]	PART_NUM[0]	25
0x1D	VERSION_NUM	VERSION_NUM[7]	VERSION_NUM[6]	VERSION_NUM[5]	VERSION_NUM[4]	VERSION_NUM[3]	VERSION_NUM[2]	VERSION_NUM[1]	VERSION_NUM[0]	25
0x1E	MAN_ID_0	MAN_ID_0[7]	MAN_ID_0[6]	MAN_ID_0[5]	MAN_ID_0[4]	MAN_ID_0[3]	MAN_ID_0[2]	MAN_ID_0[1]	MAN_ID_0[0]	25
0x1F	MAN_ID_1	MAN_ID_1[7]	MAN_ID_1[6]	MAN_ID_1[5]	MAN_ID_1[4]	MAN_ID_1[3]	MAN_ID_1[2]	MAN_ID_1[1]	MAN_ID_1[0]	25
0x20	SHORT_ADDR_0	SHORT_ADDR_0[7]	SHORT_ADDR_0[6]	SHORT_ADDR_0[5]	SHORT_ADDR_0[4]	SHORT_ADDR_0[3]	SHORT_ADDR_0[2]	SHORT_ADDR_0[1]	SHORT_ADDR_0[0]	76
0x21	SHORT_ADDR_1	SHORT_ADDR_1[7]	SHORT_ADDR_1[6]	SHORT_ADDR_1[5]	SHORT_ADDR_1[4]	SHORT_ADDR_1[3]	SHORT_ADDR_1[2]	SHORT_ADDR_1[1]	SHORT_ADDR_1[0]	76
0x22	PAN_ID_0	PAN_ID_0[7]	PAN_ID_0[6]	PAN_ID_0[5]	PAN_ID_0[4]	PAN_ID_0[3]	PAN_ID_0[2]	PAN_ID_0[1]	PAN_ID_0[0]	76
0x23	PAN_ID_1	PAN_ID_1[7]	PAN_ID_1[6]	PAN_ID_1[5]	PAN_ID_1[4]	PAN_ID_1[3]	PAN_ID_1[2]	PAN_ID_1[1]	PAN_ID_1[0]	76
0x24	IEEE_ADDR_0	IEEE_ADDR_0[7]	IEEE_ADDR_0[6]	IEEE_ADDR_0[5]	IEEE_ADDR_0[4]	IEEE_ADDR_0[3]	IEEE_ADDR_0[2]	IEEE_ADDR_0[1]	IEEE_ADDR_0[0]	76
0x25	IEEE_ADDR_1	IEEE_ADDR_1[7]	IEEE_ADDR_1[6]	IEEE_ADDR_1[5]	IEEE_ADDR_1[4]	IEEE_ADDR_1[3]	IEEE_ADDR_1[2]	IEEE_ADDR_1[1]	IEEE_ADDR_1[0]	76
0x26	IEEE_ADDR_2	IEEE_ADDR_2[7]	IEEE_ADDR_2[6]	IEEE_ADDR_2[5]	IEEE_ADDR_2[4]	IEEE_ADDR_2[3]	IEEE_ADDR_2[2]	IEEE_ADDR_2[1]	IEEE_ADDR_2[0]	76
0x27	IEEE_ADDR_3	IEEE_ADDR_3[7]	IEEE_ADDR_3[6]	IEEE_ADDR_3[5]	IEEE_ADDR_3[4]	IEEE_ADDR_3[3]	IEEE_ADDR_3[2]	IEEE_ADDR_3[1]	IEEE_ADDR_3[0]	76
0x28	IEEE_ADDR_4	IEEE_ADDR_4[7]	IEEE_ADDR_4[6]	IEEE_ADDR_4[5]	IEEE_ADDR_4[4]	IEEE_ADDR_4[3]	IEEE_ADDR_4[2]	IEEE_ADDR_4[1]	IEEE_ADDR_4[0]	76
0x29	IEEE_ADDR_5	IEEE_ADDR_5[7]	IEEE_ADDR_5[6]	IEEE_ADDR_5[5]	IEEE_ADDR_5[4]	IEEE_ADDR_5[3]	IEEE_ADDR_5[2]	IEEE_ADDR_5[1]	IEEE_ADDR_5[0]	76
0x2A	IEEE_ADDR_6	IEEE_ADDR_6[7]	IEEE_ADDR_6[6]	IEEE_ADDR_6[5]	IEEE_ADDR_6[4]	IEEE_ADDR_6[3]	IEEE_ADDR_6[2]	IEEE_ADDR_6[1]	IEEE_ADDR_6[0]	76
0x2B	IEEE_ADDR_7	IEEE_ADDR_7[7]	IEEE_ADDR_7[6]	IEEE_ADDR_7[5]	IEEE_ADDR_7[4]	IEEE_ADDR_7[3]	IEEE_ADDR_7[2]	IEEE_ADDR_7[1]	IEEE_ADDR_7[0]	76
0x2C	XAH_CTRL_0	MAX_FRAME_RETRES[3]	MAX_FRAME_RETRES[2]	MAX_FRAME_RETRES[1]	MAX_FRAME_RETRES[0]	MAX_CSMA_RETRES[2]	MAX_CSMA_RETRES[1]	MAX_CSMA_RETRES[0]	SLOTTED_OPERATION	68

0x2D	CSMA_SEED_0	CSMA_SEED_0[7]	CSMA_SEED_0[6]	CSMA_SEED_0[5]	CSMA_SEED_0[4]	CSMA_SEED_0[3]	CSMA_SEED_0[2]	CSMA_SEED_0[1]	CSMA_SEED_0[0]	68
0x2E	CSMA_SEED_1	AACK_FVN_MODE[1]	AACK_FVN_MODE[0]	AACK_SET_PD	AACK_DIS_ACK	AACK_I_AM_COORD	CSMA_SEED_1[2]	CSMA_SEED_1[1]	CSMA_SEED_1[0]	68
0x2F	CSMA_BE	MAX_BE[3]	MAX_BE[2]	MAX_BE[1]	MAX_BE[0]	MIN_BE[3]	MIN_BE[2]	MIN_BE[1]	MIN_BE[0]	68
....	-	-	-	-	-	-	-	-	-	

The reset values of the AT86RF231 registers in state P_ON[1, 2, 3] are shown in Table 14-1 on page 170.

Note: All reset values in Table 14-1 on page 170 are only valid after a power on reset. After a reset procedure (/RST = L) as described in Section 7.1.4.5 "Reset Procedure" on page 41 the reset values of selected registers (e.g. registers 0x01, 0x10, 0x11, 0x30) can differ from that in Table 14-1 on page 170.

Table 14-1. Register Summary - Reset Values

Address	Reset Value	Address	Reset Value	Address	Reset Value	Address	Reset Value
0x00	0x00	0x10	0x00[1]	0x20	0xFF	0x30	0x00[3]
0x01	0x00	0x11	0x02[2]	0x21	0xFF	0x31	0x00
0x02	0x00	0x12	0xF0	0x22	0xFF	0x32	0x00
0x03	0x19	0x13	0x00	0x23	0xFF	0x34	0x00
0x04	0x20	0x14	0x00	0x24	0x00	0x34	0x00
0x05	0xC0	0x15	0x00	0x25	0x00	0x35	0x00
0x06	0x00	0x16	0x00	0x26	0x00	0x36	0x00
0x07	0xFF	0x17	0x00	0x27	0x00	0x37	0x00
0x08	0x2B	0x18	0x58	0x28	0x00	0x38	0x00
0x09	0xC7	0x19	0x55	0x29	0x00	0x39	0x40
0x0A	0xB7	0x1A	0x57	0x2A	0x00	0x3A	0x00
0x0B	0xA7	0x1B	0x20	0x2B	0x00	0x3B	0x00
0x0C	0x00	0x1C	0x03	0x2C	0x38	0x3C	0x00
0x0D	0x03	0x1D	0x02	0x2D	0xEA	0x3D	0x00
0x0E	0x00	0x1E	0x1F	0x2E	0x42	0x3E	0x00
0x0F	0x00	0x1F	0x00	0x2F	0x53	0x3F	0x00

Notes: 1. While the reset value of register 0x10 is 0x00, any practical access to the register is only possible when DVREG is active. So this register is normally always read out as 0x04. For details refer to Section 9.4 "Voltage Regulators (AVREG, DVREG)" on page 110.

2. While the reset value of register 0x11 is 0x02, any practical access to the register is only possible when BATMON is activated. So this register is normally always read out as 0x22 in P_ON state. For details refer to Section 9.5 "Battery Monitor (BATMON)" on page 113.

3. While the reset value of register 0x30 is 0x00, any practical access to the register is only possible when the radio transceiver is accessible. So the register is normally read out as:

       a) 0x11 after a reset in P_ON state

       b) 0x07 after a reset in any other state

15. Abbreviations

AACK	-	Automatic acknowledgement
ACK	-	Acknowledgement
ADC	-	Analog-to-digital converter
AD	-	Antenna diversity
AGC	-	Automated gain control
AES	-	Advanced encryption standard
ARET	-	Automatic retransmission
AVREG	-	Voltage regulator for analog building blocks
AWGN	-	Additive White Gaussian Noise
BATMON	-	Battery monitor
BBP	-	Base band processor
BPF	-	Band pass filter
CBC	-	Cipher block chaining
CRC	-	Cyclic redundancy check
CCA	-	Clear channel assessment
CSMA-CA	-	Carrier sense multiple access/Collision avoidance
CW	-	Continuous wave
DFBP	-	Dynamic Frame Buffer Protection
DVREG	-	Voltage regulator for digital building blocks
ECB	-	Electronic code book
ED	-	Energy detection
ESD	-	Electrostatic discharge
EVM	-	Error vector magnitude
FCF	-	Frame control field
FCS	-	Frame check sequence
FIFO	-	First in first out
FTN	-	Filter tuning network
GPIO	-	General purpose input output
ISM	-	Industrial, scientific, and medical
LDO	-	Low-drop output
LNA	-	Low-noise amplifier
LO	-	Local oscillator
LQI	-	Link quality indicator
LSB	-	Least significant bit
MAC	-	Medium access control

MFR	-	MAC footer
MHR	-	MAC header
MISO	-	SPI Interface: Master input slave output
MOSI	-	SPI Interface: Master output slave input
MSB	-	Most significant bit
MSDU	-	MAC service data unit
MPDU	-	MAC protocol data unit
MSK	-	Minimum shift keying
O-QPSK	-	Offset - quadrature phase shift keying
PA	-	Power amplifier
PAN	-	Personal area network
PCB	-	Printed circuit board
PER	-	Packet error rate
PHR	-	PHY header
PHY	-	Physical layer
PLL	-	Phase locked loop
POR	-	Power-on reset
PPF	-	Poly-phase filter
PRBS	-	Pseudo random bit sequence
PSDU	-	PHY service data unit
PSD	-	Power spectral mask
QFN	-	Quad flat no-lead package
RF	-	Radio frequency
RSSI	-	Received signal strength indicator
RX	-	Receiver
SCLK	-	SPI Interface: SPI clock
/SEL	-	SPI Interface: SPI select
SFD	-	Start-of-frame delimiter
SHR	-	Synchronization header
SPI	-	Serial peripheral interface
SRAM	-	Static random access memory
SSBF	-	Single side band filter
TX	-	Transmitter
VCO	-	Voltage controlled oscillator
VREG	-	Voltage regulator
XOSC	-	Crystal oscillator

16. Ordering Information

Ordering Code	Package	Voltage Range	Temperature Range
AT86RF231-ZU	QN	1.8V - 3.6V	Industrial (-40° C to +85° C) Lead-free/Halogen-free
AT86RF231-ZF	QN	1.8V - 3.6V	Industrial (-40° C to +125° C) Lead-free/Halogen-free

Package Type	Description
QN	32QN2, 32 lead 5.0x5.0 mm Body, 0.50 mm Pitch, Quad Flat No-lead Package (QFN) Sawn

Note: T&R quantity 4,000.

Please contact your local Atmel sales office for more detailed ordering information and minimum quantities.

17. Soldering Information

Recommended soldering profile is specified in IPC/JEDEC J-STD-.020C.

18. Package Thermal Properties

Thermal Resistance	
Velocity [m/s]	Theta ja [K/W]
0	40.9
1	35.7
2.5	32.0

19. Package Drawing - 32QN2
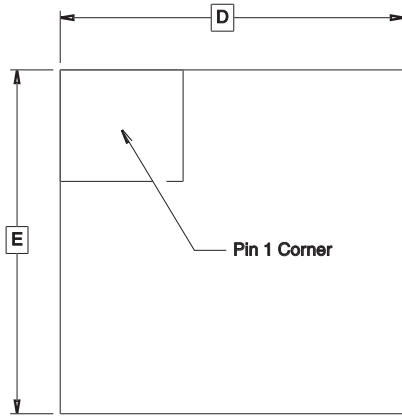
Top View
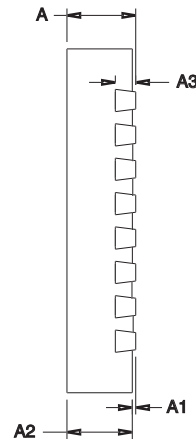
Side View
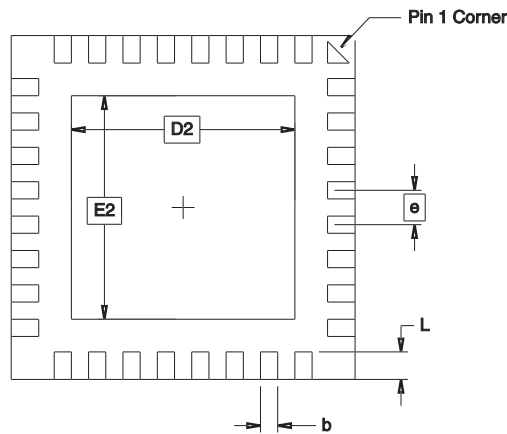
Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		5.00 BSC		
E		5.00 BSC		
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
A	0.80	0.90	1.00	
A1	0.0	0.02	0.05	
A2	0.0	0.65	1.00	
A3		0.20 REF		
L	0.30	0.40	0.50	
e		0.50 BSC		
b	0.18	0.23	0.30	2

Notes: 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-6, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

11/26/07

	Package Drawing Contact: packagedrawings@atmel.com	**TITLE** **32QN2**, 32-lead 5.0 x 5.0 mm Body, 0.50 mm Pitch, Quad Flat No Lead Package (QFN) Sawn	**GPC** ZJZ	**DRAWING NO.** 32QN2	**REV.** A

20. Appendix A - Continuous Transmission Test Mode

20.1 Overview

The AT86RF231 offers a Continuous Transmission Test Mode to support final application / production tests as well as certification tests. Using this test mode the radio transceiver transmits continuously a previously transferred frame (PRBS mode) or a continuous wave signal (CW mode).

In CW mode two different signal frequencies per channel can be transmitted:

- $f_1 = f_{CH} + 0.5$ MHz
- $f_2 = f_{CH} - 0.5$ MHz

Here f_{CH} is the channel center frequency programmed by register 0x08 (PHY_CC_CCA).

Note, in CW mode it is not possible to transmit an RF signal directly on the channel center frequency.

PSDU data in the Frame Buffer must contain at least a valid PHR (see Section 8.1 "Introduction - IEEE 802.15.4 - 2006 Frame Format" on page 79) followed by PSDU data. It is recommended to use a frame of maximum length (127 bytes) and arbitrary PSDU data for the PRBS mode. The SHR and the PHR are not transmitted. The transmission starts with the PSDU data and is repeated continuously.

20.2 Configuration

Before enabling Continuous Transmission Test Mode all register configurations shall be done as follow:

- TX channel setting (optional)
- TX output power setting (optional)
- Mode selection (PRBS / CW)

A register access to register 0x36 and 0x1C enables the Continuous Transmission Test Mode.

The transmission is started by enabling the PLL (TRX_CMD = PLL_ON) and writing the TX_START command to register 0x02.

Even for CW signal transmission it is required to write valid PSDU data to the Frame Buffer. For PRBS mode it is recommended to write a frame of maximum length.

The detailed programming sequence is shown in Table 20-1 on page 175. The column R/W informs about writing (W) or reading (R) a register or the Frame Buffer.

Table 20-1. Continuous Transmission Programming Sequence.

Step	Action	Register	R/W	Value	Description
1	RESET				Reset AT86RF231
2	Register Access	0X0E	W	0x01	Set IRQ mask register, enable IRQ_0 (PLL_LOCK)
3	Register Access	0x04	W	0x00	Disable TX_AUTO_CRC_ON
4	Register Access	0x02	W	0x03	Set radio transceiver state TRX_OFF
5	Register Access	0x03	W	0x01	Set clock at pin 17 (CLKM)
6	Register Access	0x08	W	0x33	Set IEEE 802.15.4 CHANNEL, e.g. 19
7	Register Access	0x05	W	0x00	Set TX output power, e.g. to Pmax

8	Register Access	0x01	R	0x08	Verify TRX_OFF state
9	Register Access	0x036	W	0x0F	Enable Continuous Transmission Test Mode - step # 1
10[1]	Register Access	0x0C	W	0x03	Enable High Data Rate Mode, 2 Mb/s
11[1]	Register Access	0x0A	W	0xA7	Configure High Data Rate Mode
12[2]	Frame Buffer Write Access		W		Write PHR and PSDU data (even for CW mode), refer to Table 20-2 on page 176.
13	Register Access	0x1C	W	0x54	Enable Continuous Transmission Test Mode - step # 2
14	Register Access	0x1C	W	0x46	Enable Continuous Transmission Test Mode - step # 3
15	Register Access	0x02	W	0x09	Enable PLL_ON state
16	Interrupt event	0x0F	R	0x01	Wait for IRQ_0 (PLL_LOCK)
17	Register Access	0x02	W	0x02	Initiate Transmission, enter BUSY_TX state
18	Measurement				Perform measurement
19	Register Access	0x1C	W	0x00	Disable Continuous Transmission Test Mode
20	RESET				Reset AT86RF231

Note: 1. Only required for CW mode, do not configure for PRBS mode.

2. Frame Buffer content depends on desired transmitter operation mode, either PRBS or CW mode.

The content of the Frame Buffer has to be defined for Continuous Transmission PRBS mode or CW mode. To measure the power spectral density (PSD) mask of the transmitter it is recommended to use a random sequence of maximum length for the PSDU data.

To measure CW signals it is necessary to write either 0x00 or 0xFF to the Frame Buffer, for details refer to Table 20-2 on page 176.

Table 20-2. Frame Buffer Content for various Continuous Transmission Modulation Schemes

Step	Action	Frame Content	Comment
12	Frame Buffer Access	Random Sequence	modulated RF signal
		0x00 (each byte)	f_{CH} - 0.5 MHz, CW signal
		0xFF (each byte)	f_{CH} + 0.5 MHz, CW signal

20.3 Register Description

Register 0x36 (TST_CTRL_DIGI):

Register TST_CTRL_DIG enables the continuous transmission test mode.

Bit	7	6	5	4	3	2	1	0	
+0x36	Reserved				TST_CTRL_DIG				TST_CTRL_DIGI
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset Value	0	0	1	0	0	0	0	0	

- **Bit [7:4] - Reserved**

- **Bit [3:0] - TST_CTRL_DIG**

These register bits enable continuous transmission:

Table 20-3. Continuous Transmission

Register Bit	Value	Description
TST_CTRL_DIG	<u>0x0</u>	Continuous Transmission disabled
	0xF	Continuous Transmission enabled
	0x1 - 0xE	Reserved

21. Appendix B - AT86RF231-ZF Extended Temperature Range

21.1 Introduction

Appendix B contains information specific to devices operating at temperatures up to 125°C. Only deviations to the standard device AT86RF231-ZU are covered in this appendix, all other information are similar to previous sections.

Performance figures for 125°C are only valid for device part number AT86RF231-ZF.

21.2 Electrical Characteristics

If not otherwise stated, electrical characteristics for typical operating conditions are similar to figures provided in "Electrical Characteristics" on page 156.

Table 21-1. Recommended Operating Range

No.	Symbol	Parameter	Condition	Min.	Typ.	Max	Units
21.2.1	T_{OP}	Operating temperature range		-40		+125	°C

21.3   Typical Characteristics

The following charts showing each a typical behavior of the AT86RF231. These figures are not tested during manufacturing for all supply voltages and all temperatures. All power consumption measurements are performed with pin 17 (CLKM) disabled, unless otherwise stated.

Power consumption for the microcontroller required to program the radio transceiver is not included in the measurement results.

The power consumption in SLEEP state mode is independent from CLKM master clock rate selection.

The current consumption is a function of several factors such as: operating voltage, operating frequency, loading of I/O pins, switching rate of I/O pins, and ambient temperature. The dominating factors are operating voltage and ambient temperature.

If possible the measurement results are not affected by current drawn from I/O pins. Register, SRAM or Frame Buffer read or write accesses are not performed during current consumption measurements.

21.4   Active Supply Current

21.4.1   P_ON and TRX_OFF states

Figure 21-1. Current Consumption in P_ON State
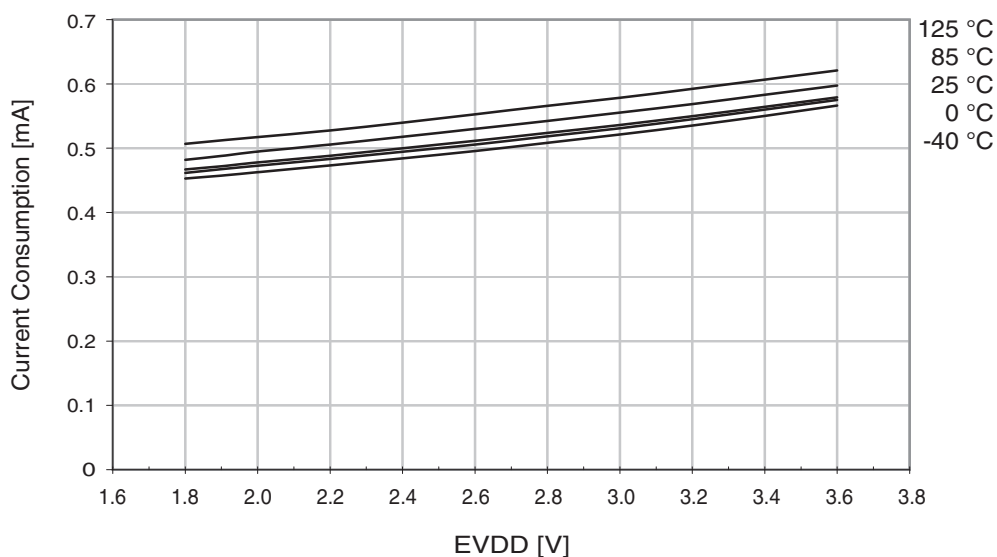
Figure 21-2. Current Consumption in TRX_OFF State
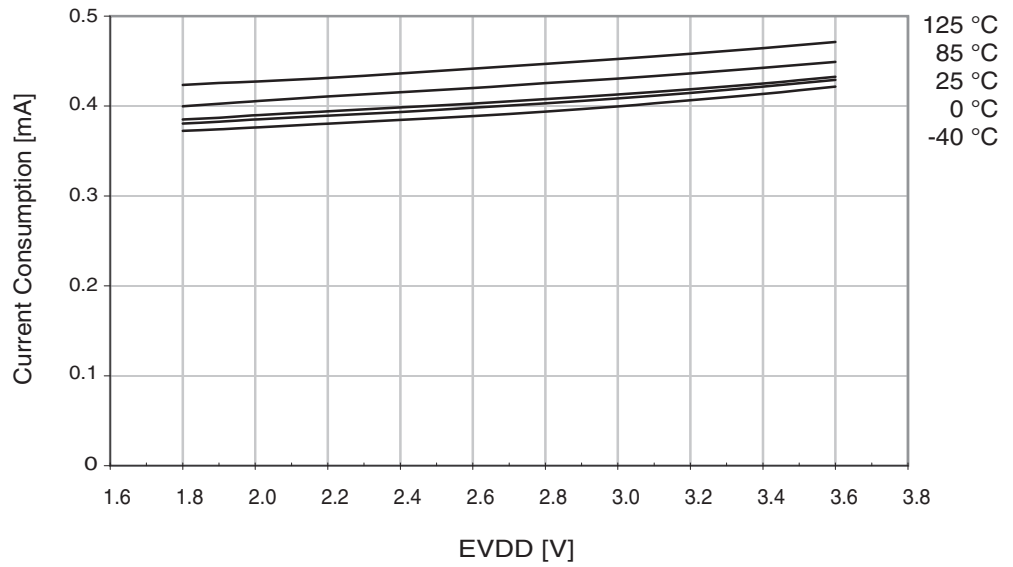
21.4.2   PLL_ON state

Figure 21-3. Current Consumption in PLL_ON State
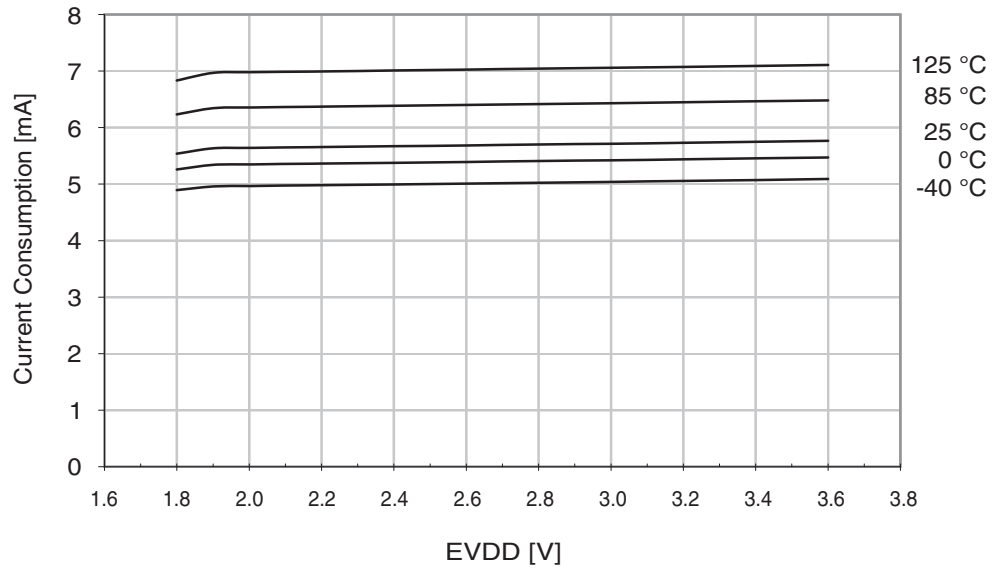
21.4.3   RX_ON state

Figure 21-4.   Current Consumption in RX_ON State - High Sensitivity
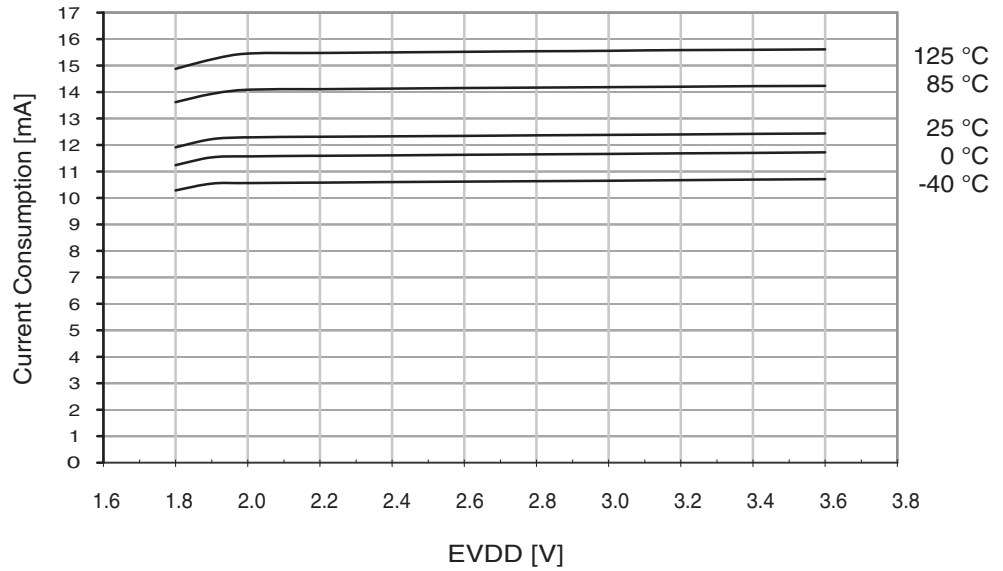
Figure 21-5.   Current Consumption in RX_ON State - High Input Level
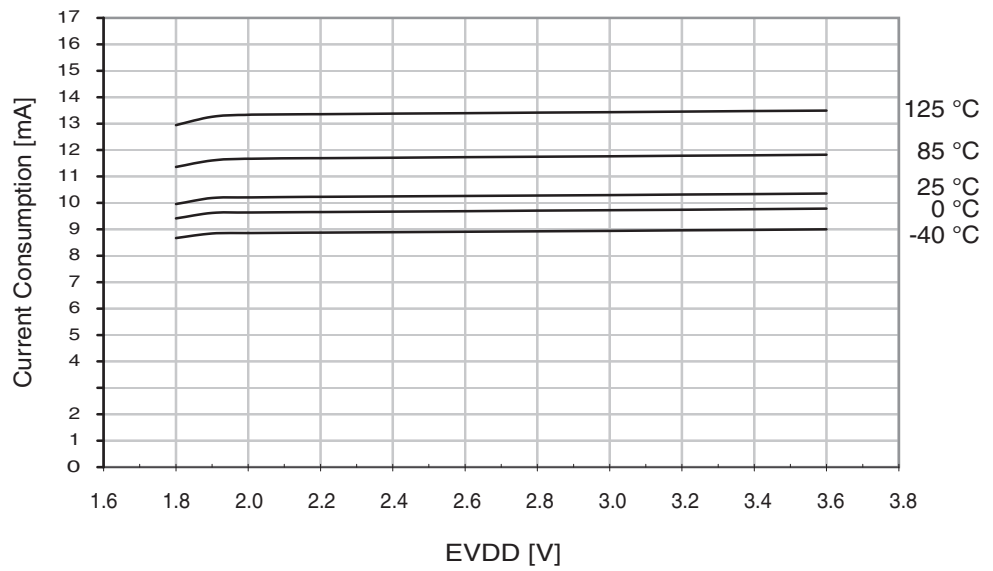
Figure 21-6. Current Consumption in RX_ON State - Reduced Sensitivity
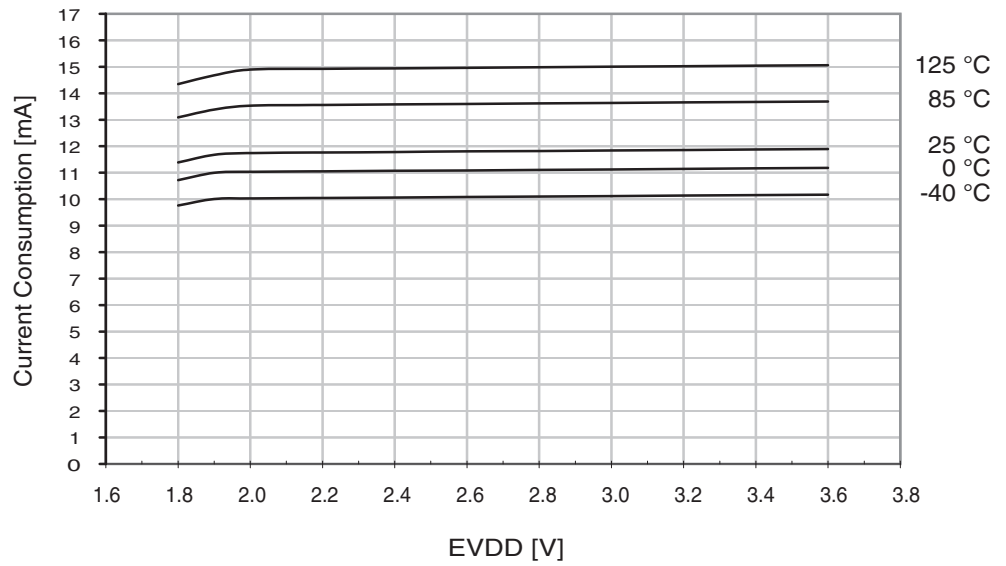
21.4.4   TX_BUSY state

Figure 21-7. Current Consumption in TX_BUSY State - Minimum Output Power
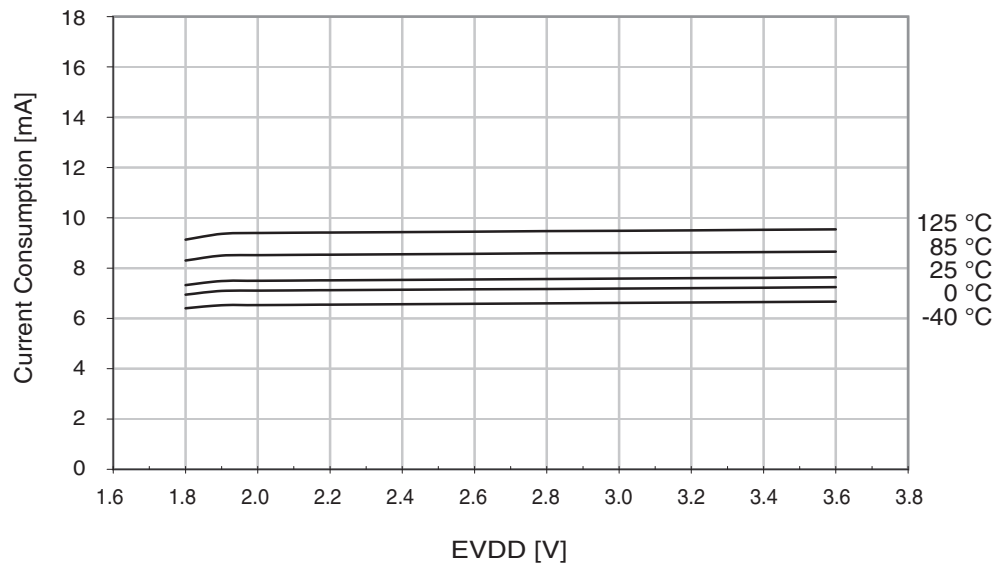
Figure 21-8. Current Consumption in TX_BUSY State - Output Power 0 dBm
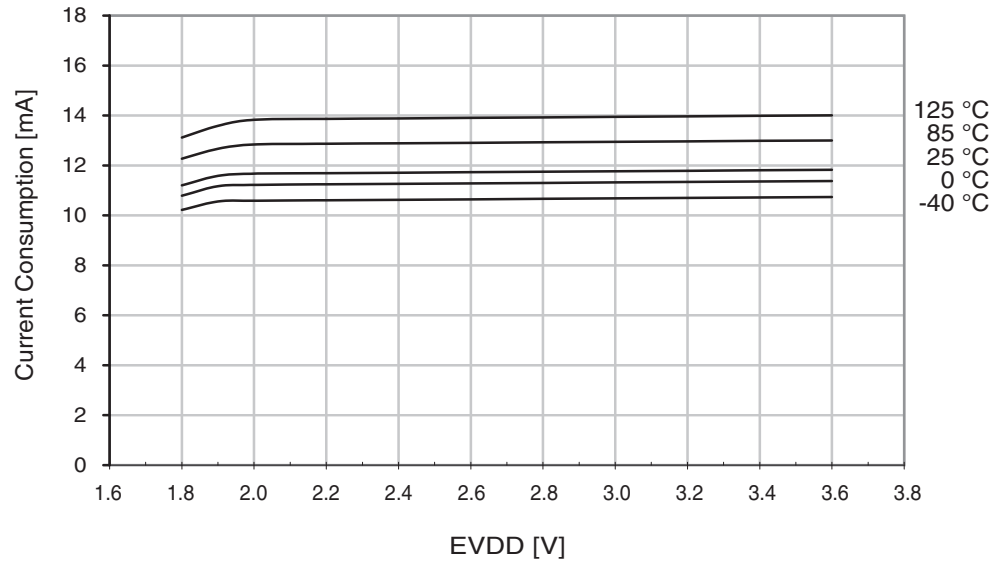
Figure 21-9. Current Consumption in TX_BUSY State - Maximum Output Power
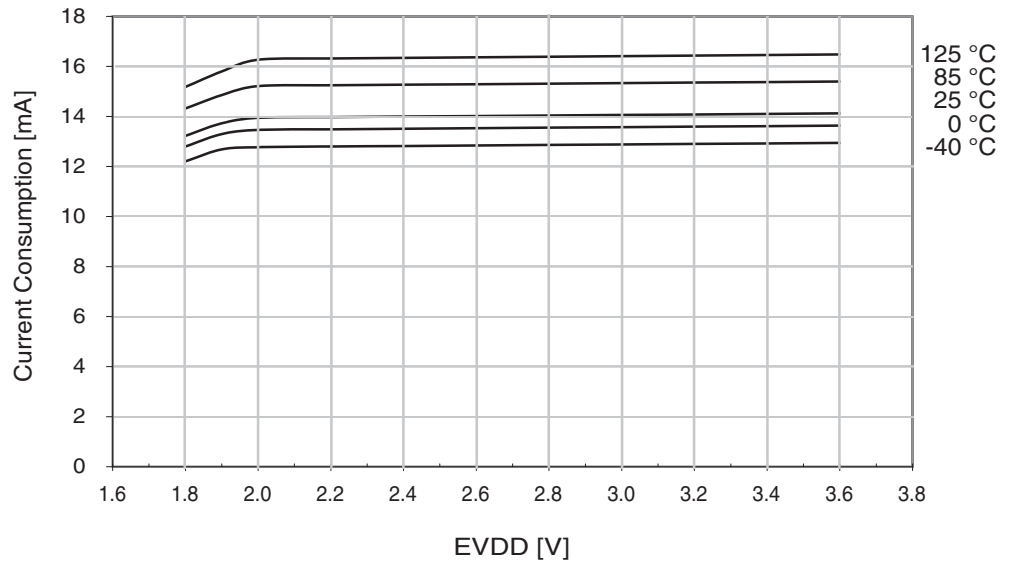
21.4.5   SLEEP

Figure 21-10. Current Consumption in SLEEP
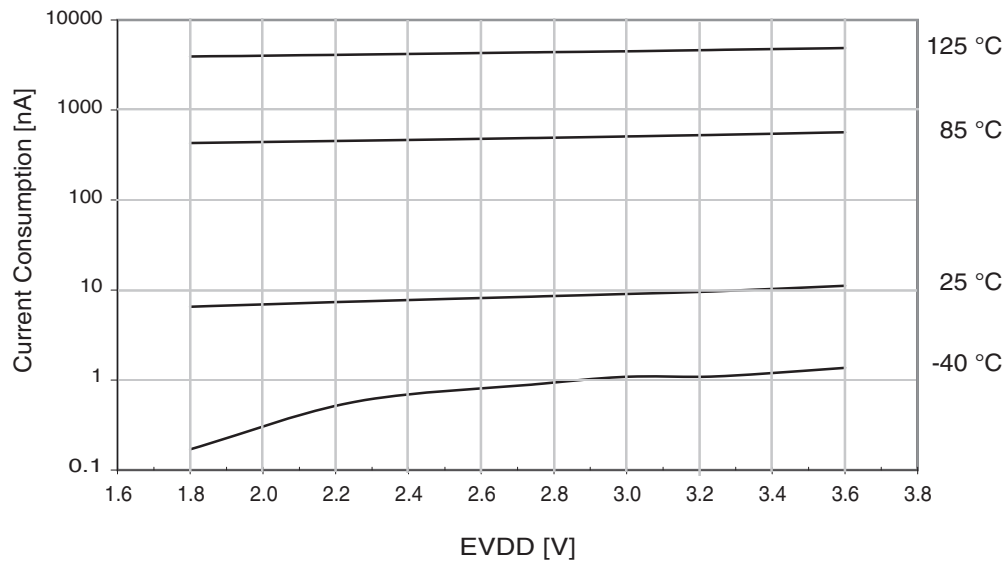
21.5 State Transition Timing

Figure 21-11. Transition Time from EVDD to P_ON (CLKM available)
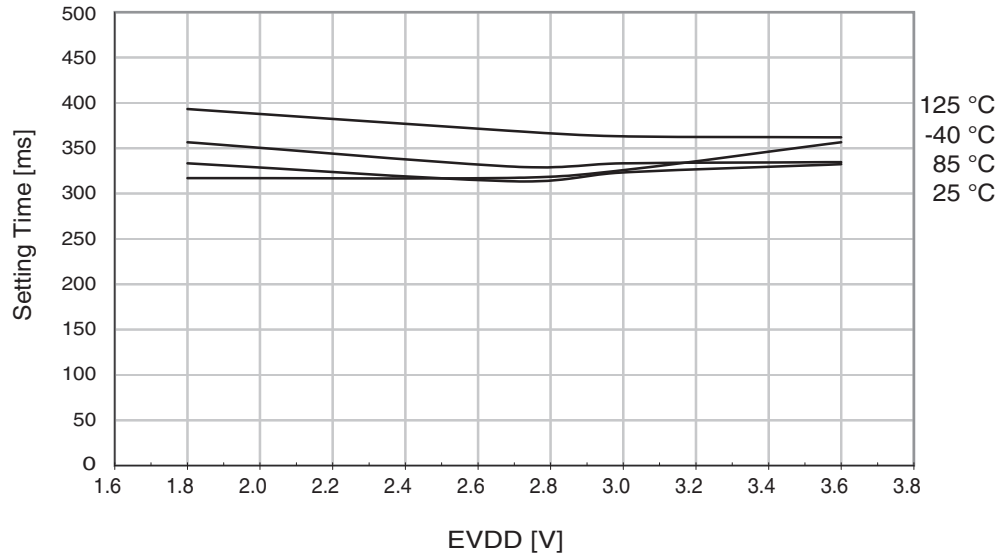
Figure 21-12. Transition Time from SLEEP to TRX_OFF (IRQ_4 (AWAKE_END))
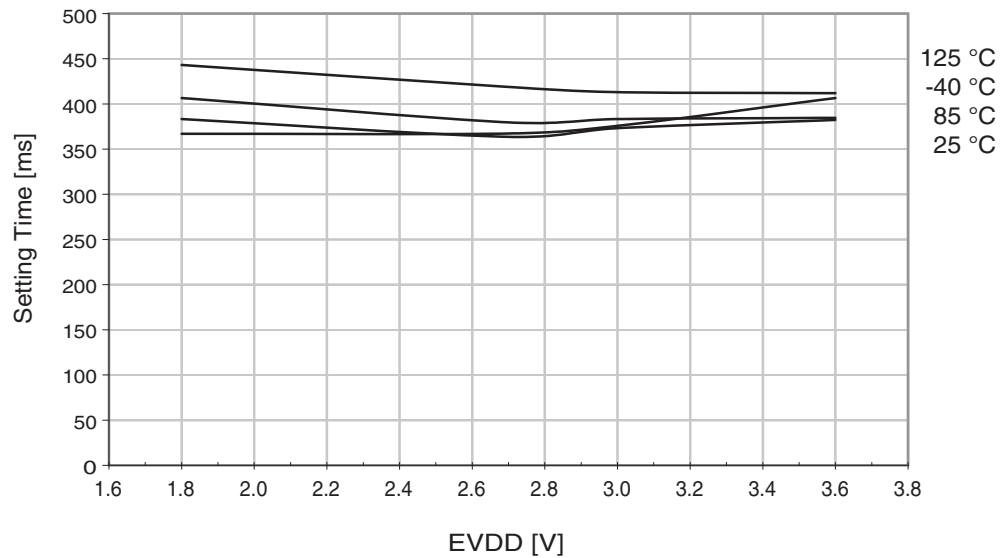
Figure 21-13. Transition Time from TRX_OFF to PLL_ON
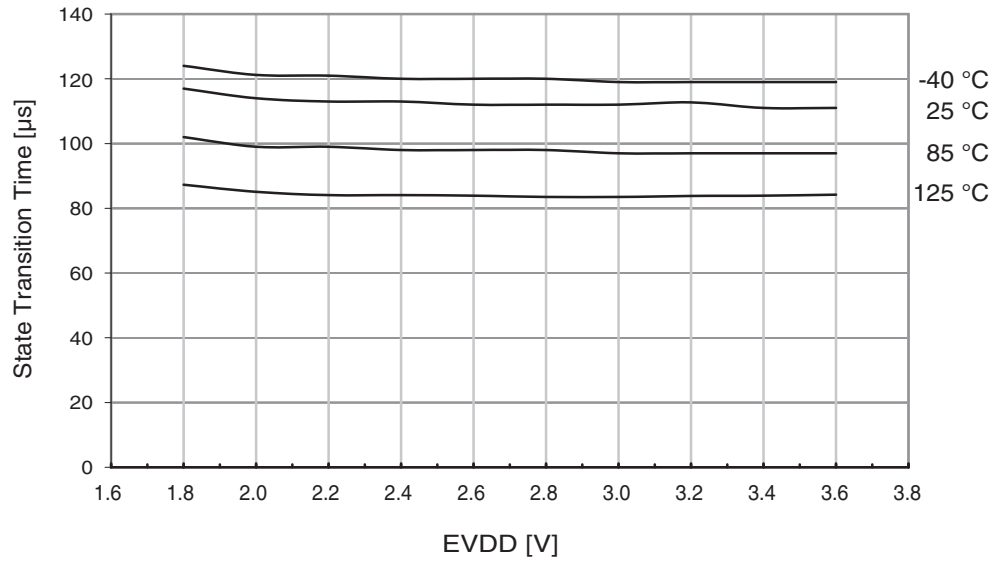
21.6 Receiver Performance

21.6.1 Sensitivity

Figure 21-14. Sensitivity
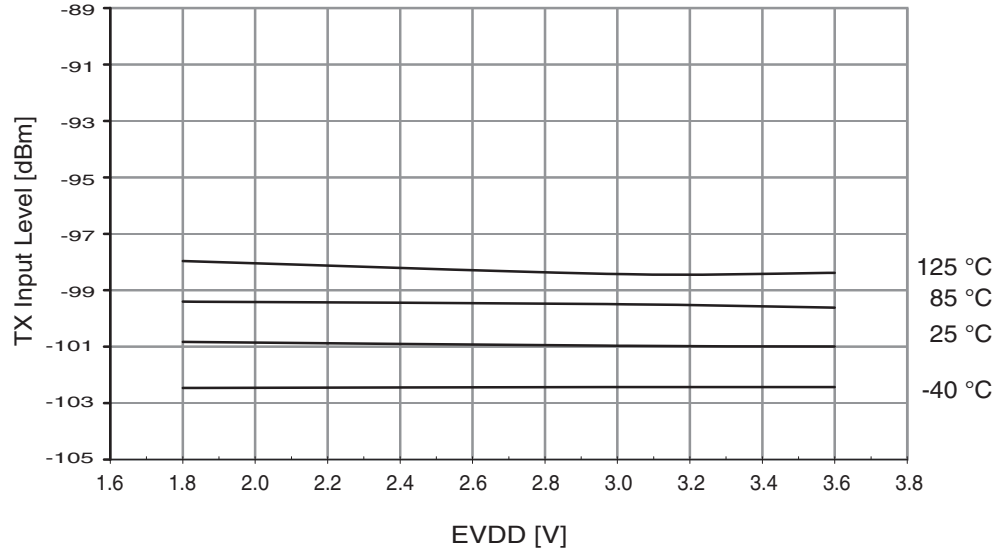
21.6.2 Adjacent & Alternate Channel Selectivity (ACRx)

Figure 21-15. Adjacent and Alternate Channel Selectivity
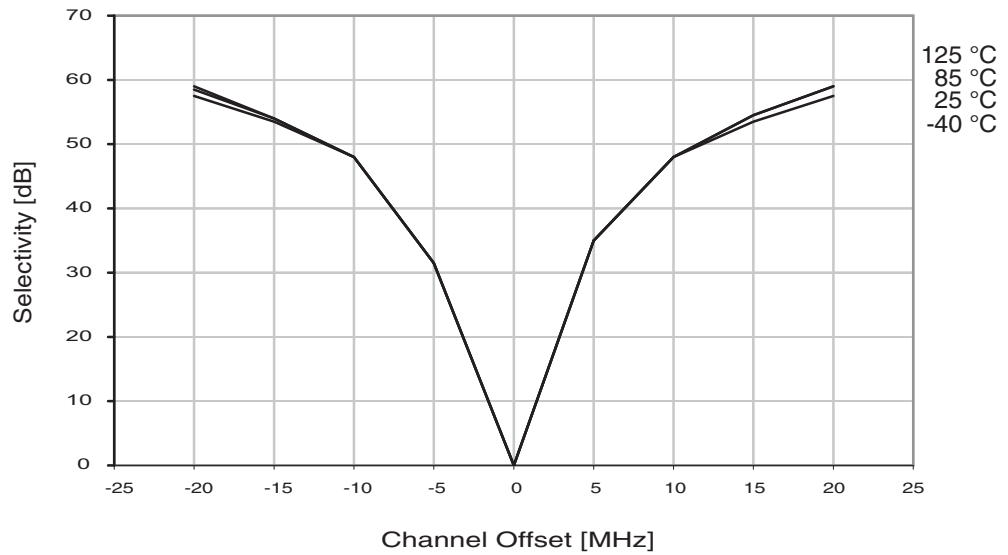
21.6.3 RSSI

Figure 21-16. RSSI
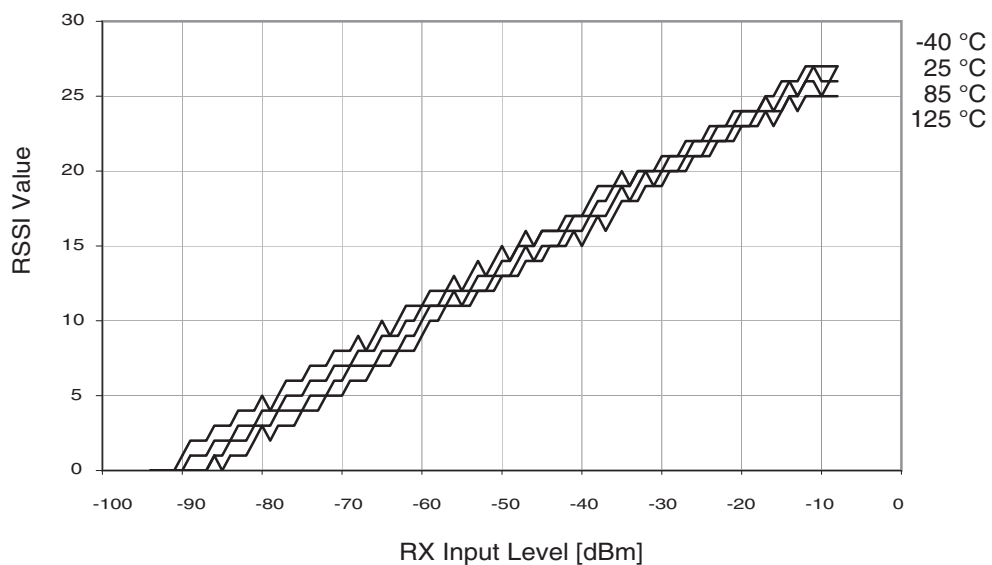
21.7   Transmitter Performance

21.7.1   TX Output Power vs. TX Power Level

Figure 21-17. TX Output Power vs. TX_PWR (EVDD = 3.0V, CH=19)
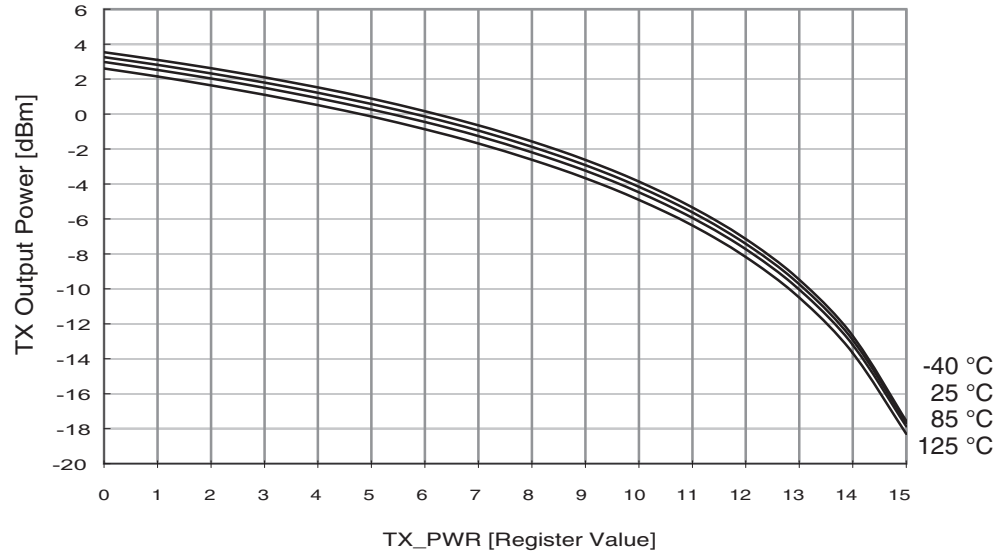
21.7.2   TX Output Power vs. EVDD

Figure 21-18. TX Output Power vs. EVDD (TX_PWR = 0, CH=19)
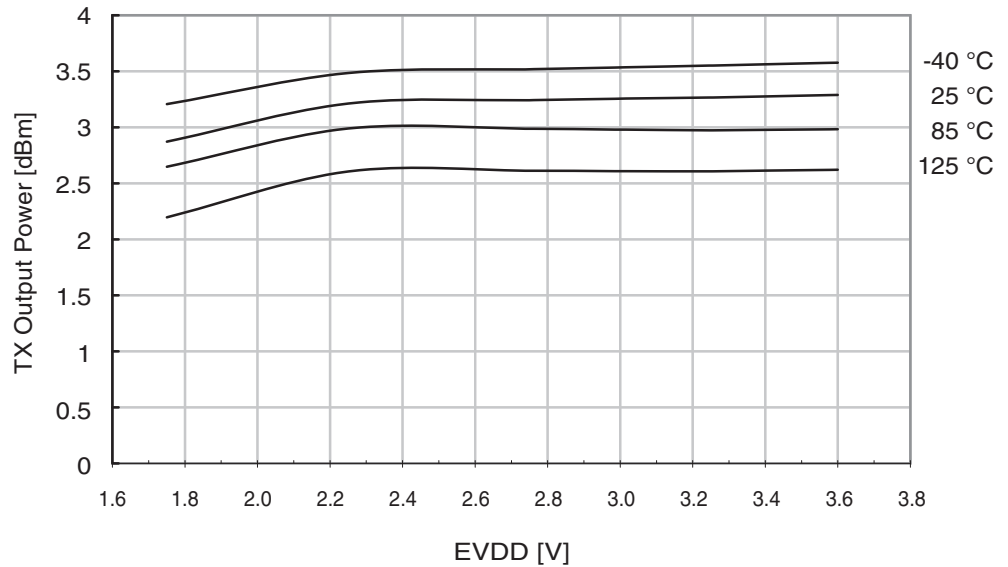
21.7.3   TX Output Power vs. Channel

Figure 21-19. TX Output Power vs. Channel (EVDD = 3.0V, TX_PWR = 0)
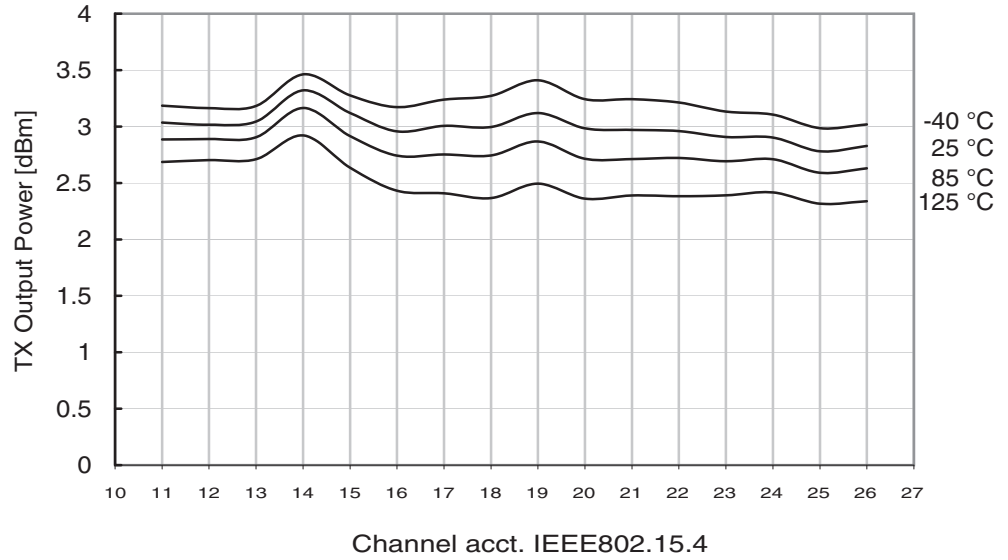
21.7.4   TX EVM vs. EVDD

Figure 21-20. Error Vector Magnitude (EVM) vs. EVDD (TX_PWR = 0, CH=19)
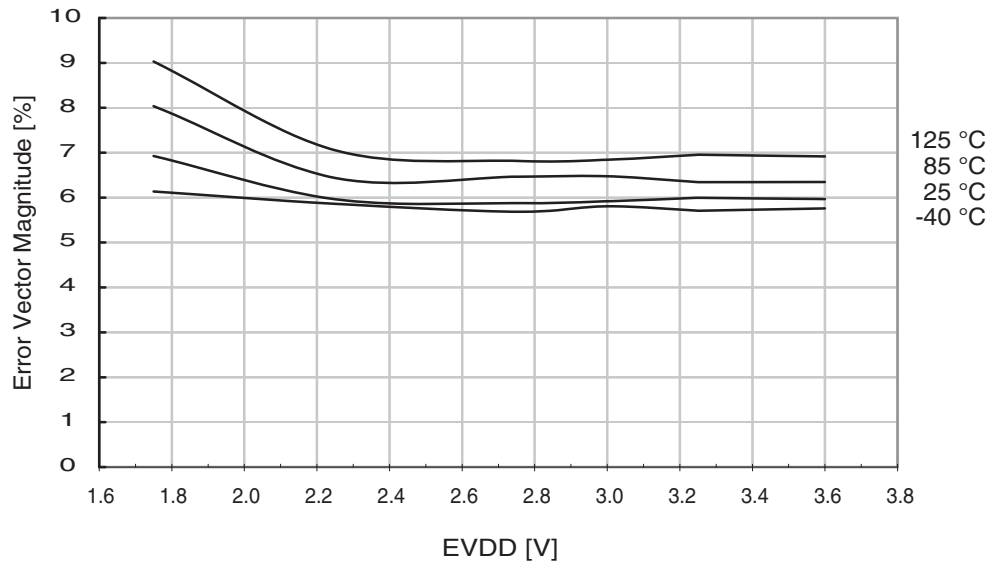
22. Appendix C - Errata

22.1 AT86RF231 Rev.A

No known errata

23. Revision history

23.1 Rev.8111C - 09/09

1. Updated the datasheet with a new device AT86RF231-ZF.

2. Added "Appendix B - AT86RF231-ZF Extended Temperature Range" on page 178

3. Editorial updates.

23.2 Rev.8111B - 02/09

1. Updated figures and graphics in sections: 5.,6., 8.,9.,11., 12.and 13.

2. Changed register and sub-register names in "AT86RF231 Extended Feature Set" on page 128.

3. Editorial changes.

23.3 Rev.8111A - 05/08

1. Initial revision

References

[1]	IEEE Std 802.15.4™-2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)
[2]	IEEE Std 802.15.4™-2003: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)
[3]	ANSI / ESD-STM5.1-2001: ESD Association Standard Test Method for electrostatic discharge sensitivity testing - Human Body Model (HBM).
[4]	ESD-STM5.3.1-1999: ESD Association Standard Test Method for electrostatic discharge sensitivity testing - Charged Device Model (CDM).
[5]	NIST FIPS PUB 197: Advanced Encryption Standard (AES), Federal Information Processing Standards Publication 197, US Department of Commerce/NIST, November 26, 2001
[6]	AT86RF231 Software Programming Model

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