APPENDIX C: PRODUCT DESCRIPTION

CIRCUIT DESCRIPTION

1 SCANNER UNIT

1-1 PA UNIT

The GATE signal from the IF unit is passed through J3 (pin 1) and applied to the driver amplifier (Q6, Q7). The amplified signal drives the power MOS FET (Q4, Q5) and is applied to the primary winding of pulse-transformer (T1). Then a high voltage is output from the secondary winding and is applied to the magnetron. The magnetron outputs a microwave signal.

The DC-DC converter consists of IC5, Q11, Q16, converts the supply voltage (+30 V) into +350 V. +350 V is applied to the primary winding of pulse-transformer (T1). Another DC-DC converters consist of (IC2, Q8, Q14 and IC3, Q9, Q17) converts +30 V into +14 V and +7 V respectively. +14 V is applied to the motor and IF unit. + 7 V is applied to the magnetron heater and IF unit.

1-2 IF UNIT

1-2-1 SERIAL-PARALLEL CONVERSION CIRCUIT

Some of the signals between the DISPLAY UNIT and SCANNER UNIT are passed through the coaxial cable after being converted into serial signals. The serial-parallel (parallel-serial) conversion circuit in CPU (IC11) re-converts these serial signals via the coaxial cable to their original state (or converts parallel signal into serial signals for sending the signals to the SCANNER UNIT). IC21, Q31, Q35 are used for the interface circuit.

1-2-2 RECEIVER AND DETECTOR CIRCUIT

The IF circuit amplifies the 60 MHz IF signal from the front-end and detects it for conversion into a video signal. The video signal is output from the SCANNER UNIT and then applied to the DISPLAY UNIT via the coaxial cable.

The signal from the front-end (J6) is amplified and separated at the buffer amplifier (Q39 and Q40) to the receiver circuit and tuner meter circuit respectively.

The buffer-amplified signal is amplified at the IF (Q1) and LOG (Q3–Q20) amplifiers. Bandwidth filters (D1, D2) are used at the both side of IF amplifier (Q1) for IF band width selection (3 MHz or 10 MHz).

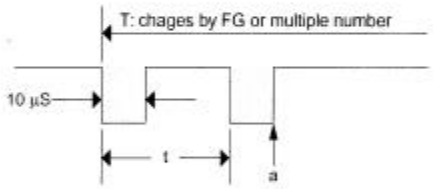
The LOG amplifier circuit connects 6-stage of same amplifiers, and saturates in order from last stage amplifier according to input level. Also the LOG amplifier circuit detects signals at each stage and applies to Q21, Q22. The detected signals from each stage are also synthesized at Q21, Q22, and are mixed with the synchronizing signal at IC5. The video signal from IC5 is amplified at the buffer amplifiers (Q23, Q24) and is then applied to the DISPLAY UNIT.

1-2-3 AUTO TUNING CIRCUIT

A portion of the IF signals from the front-end (J6) is amplified at the buffer amplifier (Q40) and is then applied to the tuner meter circuit (Q41, D15, L4). The detected voltages are compared at CPU (IC11) to obtain a 60 MHz drifted value. The drifted value is passed through the interface circuit (Q31, Q35) and is then applied to the DISPLAY UNIT.

1-2-4 TRANSMITTER PULSE GENERATION CIRCUIT

This circuit generates a synchronizing signal based on the VCO (IC6) signal, and SHM signals from the CTRL unit for indicating the antenna angle on the display. The VCO (IC6) oscillates according with the voltage from the D/A converter (IC12) controlled by the CPU. And an 1/15 signal is applied to the CPU, 1/10 signal to the motor circuit, 1/4 and 1/2 signals are applied to the transmitting trigger circuit. 1800 pulses or 3600 pulses an antenna rotation are necessary for transmitting, the VCO signal is divided by divider circuit (IC10, IC15). The divided number is switched by IC12. The output signal is also applied to the IC1–IC4 and generates below wave form.



"t" is generally about 50 µS. When applied SHM signal, "t" changes to about 100 µS. This signal is mixed with a video signal and applied to the DISPLAY UNIT. And then SHM signal is detected and compared the difference "t". Actual transmitting timing is "a" of above illustration.

The above synchronizing signal is used as the trigger signal for the pulse signal which is decided pulse width by IC1, Q26–Q29, C89, R130–R137. The pulse signal is level-converted at IC25, C109, Q30 and applied to the PA unit

1-2-5 MONITOR CIRCUIT

The magnetron current, heater current, high voltage and scanner voltage from PA unit are amplified at IC17 and applied to the A/D input of CPU (IC11). The CPU analyzes and outputs each information to the DISPLAY UNIT.

1-3 RF UNIT

The RF unit consists of a magnetron, circulator, diode limiter and front-end.

The magnetron generates high-energy oscillation for the input pulse. The circulator is used as a transmit/receive switch. The diode limiter is used for protecting the receiver section at the front-end from excessively strong signals.

The front-end consists of an amplifier, local oscillator and D.B.M (double ballanced mixer). The microwave signal, which inputed from the circulator, is amplified at the low-noise amplifier and then enters the D.B.M. A microwave signal is then mixed with a local oscillator signal to be converted into a 60 MHz IF frequency. The frequency of the local oscillator circuit is adjusted with the tuning voltage.

1-4 CTRL UNIT

The CTRL unit consists of IC1, J1, motor and metal plate for installation.

When the antenna is rotating, the base signal for the antenna angle is generated by the metal plate interrupting IC1's signal at once a rotation. The generated signal is applied to the IF unit, and then SHM signal is generated in the IF unit.

MF1 is a pulse motor, which gear ratio of 7.5 : 1.

2 DISPLAY UNIT

2-1 MAIN UNIT

The MAIN unit consists of a regulator circuit, video A/D circuit and interface circuit.

2-1-1 REGULATOR CIRCUIT

The regulator circuit supplies 30 V for SCANNER UNIT, 5 V and 3.3 V for LOGIC unit, LCD backlight voltage for LCD backlight circuit.

1) INPUT CIRCUIT

10.2–42 V DC power is applied to the MAIN unit via the PWR connector (J5) and is then passed through the line filter (L1, C21–C24) to the regulator circuit. The line filter filters RF signals to prevent their application to the switching circuit.

2) SWITCH CIRCUIT

SW1 and SW2 from MAIN unit are connected to the power switch (S1) on the SW unit. When power switch (SW unit; S1) is open, the power voltage is applied to the regulator circuit (Q12, Q13) and the regulator circuit activates power control circuit (IC6).

3) SWITCHING CIRCUIT

IC6 includes an oscillator circuit and a switching control circuit. IC6 oscillates 60 kHz frequency signal and generates sawtooth waves at C52. The time constant circuit (R46 and C52) sets the oscillation frequency.

IC6 (pins 9 and 10) controls the switching circuit (Q6, Q7), and the primary winding of transformer (T1) is alternately connected to and disconnected from the DC power.

4) OUTPUT AND RECTIFIER CIRCUITS

The secondary winding of T1 output 30 V. 30 V is rectified by D3, D4, L4, C30 and is applied to the SCANNER UNIT, LCD back light circuit and 5 V DC-DC converter circuit.

5) OUTPUT VOLTAGE CONTROL CIRCUIT

30 V output is divided by R28–R35 and is applied to the shunt regulator (IC3). When output voltage of IC3 increases due to increase of the 30 V, a base-current of the photo-coupler (IC4) increases and a corrector-emitter's voltage decreases. At this time, IC6 (pin 2) reduces output voltage and the width of output pulse between pin 9 and pin 10 becomes narrow. And also the interval time of activating Q6, Q7 will be short.

Thus the working time of primary winding of transformer (T1) becomes short, and the output of secondary winding of T1 decrease. This feedback circuit controls the constant output voltages even if resistance of output or input voltage is changed.

6) LOW VOLTAGE PROTECTION CIRCUIT
The input voltage of comparator (IC5) is divided by R38 and R39. When the divided and applied voltage is lower than 9 V, the output signal of comparator (IC5) drives Q15. Then Q15 output "High" signal to IC6 (pin 4), and then IC6's output is turned OFF.

7) LCD BACKLIGHT CIRCUIT
The LCD backlight circuit consists of IC8, Q10, D9, L5 and C37. IC8 employs DC-DC converter IC. The output voltage is passed through the voltage divider circuit (R16, R17) and applied to the LCD backlight controller (IC1a, pin 3). Another input of LCD backlight controller (IC1a, pin 2) is a brightness signal from LOGIC unit, and then IC1a outputs LCD backlight control signal.

8) 5 V DC-DC CONVERTER CIRCUIT
The 5 V DC-DC converter circuit consists of IC7, Q18, L6, C62, R59 and R60. IC7 also employs DC-DC converter IC.

9) 3.3 V DC-DC CONVERTER CIRCUIT
The 3.3 V DC-DC converter circuit (Q19, Q20, R61, R63) converts 5 V line into 3.3 V constant voltage.

2-1-2 VIDEO ANALOG/DIGITAL CIRCUIT

The video analog/digital circuit consists of the A/D converter circuit for video signals, and the circuit that separates the synchronizing signal and video signals from the SCANNER UNIT.

1) SYNCHRONIZING SIGNAL SEPARATION CIRCUIT
IC110b cuts off the voltage determined by R142 and R143 from the average voltage of input video signals. And the output voltage is used for the base voltage of the comparator circuit (IC104) that separates the synchronizing signal from video signal.

The video signal without synchronizing signal is applied to the IC105–IC107 and divided a trigger signal and SHM signal. These signals are applied to the LOGIC unit.

2) VIDEO SIGNAL PROCESSING CIRCUIT
• NOISE REDUCTION CIRCUIT
The noise reduction circuit (Q103, Q104, R110–R112, C106, C107) is a low-pass filter that switching passband width according to the transmitting pulse width, and reduces unwanted noise.

• FTC (RAIN) CIRCUIT
The FTC (Fast Time Constant) circuit (Q109–Q113, C112–C116) is a low-pass filter that controlled by the RAIN adjustment, and removes echo signals caused by snow or rain.

• STC CIRCUIT
The STC (Sensitivity Time control) circuit (IC120, R146–R148, C124–C126) used for reducing the reflection from surface of the sea. This circuit controlled by the voltage according to the STC control from the LOGIC unit.

• SLICE LEVEL COMPOSITE CIRCUIT
Each voltage of FTC, STC, GAIN are composted at IC108, and made a base voltage of the video A/D.

• VIDEO A/D
The voltage from the slice level composite circuit is divided by R134 and R135, and each voltage is applied to the 3-stage of comparator (IC109). The applied each voltage is A/D converted at IC109 by compared with the video signal.

• TUNING DETECTOR CIRCUIT
The signal at the time just after transmitting is made at IC114, R154, R155, C138. Then the video signal (without the reflection signal) is cut out, and used it for the automatic tuning and etc.

• NOISE DETECTOR CIRCUIT
The noise (without reflection signal) at the time just before transmitting is smoothed at the noise detector circuit (IC110a), and applied to the CPU to control the automatic gain level. IC122 works to cancel the interrupting signal from other ship's transmission (microwave).

2-1-3 INPUT/OUTPUT CIRCUIT

1) POSITION DATA INPUT CIRCUIT
Position data input circuit consists of IC115, IC116. The NMEA signals from the external connector (J7, pins 3, 4) are shaped wave form at the Schmitt circuit (IC115) via the photo-coupler (IC116), and are then applied to the LOGIC unit via J1 (pin 28).

2) BEARING DATA INPUT CIRCUIT
Bearing data input circuit consists of IC115, IC117. The NMEA signals from the external connector (J6, pin 3, 4) are shaped wave form at the Schmitt circuit (IC115) via the photo-coupler (IC117), and are then applied to the LOGIC unit via J1 (pin 26).

3) NMEA OUTPUT CIRCUIT
NMEA output circuit consists of Q114, Q115, D105. The NMEA signals from the LOGIC unit are input to the MAIN unit via J1 (pin 29). The signals are buffer-amplified and level-shifted at NMEA output circuit, and are then applied to the external connector (J7, pin 1).

4) SERIAL DATA OUTPUT CIRCUIT
Serial data output circuit consists of IC119, Q116, Q117. The signals from the LOGIC unit are buffer-amplified and output to the SCANNER UNIT via the external connector (J4).

2-2 LOGIC UNIT

The LOGIC unit consists of I/O, FPGA, CPLD, SRAM and CPU that are 32 bit ARM RISC micro-controller. CPU and a control circuit control all functions.

1) CPU (IC6)
The CPU (IC6) is a 32-bit RISC CPU and acts as a computer circuit to control all functions and to respond to all kind of interruptions except the PPI image processing. The CPU uses a clock signal from X1.

The CPU (IC6) has a DRAM for using to load the program from the flash ROM at the start up. Thus the CPU can act the program operation at high-speed.

2) I/O CONTROLLER (IC10)
IC10 is an I/O controller which controls the chip select signal of memories, timer function, UART function, DMA (Direct Memory Access) controller and etc.

Pins 61, 66, 67 and 95–100 work as I/O pins for key scan of each operation.

Position information of owns ship is applied to pin 43 (U0RXD) via the N_RX terminal (J1, pin 28) on the MAIN unit.

A bearing signal of owns ship is applied to pin 39 (U1RXD) via the C_RX terminal (J1, pin 26) on the MAIN unit.

An N+1 direction signal is applied to pin 37 (BINT1) via the AUX terminal (J1, pin 25) on the MAIN unit.

An SHM signal (Head bearing) is applied to pin 36 (BINT2) via the SHM terminal (J1, pin 5) on the MAIN unit.

A communication data from the sub CPU in the SCANNER UNIT is applied to pin 35 (BINT3) via the S_DAT terminal (J1, pins 23, 24) on the MAIN unit.

An alarm signal from IC18 is amplified at the buffer amplifier (IC12) and applied to the pin 34 (BINT4).

Pin 46 (U0TXD) echoes position information of owns ship input from pin 43 to MAIN unit.

Pin 40 outputs a communication data to the sub CPU in the SCANNER UNIT via the buffer amplifier on the MAIN unit.

3) RESET IC (IC7)
IC7 is a reset IC for CPU (IC6) and I/O controller (IC10) when turning power ON.

4) ROM (IC5, IC3)
IC5 is 4 Mbits flash ROM, stores a system operating program for IC6 and configuration data for IC18. This flash ROM can be updated or re-programmed from outside via the interface connector (J1).

IC3 is a serial EEPROM, which backuped while power OFF such as the data of setup menu.

5) SERIAL A/D CONVERTER (IC1)
IC1 is an 8 bits×4 channels serial A/D converter, which converts STC and TUNE signals to digital signal.

6) D/A CONVERTER (IC2)
IC2 is an 8 bits×6 channels D/A converter, which controls the LCD brightness, display contrast, key panel and STC setting, GAIN setting.

7) FIELD MEMORY (IC4)
IC4 is a 4 Mbits field memory which stores text of image data for display, and also stores control signal and blanking signal for LCD.

8) CPLD (IC16)
IC16 is a CPLD (Complex programmable Logic Device), which controls a sampling clock for the PPI. IC16 generates sampling master clocks for each range (determined CPU signal) using the doubling (at inside of IC16) clock from crystal oscillator (X1).

Master sampling frequency: 52.096 MHz

Range [NM]	Sampling frequency	Devided No.	Range [NM]	Sampling frequency	Devided No.
0.125 (1/8)	52.096 MHz	1/1	4	3.256 MHz	1/16
0.259 (1/4)	52.096 MHz	1/1	6	2.171 MHz	1/24
0.5 (1/2)	26.048 MHz	1/2	8	1.628 MHz	1/32
0.75 (3/4)	17.365 MHz	1/3	12	1.085 MHz	1/48
1	13.024 MHz	1/4	16	814 kHz	1/64
1.5	8.683 MHz	1/6	24	543 kHz	1/96
2	6.512 MHz	1/8	32	407 kHz	1/128
3	4.341 MHz	1/12	36	362 kHz	1/144

9) RAM (IC15, IC20)
IC15 is a 256 kbits SRAM, which memories the sampled data for 2 transmission at the sampling frequency.

IC20 are used for video RAMs for the echo trail screen and PPI screen. This chip has a capacity of 1 M bits.

10) FPGA (IC18)
IC18 is a FPGA (Field Programmable Gate Array), which consists of an SRAM having a capacity of equivalen to about 10000 gates.