SECTION 2 CIRCUIT DESCRIPTION

2-1 RECEIVER CIRCUITS

2-1-1 RF CIRCUIT (RX UNIT)

Received signals enter the antenna connector (J3) and pass through a band-pass filter (C4–C7, C11–C13, D3, D4, L1, L2). The filtered signals are applied to an pre-amplifier (Q2). The pre-amplified signals are applied to a band-pass filter (C17, C18, C23, C31, C36–C38, D5, D7, L6, L24), and applied to an RF-amplifier (Q3). The RF-amplified signal passes through a band-pass filter (C44–C47, C51–C53, D8, D9, L7, L9), and then applied to the 1st mixer circuit.

2-1-2 1ST MIXER AND 1ST IF CIRCUITS (RX UNIT)

The 1st mixer circuit converts the received signals to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing a PLL frequency, only the desired frequency can be passed through a pair of crystal filters at the next stage of the 1st mixer.

The filtered signals are applied to a 1st mixer (IC6, pin 4) and are then mixed with a 1st LO signal from the PLL circuit to produce a 30.875 MHz 1st IF signal.

The 30.875 MHz 1st IF signal is applied to crystal band-pass filter (FI1). FI1 is an MCF (Monolithic Crystal Filter) which suppresses out-of-band signal. The 1st IF signal is applied to the 2nd mixer circuit (IC5, pin 16) via the buffer amplifier (Q8)

2-1-3 2ND IF AND DEMODULATOR CIRCUITS (RX UNIT)

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double superheterodyne system (which converts receive signals twice improves the image rejection ratio and obtains stable receiver gain.

The 1st IF signal is applied to a 2nd mixer (IC5, pin 16) and is then mixed with a 2nd LO signal to produce a 455 kHz 2nd IF signal.

The 455 kHz 2nd IF signal is applied to a ceramic band-pass filter (FI2) where unwanted signals are suppressed and then to a limiter amplifier section in system IC (IC5, pin 5).

IC5 contains the local oscillator circuit, quadrature detector circuit, noise filter circuit, IF amplifier, limiter amplifier, noise amplifier, and so on. The local oscillator section and X1 generate 30.42 MHz for the 2nd LO signal.

The 2nd LO signal from the limiter amplifier (IC5, pin 5) is applied to the quadrature detector section (IC5, pin 11 and ceramic discriminator X2) to demodulate the 2nd IF signal into an AF signal. The AF signal is output from pin 9 of IC5.

2-1-4 SQUELCH CIRCUIT (RX AND LOGIC UNITS)

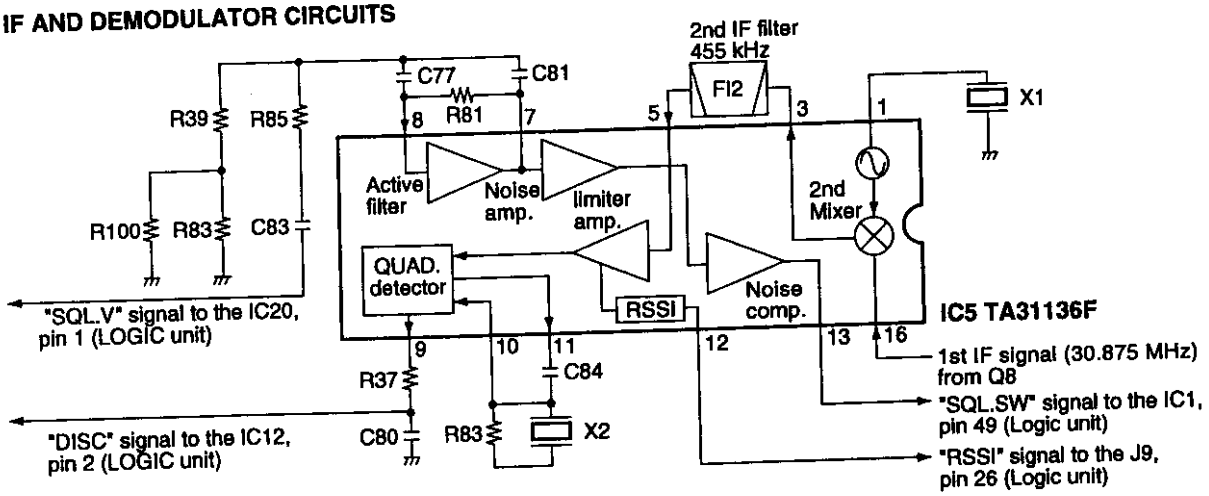
A squelch circuit cuts out AF signals when no RF signal is received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switches.

The squelch switching signal from IC5, pin 13 is applied to the [SQL] select switch (LOGIC unit; IC20, pin1) via the "SQL.V" signal. IC20 selects the squelch switch of R2 (on FRONT unit) or R91 (on LOGIC unit). When the [LOCAL INHIBIT] switch is "OFF", the squelch switch selects R2 (on FRONT unit). When the [LOCAL INHIBIT] switch is "ON", the squelch switch selects R91 (on LOGIC unit).

2-1-5 AF AMPLIFIER CIRCUIT (RX AND LOGIC UNITS)

The AF signal outputs from pin 9 of IC5 (RX unit) is applied to pin 2 of IC12 (LOGIC unit), and then applied to pin 3 of IC13 (LOGIC unit) which functions as a high-pass and low-pass filter via a de-emphasis circuit. The filtered signal is output from pin 7 of IC13 (LOGIC unit) and is the applied to the [VOLUME] control (R1) on the FRONT PANEL through an AF mute switch (LOGIC unit; Q10 and Q11). When the squelch is closed, Q10 and Q11 cuts off the AF signal as an AF mute switch. The AF signal is power-amplified at an AF power amplifier (LOGIC unit; IC15) to drive a speaker.

• **2nd IF AND DEMODULATOR CIRCUITS**



2-2 TRANSMITTER CIRCUITS

2-2-1 MICROPHON AMPLIFIER CIRCUIIT (LOGIC UNIT)

The microphone amplifier circuit (IC16) amplifies the audio signals from the microphone. The amplified signal is mixed with the "LI" signal from IC16 (on the LOGIC unit) and "MOD–MUTE" signal from Q12 and Q13 (on the LOGIC unit) at the mixer amplifier (IC17). The mixed signal passes through the high-pass and low-pass filter (IC18) via the pre-emphasis circuit (IC17), within +6 dB/octave pre-emphasis characteristics (300 Hz–3 kHz), to a level needed for the modulation circuit.

The filtered signal is applied to the mixer amplifier, and is then mixed with the "DI" signal from IC19. The mixed signal is applied to the limiter amplifier (TX unit; IC5, pin 3).

2-2-2 MODULATION CIRCUIT (TX UNIT)

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone AF signals.

The "MOD" signal from pin 7, J1 is applied to the limiter-amplifier (IC5, pin 3) via the pin 1, J5. The limiter-amplified signal passes through the modulating controller (Q13) and low-pass filter (IC5). The filtered signal is adjusted the input level by the R50, and is then applied to the VCO circuit (D2, D3, Q2).

2-2-3 YGR-AMPLIFIER CIRCUIT (TX UNIT)

The YGR-amplifier circuit includes the buffer-amplifier (Q4), pre-driver (Q5) and YGR-amplifier (Q6). The buffer-amplified signal from the VCO circuit is amplified at the YGR-amplifier circuit. The YGR-amplified signal is applied to the power amplifier (PA unit; IC1, pin 1).

The "APCV" signal from the APC control circuit (PA unit) is applied to the YGR-amplifier (Q6) to stable RF output power.

2-2-4 RF POWER AMPLIFIER CIRCUIT (PA UNIT)

IC1 is a power module which provides a stable 45 W of output power.

The amplified signal from the TX unit passes through the low-pass filter (C16, C17, L6), and is then applied to power -amplifier (IC1, pin 1). The power-amplified signal is applied to the RF detector circuit (D1, D2) to control APC circuit, and passes through the low-pass filter (L1–L4, C1, C2, C5, C6, C9, C10). Then, the filtered signal is applied to the TX antenna connector.

2-2-5 APC CIRCUIT (PA UNIT)

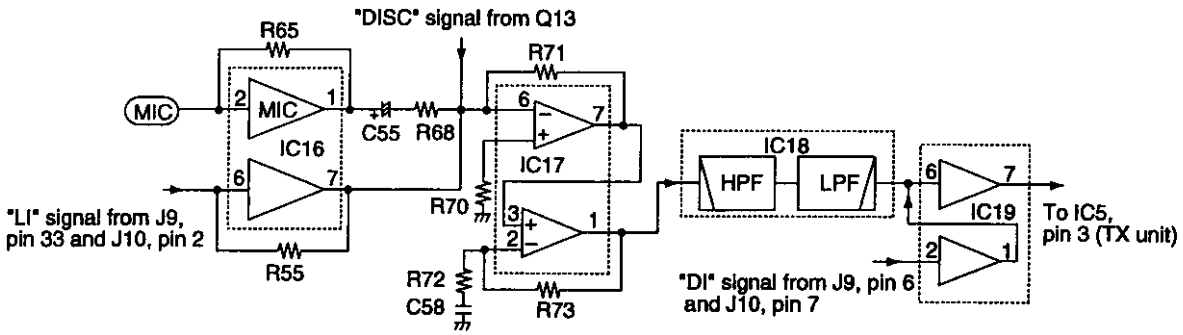
APC circuit controls a current of the power module's first stage and a current of the driver amplifier to obtain stable RF output power.

The APC mismatch detector circuit consists of C3, C7, D1, D2, L3. When the antenna impedance is matched at 50 Ω, the detected voltage by D1 and D2 is at its minimum. The detected voltage is applied to a differential amplifier (IC3, pin 3). The APC reference voltage is applied to pin 1,of IC3.

When the antenna impedanceis mismatched, the voltage of IC3 (pin 3) exceeds the reference voltage of IC3 (pin 1). The output level from IC3 (pin 4) decreases. Q1 amplifies the current from the differential amplifier (IC3) which controls Q2. Q2 changes the supply voltage to IC1.

This decreases the output power from the power amplifier (IC1) until the input voltage of IC3 (pin 6) reaches the same level as pin 5 of IC2.

• MICROPHONE AMPLIFIER CIRCUITS



2-3 PLL CIRCUITS

2-3-1 GENERAL

Each receiver and transmitter circuit has an independent PLL circuit for controlling frequencies. All PLL circuits are shielded and installed on the RX and TX Units.

PLL circuits steadily oscillate the transmit frequency and the receive local frequency. The PLL output frequency is controlled by the divided ratio (N-data) of the program mable divider.

2-3-2 RECEIVER PLL CIRCUIT (RX UNIT)

The PLL IC (IC3) which includes the prescaler, the programmable counter and the phase comparator generates the 1st LO frequency with a Colpitts VCO (D10, D11, Q4). The PLL IC sets the dividing ratio based on N-data from the CPU (LOGIC unit; IC1) to control the programmable counter. The PLL IC compares the phases of a VCO signal with the reference oscillator frequency, and is then applied to VCO circuit (D10, D11, Q4) via the charge pump circuit (D14, Q10, Q11).

2-3-3 RECEIVER REFERENCE OSCILLATOR CIRCUIT (RX UNIT)

A 12.8 MHz reference frequency is produced by the oscillator (X3). The frequency is adjusted with R84. The reference frequency is applied to the PLL IC (IC3, pin 1).

2-3-4 RECEIVER VCO CIRCUIT (RX UNIT)

The VCO circuit (D10, D11, Q4) generates the receive frequency. D10, D11, L14 and L15 provide oscillate frequency control. The controlled signal is applied to the buffer-amplifier (Q5) to amplify the VCO oscillation. The buffer-amplified signal is applied to PLL IC (IC3, pin 8) and the buffer-amplifier (Q6). The buffer-amplified signal is applied to the mixer circuit (IC6, pin 3).

2-3-5 TRANSMITTER PLL CIRCUIT (TX UNIT)

The PLL IC (IC3) which includes the prescaler, the programmable counter and the phase comparator generates the 1st LO frequency with a Colpitts VCO (D2, D3, Q2). The PLL IC sets the dividing ratio based on N-data from the CPU (LOGIC unit; IC1) to control the programmable counter. The PLL IC compares the phases of a VCO signal with the reference oscillator frequency, and is then applied to VCO circuit (D2, D3, Q2) via the charge pump circuit (D6, Q10, Q11).

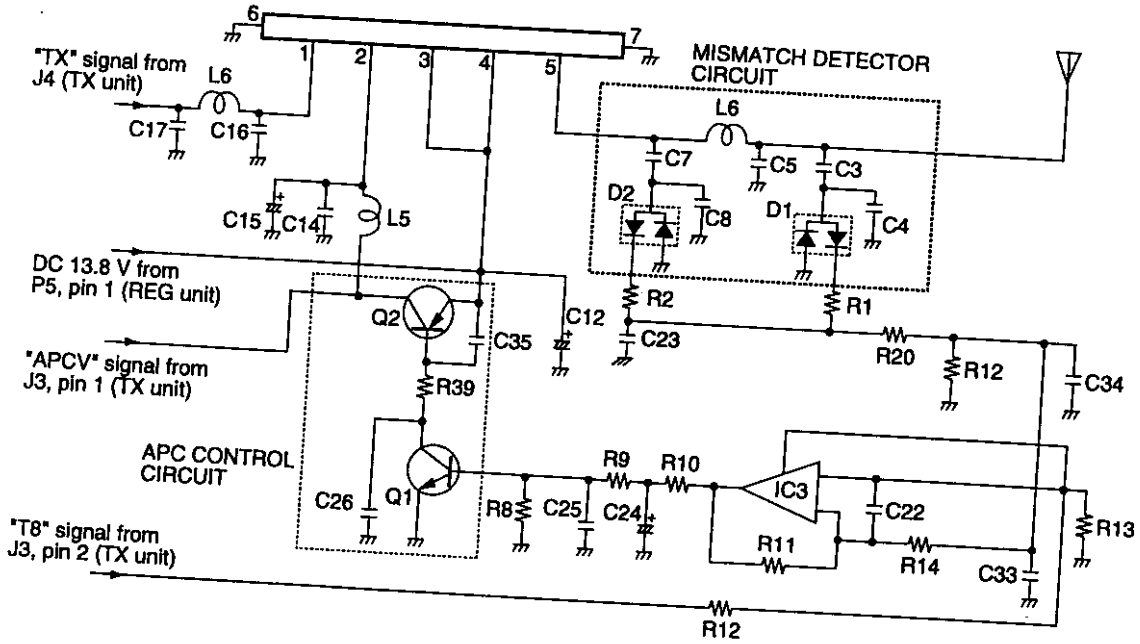
2-3-6 TRANSMITTER REFERENCE OSCILLATOR CIRCUIT (TX UNIT)

A 12.8 MHz reference frequency is produced by the oscillator (X1). The frequency is adjusted with R38. The reference frequency is applied to the PLL IC (IC3, pin 1).

2-3-7 TRANSMITTER VCO CIRCUIT (TX UNIT)

The VCO circuit (D2, D3, Q2) generates the transmit frequency. D2, D3, L1 and L2 provide oscillate frequency control. The controlled signal is applied to the buffer-amplifier (Q3) to amplify the VCO oscillation. The buffer-amplified signal is applied to PLL IC (IC3, pin 8) and the YGR-amplifier circuit (Q4, Q5, Q6).

• APC CIRCUIT



2-4 POWER SUPPLY CIRCUIT

2-4-1 VOLTAGE LINES

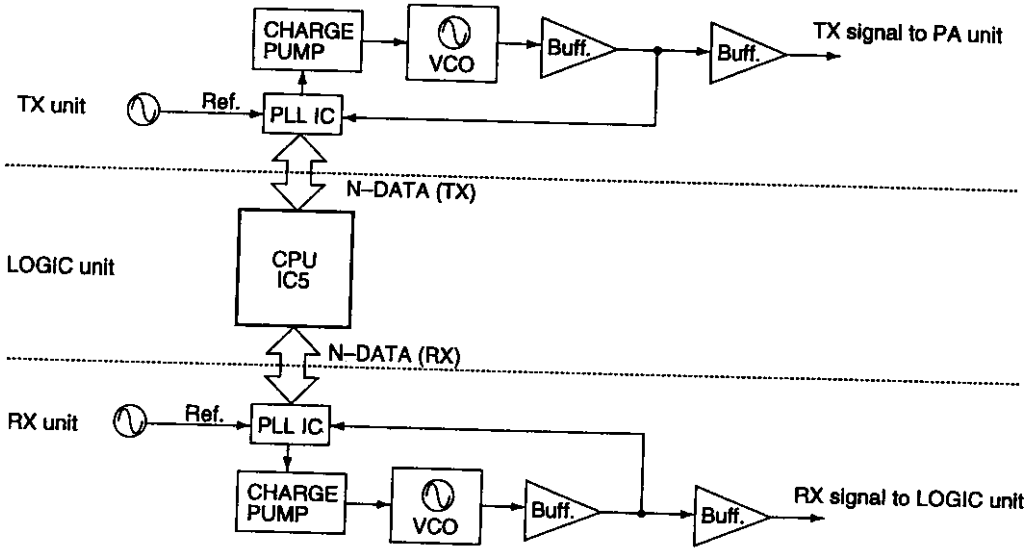
LINE	DESCRIPTION
13.8 V	The voltage from the connected DC power supply. The output voltage is applied to the CPU (LOGIC unit; IC1, pin 45) via the V.DET circuit (LOGIC unit; IC21, pin 3 and 5).
S13.8 V	The same voltage as the 13.8 V line which is controlled by the power switch (FRONT unit; S1). The output voltage is applied to the AF amplifier (LOGIC unit; IC15, pin 5) via the "V13" line.
+ 9 V	Common 9 V converted from the DC power supply by the + 9 V regulator circuit (REG unit; IC1). The output voltage is applied to TX switch, + 5 V regulator, ripple filter on TX unit and + 5 V regulator, ripple filter on RX unit.
+ 5 V	Common 5 V converted from the + 9 V regulator circuit (REG unit; IC1) by the + 5 V regulator circuit (LOGIC unit; IC9). The output voltage is applied to RESET circuit (LOGIC unit).

2-5 PORT ALLOCATIONS

2-5-1 CPU (LOGIC UNIT IC1)

Pin number	Port name	Description
3	P62 / A18	Outputs LOCAL INHIBIT LED control signal .
4	P61 / A17	Outputs COR SIMURATE LED control singal.
5	P60 / A16	Outputs RESET LED control signal.
29	P21 / INTP0	Input port for the transmitting mode from the outside signal.
30	P22 / INTP1	Input port for the STB signal to switch the outside frequency.
31	P23 / INTP2 / C1	Input port for the LOCAL mode from the outside signal.
32	P24 / INTP3	Input port for the RESET signal from the outside signal.
45	P74 / AN4	Input port for the VD, H signal from the DC power supply voltage detecting circuit.
46	P73 / AN3	Input port for the VD, L signal from the DC power supply voltage detecting circuit.
47	P72 / AN2	Input port for the TX unlock signal.
48	P71 / AN1	Input port for the RX unlock signal.
49	P70 / AN0	Input port for the squelch signal.
54	P00	Outputs clock signal to TX and RX PLL IC.
55	P01	Outputs data signal to TX and RX PLL IC.
56	P02	Outputs LE signal to TX PLL IC.
57	P03	Outputs LE signal to RX PLL IC.
58	P04	Outputs control signal for transmitting.

• **PLL CIRCUITS**



SECTION 3 ADJUSTMENT PROCEDURES

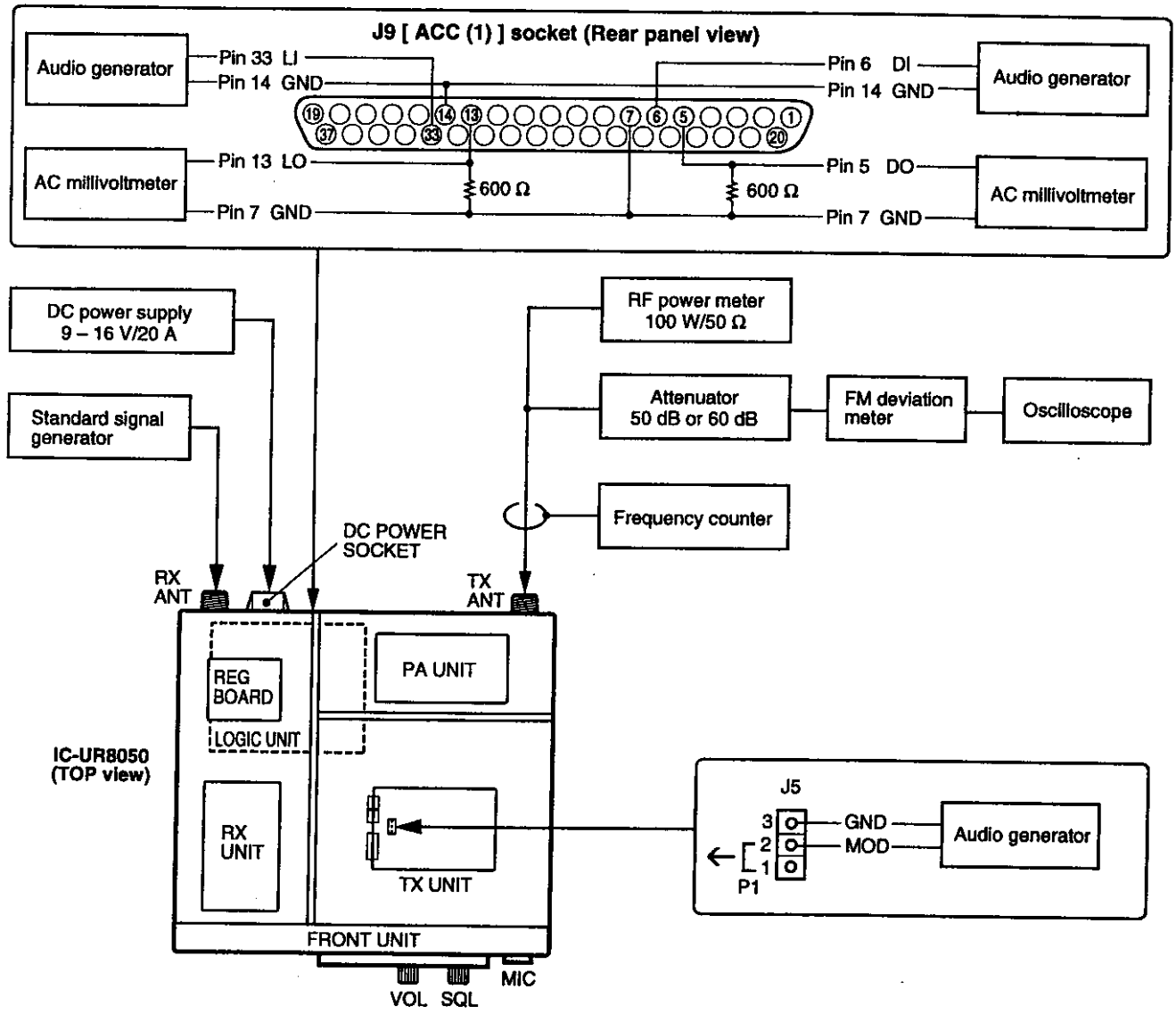
3-1 PREPARATION

■ REQUIRED TEST EQUIPMENT

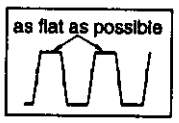
EQUIPMENT	GRADE AND RANGE	EQUIPMENT	GRADE AND RANGE
DC power supply	Output voltage : 9–16 V DC Current capacity : 20 A or more	Standard signal generator (SSG)	Frequency range : 300–600 MHz Output level : 0.1 µV–32 mV (–127 to –17 dBm)
RF power meter (terminated type)	Measuring range : 1–100 W Frequency range : 300–600 MHz Impedance : 50 Ω SWR : Less than 1.2 : 1	Oscilloscope	Frequency range : DC–20 MHz Measuring range : 0.01–20 V
Frequency counter	Frequency range : 0.1–600 MHz Frequency accuracy : ±1 ppm or better Sensitivity : 100 mV or better	DC voltmeter	Input impedance : 50 kΩ/V DC or better
FM deviation meter	Frequency range : 30–600 MHz Measuring range : 0 to 10 kHz	AC millivoltmeter	Measuring range : 10 mV–10 V
Audio generator (AG)	Frequency range : 300–3000 Hz Measuring range : 1–500 mV	Digital multimeter	Input impedance : 10 MΩ/V DC or better
		Attenuator	Power attenuation : 50 or 60 dB Capacity : 100 W or more
		Terminator	Impedance : 50 Ω Capacity : 100 W or more
			Impedance : 600 Ω dummy

CW: Clockwise CCW: Counterclockwise

■ CONNECTION

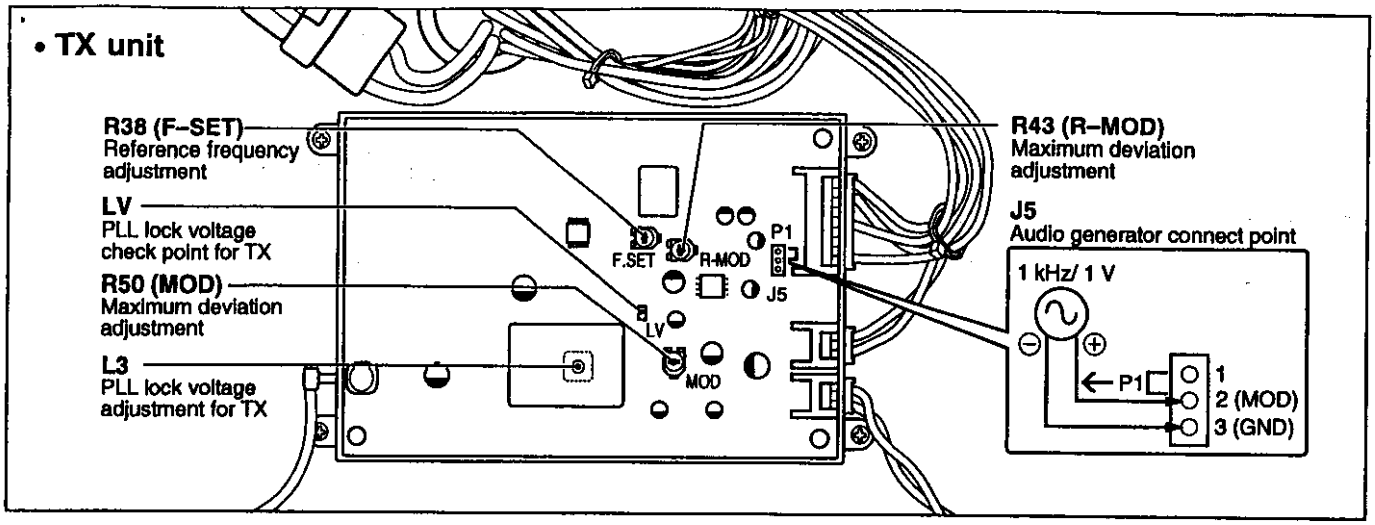


3-2 PLL AND TRANSMITTER ADJUSTMENTS

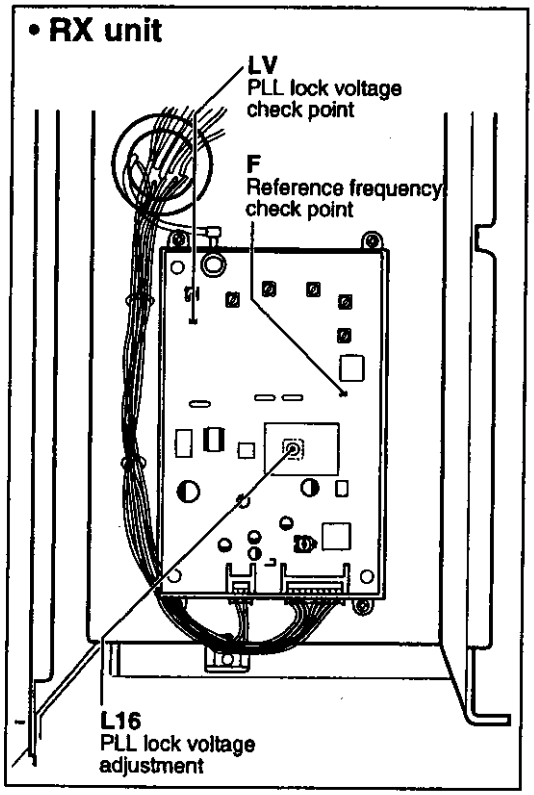
ADJUSTMENT		ADJUSTMENT CONDITIONS	MEASUREMENT		VALUE	ADJUSTMENT	
			UNIT	LOCATION		UNIT	ADJUST
PLL LOCK VOLTAGE	1	• Operating freq. : 415.000 MHz • Apply DC voltage : 13.8 V [VOLUME] : Max. CCW [SQUELCH] : Max. CW • Connect an RF power meter or terminator to the [TX ANT] connector. • Transmitting	TX	Connect a digital multimeter or an oscilloscope to check point [LV].	2.7 V	TX	L3
	2	• [LOCAL INHIBIT] switch : ON • Receiving freq. : 415.050 MHz [VOLUME] : "11 o'clock" position • Receiving	RX	Connect a digital multimeter or an oscilloscope to check point [LV].	2.4 V	RX	L16
REFERENCE FREQUENCY	1	• Operating freq. :415.000 MHz • Transmitting	Rear panel	Loosely couple a frequency counter to the [TX ANT] connector.	415.0000 MHz	TX	R38 (F–SET)
OUTPUT POWER	1	• [LOCAL INHIBIT] switch : ON • Operating freq. : 415.000 MHz • Apply DC voltage : 13.8 V [VOLUME] : Max. CCW [SQUELCH] : Max. CW • Transmitting	Rear panel	Connect an RF power meter or a terminator to the [TX ANT] connector.	47 W	PA	R16 (Hi)
DEVIATION (MAXIMUM)	1	• [LOCAL INHIBIT] switch : ON • Set an FM deviation meter as : HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P–P)/2 • Disconnect P1 from J5 on the TX unit, connect an audio generator to J5 and set as : 1 kHz/ 1 V • Transmitting	Rear panel	Connect an FM deviation meter to the [TX ANT] connector through an attenuator.	± 4.7 kHz [Wide] ± 2.3 kHz [Narrow]	TX	R50 (MOD)
	2	• Set an AG as : 50 Hz/ 1 V • Transmitting			Minimum deviation, and a connected oscilloscope to the FM deviation meter as shown below. 		R43 (R–MOD)
	3	After adjustment, connect P1 to J5 on the TX unit.					
(MICROPHONE)	4	• Connect an AG to [MIC] connector and set as : 1 kHz/ 4 mV • Transmitting	Rear panel	Connect an FM deviation meter to the [TX ANT] connector through an attenuator.	± 3.0 kHz [Wide] ± 1.5 kHz [Narrow]	LOGIC	R61 (MIC)
(REPEATER)	5	• [LOCAL INHIBIT] switch : OFF • Connect an SSG to the [RX ANT] connector and set as: Level : 1 mV* (60 dBμ) Deviation : ± 3 kHz Modulation : 1 kHz • Receiving					R47 (MOD)
	6	•Set an SSG as Deviation : ± 5.0 kHz [Wide] : ± 2.5 kHz [Narrow] • Receiving			± 3.0–5.0 kHz [Wide] ± 1.5–2.5 kHz [Narrow]		Verify

*This output level of the standard signal generator (SSG) is indicated as the SSG's open circuit.

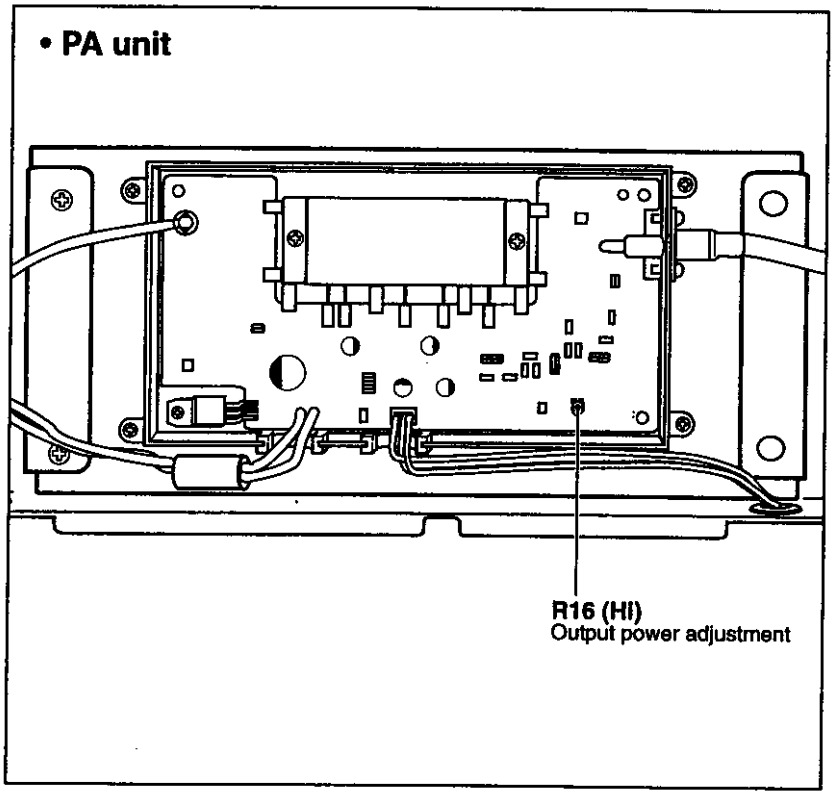
• TX unit



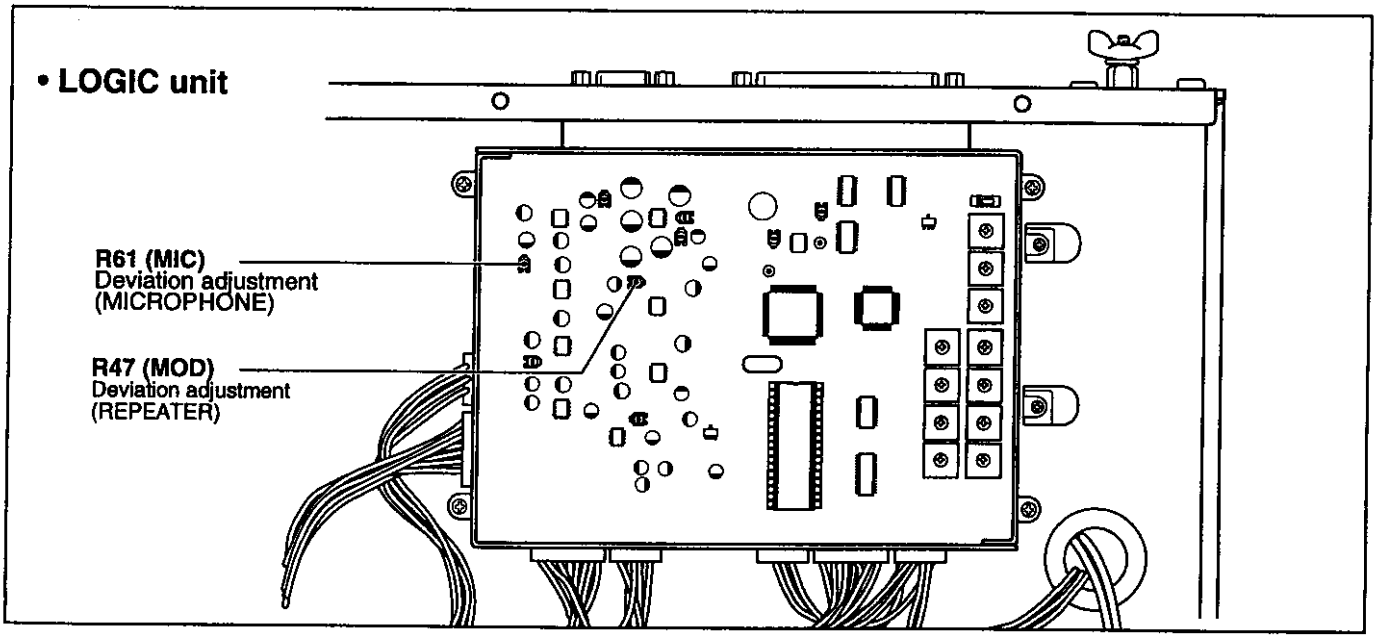
• RX unit



• PA unit



• LOGIC unit

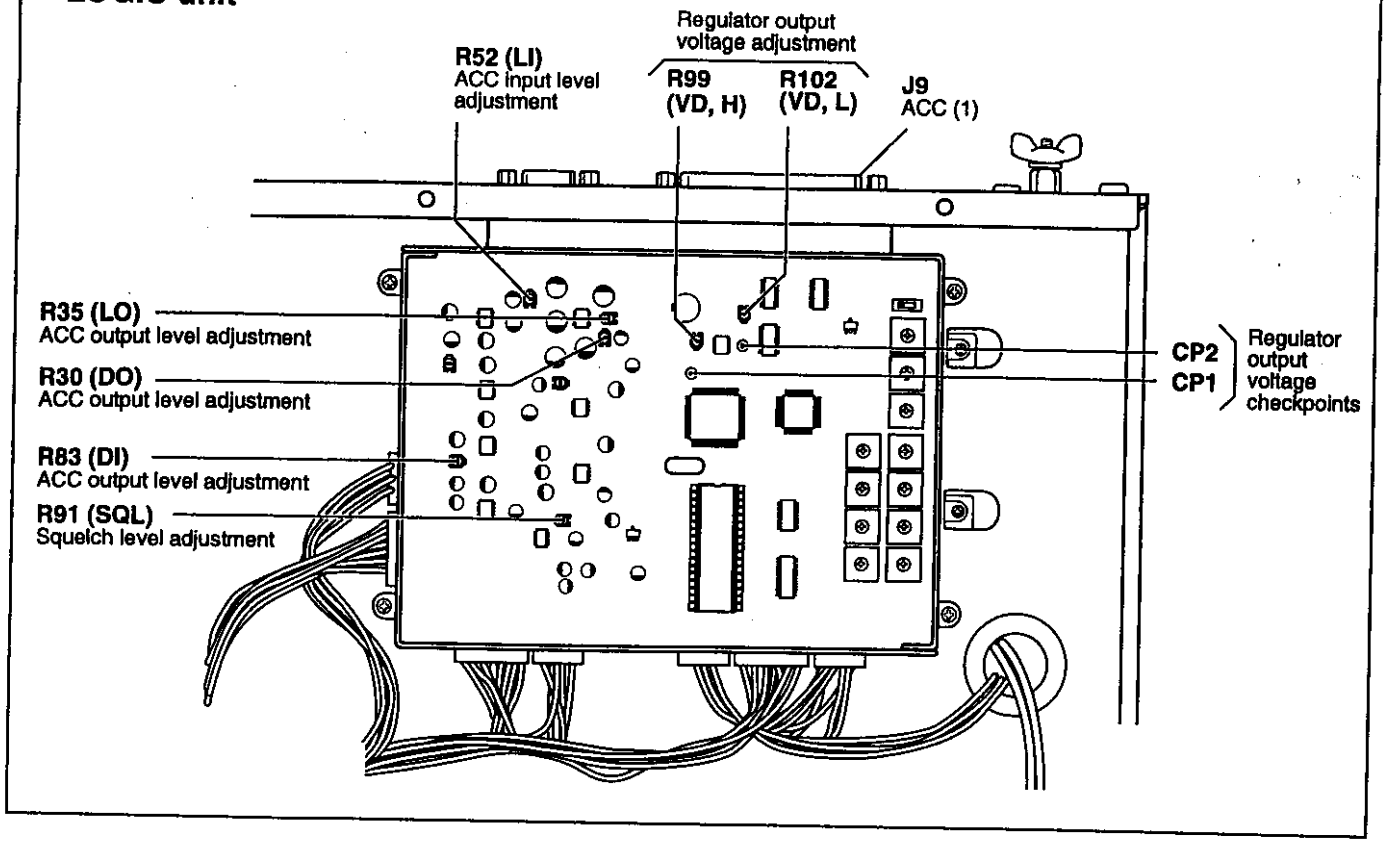


3-3 ACC LEVELS, REGULATOR OUTPUT AND RECEIVER ADJUSTMENTS

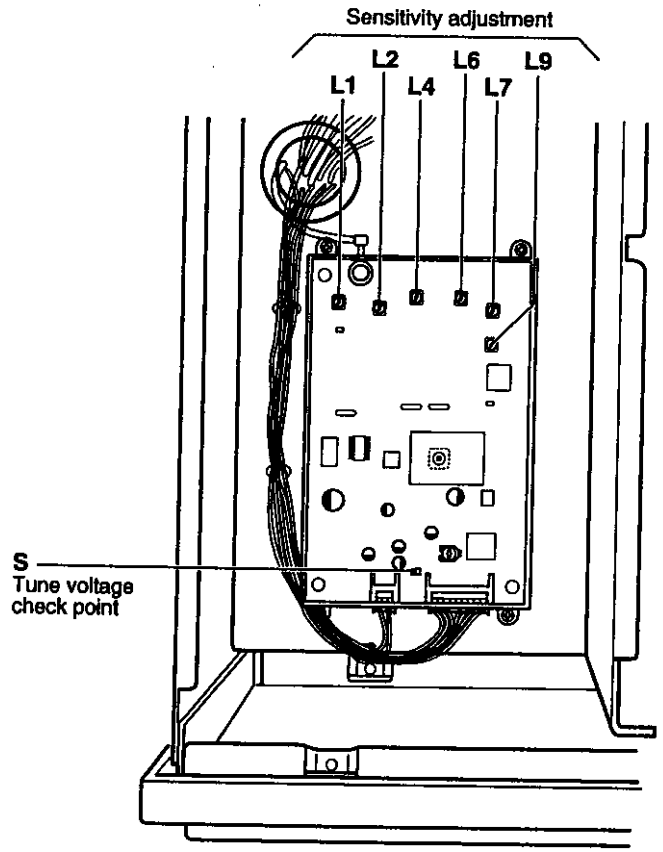
ADJUSTMENT		ADJUSTMENT CONDITIONS	MEASUREMENT		VALUE	ADJUSTMENT	
			UNIT	LOCATION		UNIT	ADJUST
ACC OUPUT LEVEL (DO)	1	• [LOCAL INHIBIT] switch : ON • Connect an SSG to the [RX ANT] connector and set as : Level : 1 mV* (–60 dBμ) Deviation : ±3.0 kHz [Wide] ±1.5 kHz[Narrow] Modulation : 1 kHz • Receiving	Rear panel	Connect a millivoltmeter and 600 Ω terminator in parallel to [ACC1] socket (J9 pin 5, 7).	0 dBm	LOGIC	R30 (DO)
ACC OUPUT LEVEL (LO)	2			(J9 pin 13, 7)	0 dBm		R35 (LO)
ACC INPUT LEVEL (LI)	1	• [LOCAL INHIBIT] switch : ON • Set an FM deviation meter as: HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P–P)/2 • Connect an AG to [ACC1] socket (J9 pin 33, 14) and set as : 1 kHz/ 100 mV • Transmitting	Rear panel	Connect an FM deviation meter to the [TX ANT] connector through an attenuator.	± 3.0 kHz [Wide] ± 1.5 kHz [Narrow]	LOGIC	R52 (LI)
ACC INPUT LEVEL (DI)	2	• Connect an AG to [ACC1] socket (J9 pin 6, 14) and set as Level : 1 kHz/100 mV • Transmitting			±3 kHz		R83 (DI)
REGULATOR OUTPUT VOLTAGE	1	• Connect an RF power meter or a terminator to the [TX ANT] connector. • R99, R102 (LOGIC unit) : Max. CCW • Apply DC voltage : 11 V	LOGIC	Connect a digital multimeter to check point CP1.	At the point where the voltage just switches H (5 V) to L (0 V).	LOGIC	R99 (VD, H)
	2	• Apply DC voltage : 10 V		Connect a digital multimeter to check point CP2.			R102 (VD, L)
	3	• Decrease applied DC voltage 13.8 V to 9 V. • Transmitting	Rear	Connect a DC voltmeter between the + and – terminals at DC power socket.	Turns off [TX] LED at 10 V. (stop transmitting)	Front	Verify
	4	• Increase applied DC voltage 9 V to 13.8 V. • Transmitting			Turns on [TX] LED at 11 V. (start transmitting)		
SENSITIVITY	1	• [LOCAL INHIBIT] switch : ON • Receiving freq. : 415.000 MHz • Connect an SSG to the [RX ANT] connector and set as : Level : 3.2 μV* (–97 dBm) Deviation : ±3.0 kHz [Wide] : ±1.5 kHz [Narrow] Modulation : 1 kHz • Receiving	RX	Connect a digital multimeter to check point CP.S.	Maximum voltage	RX	Adjust in sequence L1, L2, L4, L6, L7, L9
SQUELCH LEVEL	1	• [LOCAL INHIBIT] switch : ON • Receiving freq : 415.000 MHz • Connect an SSG to the [RX ANT] connector and set as : Level : 0.32 μV* (–10 dBμ) Modulation : OFF • Receiving	FRONT	[BUSY] LED	At the point where the [BUSY] LED just turns on.	FRONT	[SQUELCH] control
	2	• [LOCAL INHIBIT] switch : OFF • R91 (LOGIC unit) : Max. CW • Set an SSG as: Level : 0.22 μV* (–13 dBμ) • Receiving		Speaker output	At the point where the audio signal just appears.	LOGIC	R91 (SQL)

*This output level of the standard signal generator (SSG) is indicated as the SSG's open circuit.

• LOGIC unit

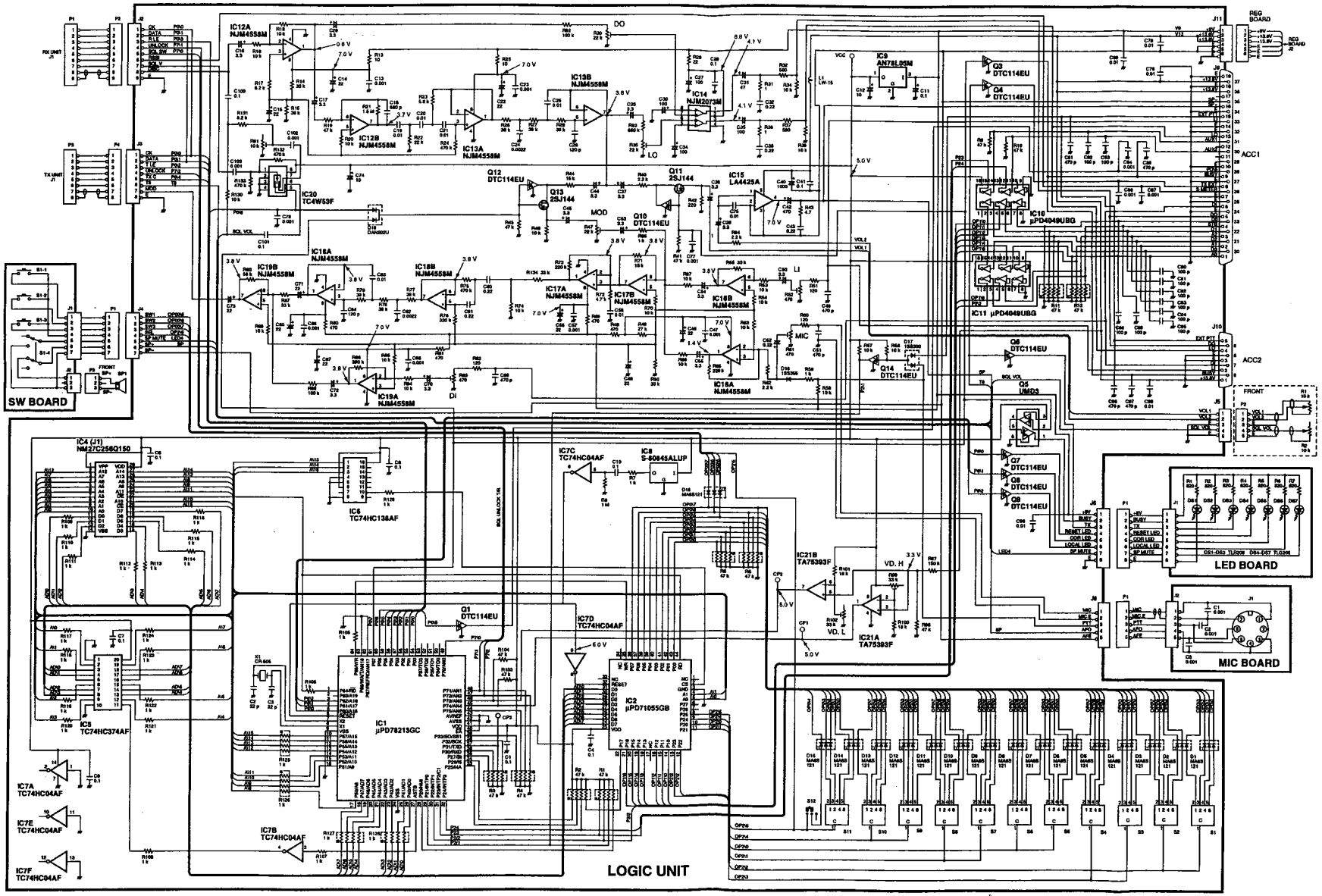


• RX unit

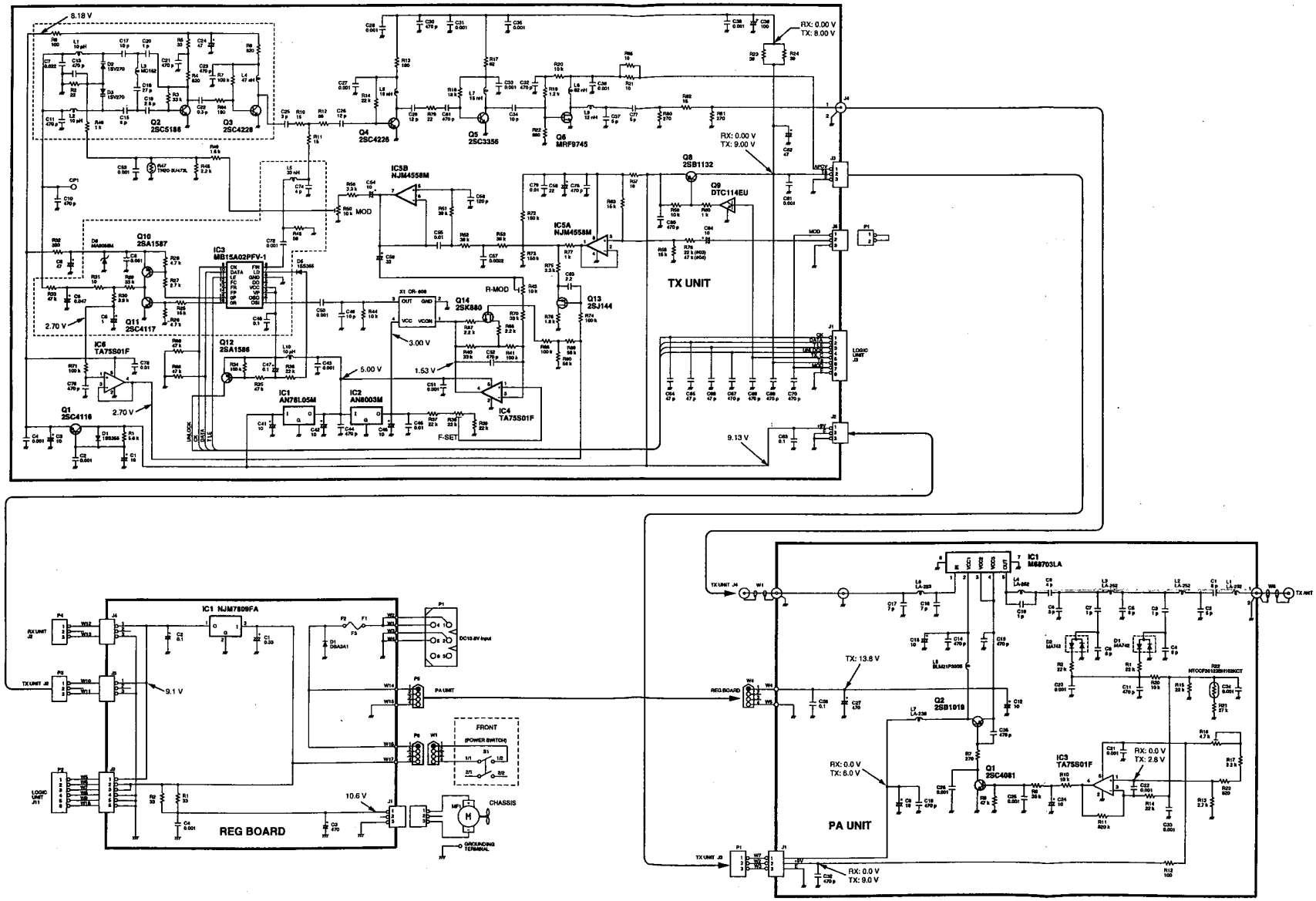


SECTION 6 VOLTAGE DIAGRAM

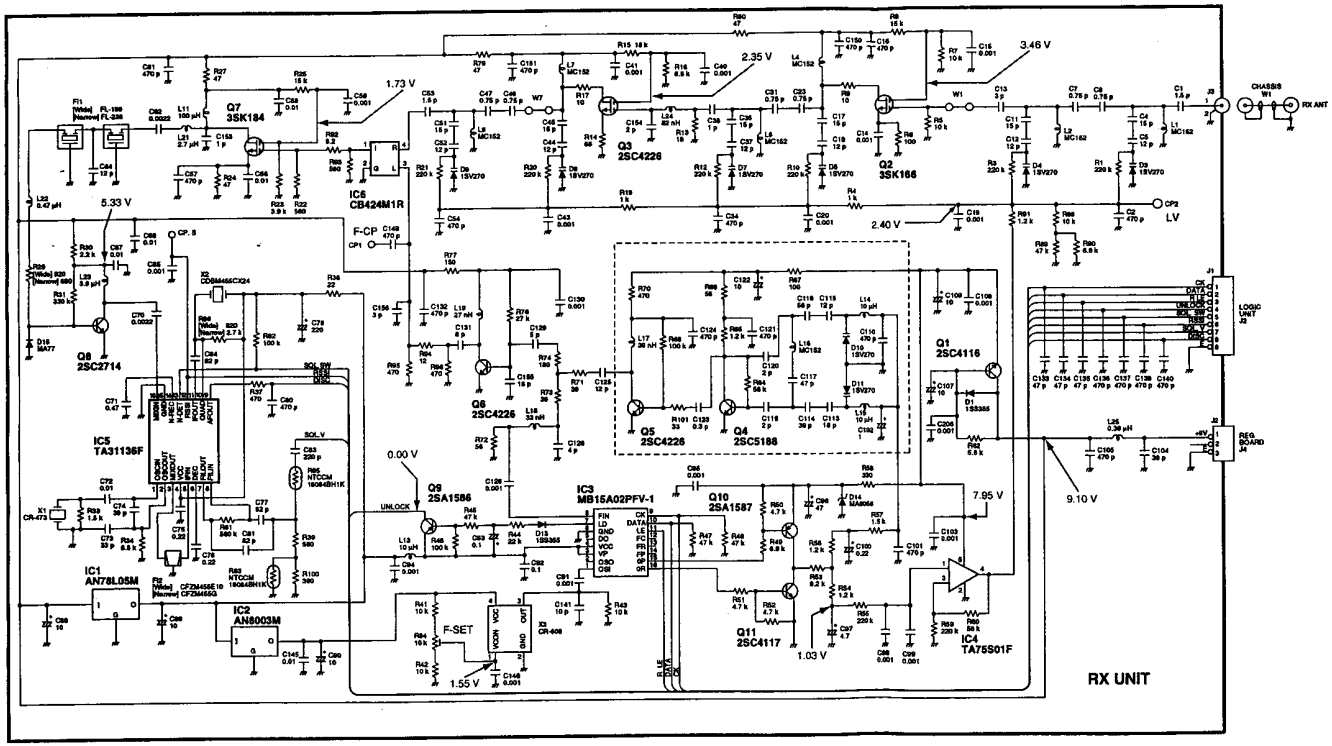
• **LOGIC UNIT**



• TX, PA AND REG UNIT



• RX UNIT


RX UNIT
IC1 AN78L05M
IC2 AN6003M
IC3 MB15A02PFV-1
IC4 TA75S01F
IC5 TA31136F
IC6 CB424M1R
Q1 2SC4116
Q2 3SK166
Q3 2SC4226
Q4 2SC5188
Q5 2SC4226
Q6 2SC4226
Q7 3SK184
Q8 2SC2714
Q9 2SA1586
Q10 2SA1587
Q11 2SC4117
5.33 V
1.73 V
2.35 V
3.46 V
2.40 V
0.00 V
7.95 V
9.10 V
1.03 V
1.55 V
F-SET
F-CP
LV
RX ANT
LOGIC UNIT
REG BOARD