SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 DUPLEXER CIRCUIT (RF UNIT)

The transceiver has a duplexer (low-pass and high-pass filters) on the frist stage from the antenna connector to separate the signals into below UHF and SHF signals. The high-pass filter (L51–L55, C41–C46 and C48–C50) is for SHF (1200 MHz) signal and the low-pass filter (C9, C10, C12–C14 and L7–L9) is for below UHF (50 MHz, 144 MHz, 440 MHz and WFM) signals. The filtered SHF signal is applied to the low-pass fileter (C51–C54, L56 and L57).

The RF signals below UHF pass through the duplexer circuit and are separated into VHF (50 MHz, 144 MHz and WFM band) and UHF (440 MHz band) signals. The high-pass filter (C4–C8, L5, L6) is for UHF (440 MHz band) signal and the low-pass filter (C15–C20, L10–L12) is for VHF (50 MHz, 144 MHz and WFM band) signals.

The VHF signals are applied to the another duplexer circuit for separation into 50 MHz and above WFM band signals. The high-pass filter (C21–C24, C84 and L13–L15) is for 144 MHz and WFM band signals and the low-pass filter (C27–C33 and L16–L18) is for 50 MHz band signal.

The separated signals are applied to each RF circuits.

4-1-2 ANTENNA SWITCHING CIRCUITS (RF UNIT)

The antenna switching circuit functions as a low-pass filter while receiving. However, its impeadance becomes very high while transmitting by applying a current to D101 and D102 (50 MHz), D302 and D303 (144MHz and WFM), D402 and D403 (440 MHz), D51 and D52 (1200 MHz).

Thus, transmit signals are blocked from entering the receiver circuits. The antenna switching circuit employs a 1/4λ type diode switching system. The passed signals are then applied to each RF amplifier circuit.

4-1-3 50 MHz BAND RF CIRCUIT (RF UNIT)

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit (D101 and D102) are amplified at the RF amplifier (Q101). The amplified signals pass through the tunable bandpass filter (L108–L110, C115, C117, C120, D106, D107) to suppress out-of-band signals, and are then applied to the 1st mixer circuit (IC601, pin 1).

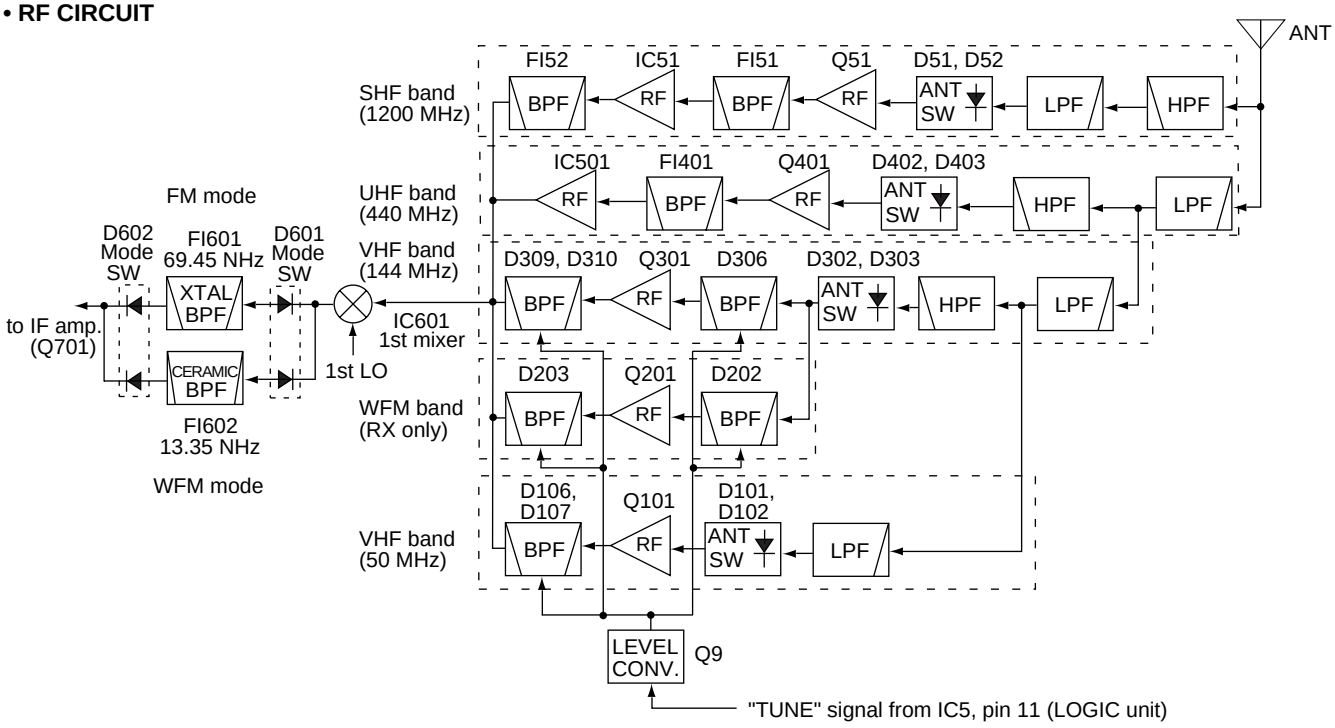
4-1-4 144 MHz AND WFM BANDS RF CIRCUITS (RF UNIT)

The signal from the antenna switching circuit (D302, D303) are applied to the each band-pass fileters and RF amplifier.

• RF signals 144 MHz band

The 144 MHz band signals are applied to the RF amplifier (Q301) via the tunable bandpass filter (L303, L304, C306, D306). The amplified signals pass through the tunable bandpass filter (C318–C321, D309, D310, L305, L306), and are then applied to the 1st mixer circuit (IC601, pin 1).

• RF CIRCUIT



• RF signals WFM band

The WFM band signals are applied to the RF amplifier (Q201) via the tunable band-pass filter (D202). The amplified signals pass through the tunable bandpass filter (D203), and are then applied to the 1st mixer circuit (IC601, pin 1).

Varactor diodes (D106, D107, D202, D203, D306, D309, D310) are employed by the tunable bandpass filter to tune the center frequency of the bandpass filter. These diodes are controlled by the PLL lock voltage and obtain good image response rejection.

4-1-5 440 MHz BAND RF CIRCUIT (RF UNIT)

The signals from the antenna switching circuit (D402 and D403) are amplified at the RF amplifier (Q401). The amplified signals pass through the bandpass filter (FI401), and are then applied to the 1st mixer circuit (IC601, pin 1) after being amplified at another RF amplifier (IC501).

4-1-6 1200 MHz BAND RF CIRCUIT (RF UNIT)

The signals from the antenna switching circuit (D51 and D52) are amplified at the RF amplifier (Q51). The amplified signals pass through the bandpass filter (FI51), and are then applied to the RF amplifier (IC51). The amplified signal is applied to the 1st mixer circuit (IC601, pin 1) via the bandpass filter (FI52).

4-1-7 1ST MIXER CIRCUIT (RF UNIT)

The 1st mixer circuit converts the received RF signals into a fixed frequency of the 1st IF signal with a 1st LO output frequency. By changing the PLL frequency, only the desired frequency will pass through at the next stage of the 1st mixer. 1st mixer circuit produces the different 1st IF signal for WFM and other band signals.

• 50, 144, 440 and 1200 MHz band

The applied RF signals are mixed with 1st LO signals at the 1st mixer (IC601) to produce a 69.45 MHz 1st IF signal. The 1st IF signal is output from the 1st mixer (IC601, pin 6), and then passed through the crystal bandpass filter (FI601) to suppress unwanted harmonic components. The filtered 1st IF signal is applied to the IF amplifier (IC701). The amplified signal is applied to the 2nd mixer circuit (LOGIC unit; IC701, pin 16).

• WFM band

The RF signals are mixed with 1st LO signals at the 1st mixer (IC601) to produce a 13.35 MHz 1st IF signal. The 1st IF signal is output from the 1st mixer (IC601, pin 6), and then passed through the 1st IF filter (FI602) to suppress unwanted harmonic components. The filtered signal is applied to the 2nd mixer circuit (LOGIC unit; IC701, pin 16).

The 1st LO signals are gererated at the VCO circuit which consists of Q301, Q302, D301, Q311, Q312, D302, D311 for 50 MHz, 144 MHz and WFM, Q321, Q322, D321, D322 for 440 MHz, Q350, D351, D352 for 1200 MHz on the VCO unit.

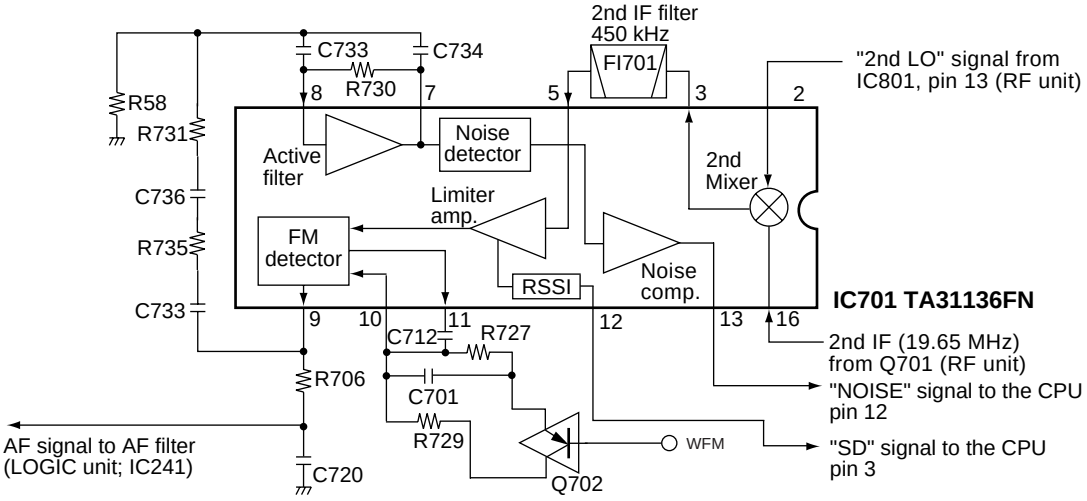
• The 1st LO signal for 50, 144, 440, WFM band

The 1st LO signals which are generated on the VCO unit are applied to the buffer-amplifier (Q313 and D312 for 50 MHz, 144 MHz and WFM, Q323 for 440 MHz). The buffer-amplified signals are applied to the LO-amplifier (Q822 for 50 MHz, 144 MHz and WFM, Q823 for 440 MHz), and are then applied to the 1st mixer circuit via the TX/RX switch (D802 and D803 for 50 MHz, 144 MHz and WFM, D804 and D805 for 440 MHz) on the RF unit.

• The 1st LO signal for 1200 MHz band

The 1st LO signals which are generated on the VCO unit are applied to the buffer-amplifier (Q351). The buffer-amplified signals are applied to the doubler circuit (Q353), and passes through the high-pass and low-pass filter. The filtered signals are applied to the 1st mixer circuit (Q601) on the LOGIC unit after being amplified at the LO-amplifier (Q824).

• 2nd IF AND DEMODULATOR CIRCUITS (LOGIC unit)



4-1-8 2ND IF AND DEMODULATOR CIRCUITS (RF AND LOGIC UNITS)

The 2nd mixer circuit converts the 1st IF signal to the 2nd IF signal. A double conversion superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtain stable receiver gain.

The FM IF IC (LOGIC unit; IC701) contains 2nd local oscillator, 2nd mixer, limiter amplifier, quadrature detector and S-meter detector circuits.

The filtered 1st IF signal from the 1st IF filter (RF unit; FI601 or FI602) is mixed with the 2nd LO signal at the 2nd mixer (LOGIC unit; IC701) to produce the 450 kHz 2nd IF signal. The 2nd IF signal passes through or bypasses (WFM mode signal) 2nd IF filter (FI701) where unwanted heterodyne signals are suppressed via the mode switch (LOGIC unit; D701, D702). The filtered signals are applied to the limiter amplifier section (LOGIC unit; IC701, pin 5), and then applied to the quadrature detector section to demodulate the 2nd IF signal into AF signals.

The demodulated AF signals are output from pin 9 of the IF IC (LOGIC unit; IC701) and are applied to the AF circuit.

4-1-9 AF AMPLIFIER CIRCUIT (LOGIC UNIT)

The AF amplifier circuit which is included a low-pass and high-pass filter, AF mute switch, AF volume controller and AF amplifier amplifies the demodulated AF signals to drive a speaker.

The demodulated AF signals (DETO signal) from the FM IF IC (IC701) are passed through the AF filter (low-pass and high-pass filters). The filtered signals are applied to the AF mute switch (Q361) which is controlled by “RM/MM” signals from the CPU (IC1, pin 31), and are then applied to the electric volume control circuit (IC202, IC203). The level controlled AF signals are output from volume IC (IC202, pin 7) and are then applied to the AF amplifier (IC201, pin 4). The AF signals are then applied to the internal speaker (SP1) via the [EXT SP] jack (LOGIC unit; J3) when no plug is connected to the jack.

The AF filter circuit (IC241) removes AF signals below 300 Hz (CTCSS signals) for clear AF output and these are applied to the CPU (IC1, pin4) for CTCSS squelch detection via the “CTCIN” line.

4-1-10 SQUELCH CIRCUIT (LOGIC UNIT)

• NOISE SQUELCH

The noise squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

A portion of the AF signals from the FM IF IC (IC701, pin 9) are applied to the active filter section (IC701, pin 7, 8). The active filter section amplifies and filters noise components. The filtered signals are applied to the noise detector section and output from IC701 (pin 13) as “NOISE” signal.

The “NOISE” signal from IC701 (pin 13) is applied to the CPU (IC1, pin 12). The CPU analyzes the noise condition and outputs the “RM/MM” signal to AF mute switch (Q361).

Even when the squelch is closed, the AF mute switch (Q361) opens at the moment of emitting beep tones.

• TONE SQUELCH

The tone squelch circuit detects AF signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the AF signals from the FM IF IC (IC701, pin9) passes through the AF filter (IC241) to remove AF (voice) signals and is applied to the CTCSS decoder inside the CPU (IC1, pin 4) via the “CTCIN” line to control the AF mute switch.

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHON AMPLIFIER CIRCUIIT (LOGIC UNIT)

The microphone amplifier circuit amplifies the audio signals from the microphone, within +6 dB/octave pre-emphasis characteristics (300 Hz–3 kHz), to a level needed for the modulation circuit.

The AF signals from the internal microphone (MC1) or external [MIC] jack (J4) are applied to the microphone (limiter) amplifier (IC301, pin 3) which has +6 dB/octave pre-emphasis characteristics, and are then passed through the low-pass filter (IC301, pin 6 and 7). The filetered signals are applied to the modulation circuit for each band in the RF unit via the band switch (Q304: for 144 MHz band, Q305: for UHF band, Q306: for 50 MHz band, Q309: for 120MHz band) as the “MOD” signal.

4-2-2 MODULATION CIRCUIT (VCO AND RF UNIT)

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone AF signals.

(1) 50 MHz band

The signals from the limiter amplifier (RF unit; IC301) changes the reactance of a diode (RF unit; D341) to modulate the oscillated signal at the 50-VCO circuit (RF unit; Q341, D341, L341–343). The modulated signals are amplified at the buffer-amplifier (Q342) and the LO amplifier (Q821). The amplified signals are applied to the drive/power amplifier circuits for VHF band.

(2) 144 MHz band

The signals from the limiter amplifier (RF unit; IC301) changes the reactance of a diode (VCO unit; D302) to modulate the oscillated signal at the 144-VCO circuit (VCO unit; Q311, Q312, D302, D311–D313). The modulated signals are amplified at the buffer-amplifier (Q312, Q313) and the LO amplifier (Q822). The amplified signals are applied to the drive/power amplifier circuits for VHF band.

(3) 440 MHz band

The signals from the limiter amplifier (RF unit; IC301) changes the reactance of a diode (VCO unit; D321) to modulate the oscillated signal at the 440-VCO circuit (VCO unit; Q321, Q322, D321, D322, L322). The modulated signals are amplified at the buffer-amplifier (Q323) and the LO amplifier (Q823). The amplified signals are applied to the drive/power amplifier circuits for UHF band.

(4) 1200 MHz band

The signals from the limiter amplifier (RF unit: IC301) changes the reactance of a diode (VCO unit; D352) to modulate the oscillated signal at the 1200-VCO circuit (VCO unit; Q350, D351, D352, L330). The modulated signals are amplified at the buffer-ampifier (Q351). The amplified signals are applied to the doubler circuit (Q353), and then passed through the high-pass (C376–C380, L334, L335) and the low-pass (C381–C386, L336, L337) filters. The filtered signals are amplified at the buffer-amplifier (Q354) and the LO amplifier (Q824). The amplified signals are applied to the drive/power amplifier circuits for SHF band.

4-2-3 DRIVE/POWER AMPLIFIER CIRCUITS (RF UNIT)

The amplifier circuit amplifies the VCO oscillating signal to the output power level.

(1) 50 MHz PA

The signal from the LO amplifiers (Q821) is amplified at the buffer-amplifier (Q133) and the YGR amplifier (Q134). The amplified signal is applied to the driver amplifiers (Q921), and is then amplified at the power amplifier (Q922) to obtain 5.0 W of RF power.

The amplified signal is passed through the antenna switching circuit (D101 and D102) and low-pass filters, and is then applied to the antenna connector.

(2) 144 MHz PA

The signal from the LO amplifiers (Q822) is passed through the Tx/Rx switch (D802 and D803), and is amplified at the buffer-amplifier (Q133) and the YGR amplifier (Q134). The amplified signal is applied to the driver amplifiers (Q921), and is then amplified at the power amplifier (Q922) to obtain 5.0 W of RF power.

The amplified signal is passed through the antenna switching circuit (D101 and D102), low-pass filters and high-pass filters. The signal is applied to the antenna connector.

(3) 440 MHz PA

The signal from the LO amplifiers (Q823) is passed through the Tx/Rx switch (D804 and D805), and is amplified at the buffer amplifier (Q135) and the YGR amplifier (Q136). The amplified signal is applied to the driver amplifier (Q921), and is then amplified at the power amplifier (Q922) to obtain 5.0 W of RF power.

The amplified signal is passed through the antenna switching circuit (D402 and D403), low-pass filters and high-pass filters. The low-pass filtered signal is applied to the antenna connector.

(4) 1200 MHz PA

The signal from the LO amplifiers (Q824) is passed through the Tx/Rx switch (D806 and D807), and is amplified at the buffer-amplifiers (Q131 and Q132) and the YGR amplifier (Q138). The amplified signal is applied to the driver amplifiers (Q921) to obtain 1.0 W of RF power.

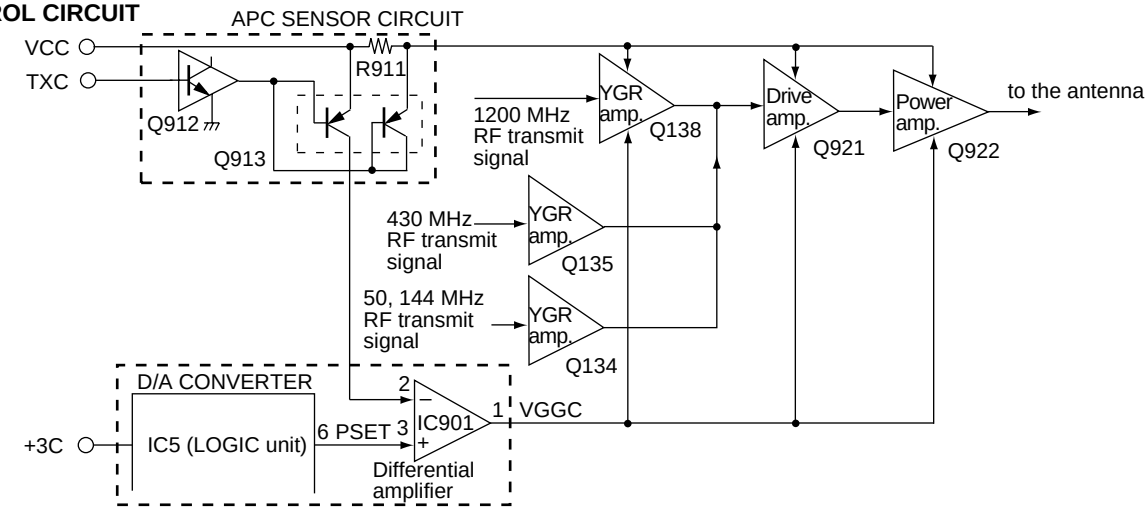
The amplified signal is passed through the antenna switching circuit (D51 and D52), low-pass filter and high-pass filters. The high-pass filtered signal is applied to the antenna connector.

Collector voltages for the drive amplifier (Q921) and control voltage for the power amplifier (Q922) and YGR amplifier (Q138) are controlled by the APC circuit to protect the power module from a mismatched condition as well as to stabilize the output power.

4-2-4 APC CIRCUITS (RF UNIT)

The APC circuit protects the power amplifier from a mismatched output load and stabilizes the output power. The APC circuit is designed to use VHF, UHF and SHF bands commonly.

• APC CONTROL CIRCUIT



The APC sensor (R911) detects driving current from the drive voltage at the YGR (Q138), drive (Q921) and power (Q922) amplifiers. The detected current is converted into DC voltage at Q913, then applied to the APC control circuit (IC901, pin 2). The applied voltage is compared with a "PSET" voltage from the CPU via the D/A converter (LOGIC unit; IC5), and the APC control circuit outputs "VGGC" voltage from pin 1 to control the YGR, drive and power amplifiers.

When the driving current is increased, input voltage of the differential amplifier (IC901, pin 2) will be increased. In such cases, the differential amplifier output voltage (IC901, pin 1) is decreased to reduce the driving current.

4-3 PLL CIRCUITS

4-3-1 50 MHz BAND PLL CIRCUIT (RF UNIT)

The osillated signal at the 6MVCO (Q341, D341) is amplified at the buffer amplifiers (Q342, Q343). The amplified signal is applied to the PLL IC (IC801, pin 2) via the buffer-amplifier (Q813).

The signal which is applied to the PLL IC (IC801) is divided by N-data from the CPU and phase-detected with the divided reference frequency (5 kHz) then output from pin 8. The output signal is converted into DC voltage at the active filter (Q804, Q805) and is fed back to the 6MVCO as the lock voltage.

4-3-2 144 MHz BAND PLL CIRCUIT (VCO BOARD AND RF UNIT)

The osillated signal at the 144-VCO circuit (VCO unit; Q311, Q312, D302 and D311) is amplified at the buffer amplifiers (VCO unit; Q313).The amplified signal is applied to the PLL IC (IC801, pin 19) via a buffer-amplifier (Q807).

The applied signal is divided by serial data from the CPU (N-data) and phase-detected with the divided reference frequency (5 kHz) at the phase detector section in the PLL IC. The phase-detected signal is output from IC801 (pin 13) and converted DC voltage at the active filter (Q811, Q812). The converted DC voltage is fed back to the VCO board as the "VLV" signal of the lock voltage.

While operating in the 144 MHz band, the lock voltage is applied to the CPU (LOGIC unit; IC1) via the tune control circuit (Q803) to track the center frequency of the tunable bandpass filters (D306, D309, D310) as the "TUNE" signal.

4-3-3 440 MHz BAND PLL CIRCUIT (VCO BOARD AND RF UNIT)

The osillated signal at the 440-VCO circuit (VCO unit; Q321, Q322, D321 and Q322) is amplified at the buffer-amplifiers (VCO unit; Q323).The amplified signal is applied to the PLL IC (IC801, pin 19) via a buffer-amplifier (Q807).

The applied signal is divided by serial data from the CPU (N-data) and phase-detected with the divided reference frequency (5 kHz) at the phase detector section in the PLL IC. The phase-detected signal is output from IC801 (pin 13) and converted DC voltage at the active filter (Q811, Q812). The converted DC voltage is fed back to the VCO board as the "VLV" signal of the lock voltage.

4-3-4 1200MHz BAND PLL CIRCUIT (VCO BOARD AND RF UNIT)

The osillated signal at the 1200-VCO circuit (VCO unit; Q350, D351 and D352) is amplified at the buffer-amplifiers (VCO unit; Q351 and Q353). The signal passes through the buffer amplifier (Q354), the high-pass (C376–C380, L334 and L335) and the low-pass filter (C381–C385, L336 and L337). The filtered signal is applied to the PLL IC (IC802, pin 1) via the buffer amplifier (Q816).

The applied signal is divided by serial data from the CPU (N-data) and phase-detected with the divided reference frequency (5 kHz) at the phase detector section in the PLL IC. The phase-detected signal is output from IC801 (pin 13) and converted DC voltage at the active filter (Q811, Q812). The converted DC voltage is fed back to the VCO board as the "VLV" signal of the lock voltage.

4-4 POWER SUPPLY CIRCUITS

VOLTAGE LINE

LINE	DESCRIPTION
HV	The voltage from the external power supply or attached battery pack.
VCC	The same voltage as the "HV" line (external power supply or battery pack) passed through a diode (RF unit; D1).
+3CPU	Common 3V converted from the "VCC" line by +3C CPU regulator IC (LOGIC unit; IC141). The output voltage is supplied to the +3C regulator circuits, etc.
+3C	Common 3V converted from the "VCC" line by the +3C regulator circuit (LOGIC unit; Q142 and Q145) using the +3CPU regulator (LOGIC unit; IC141.)
+3	Common 3V converted from the "VCC" line by the +3 regulator circuit (LOGIC unit; IC5, Q1, Q2 and Q3) using the +3C regulator (LOGIC unit; Q142 and Q145).
R+3	3V for receiver circuit converted from the "VCC" line by the "R+3" regulator circuit (RF unit; Q7 and Q8).
T4	4V for transmitter circuit converted from the "VCC" line by the T4 regulator circuit (RF unit; Q901–Q903 and D901). The T4 regulator circuit is controlled by the CPU (LOGIC unit; IC1, pin 21) via the "TXC" line.

4-5 PORT ALLOCATIONS

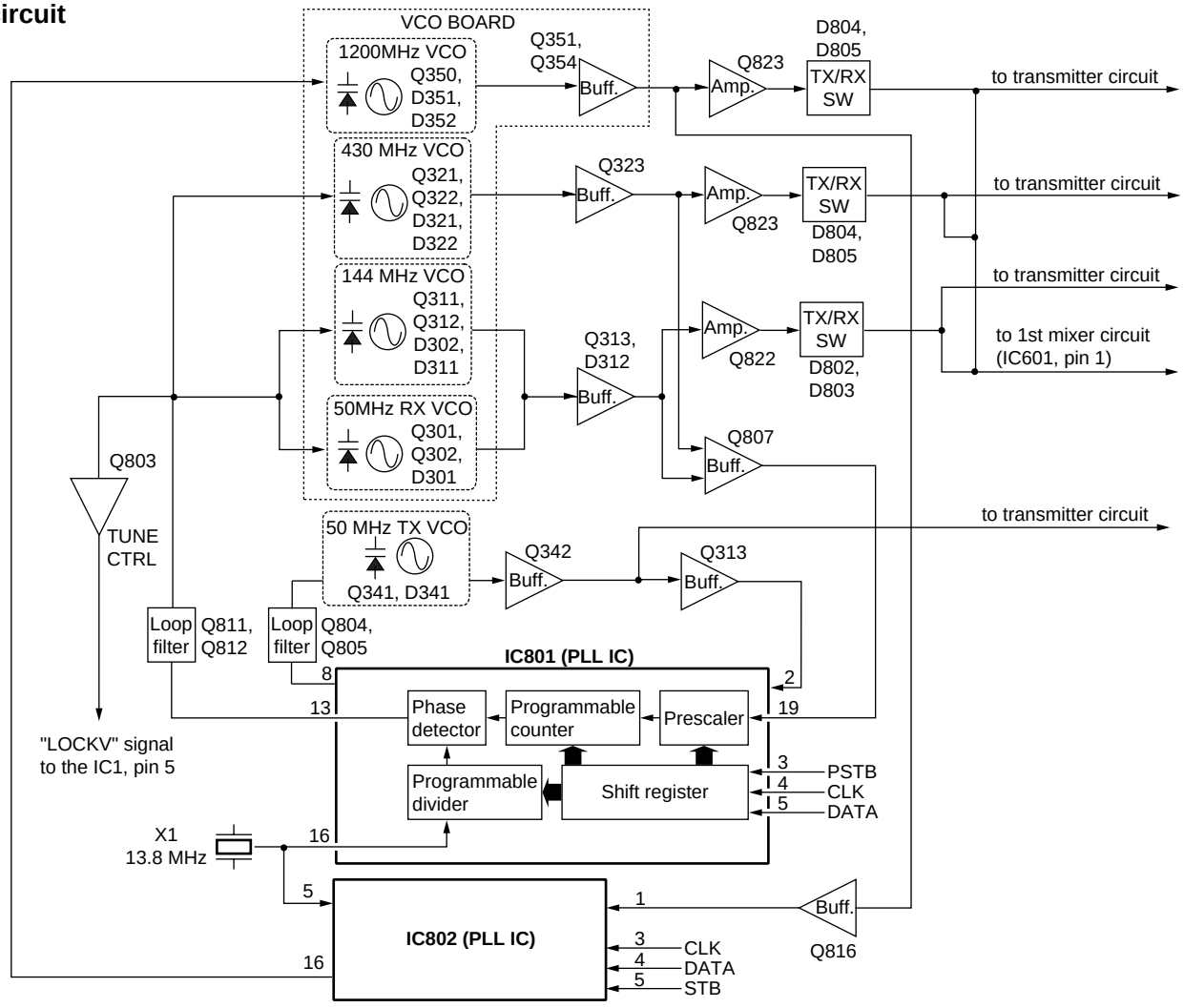
4-5-1 I/O EXPANDER IC (RF UNIT; IC2)

Pin number	Port name	Description
4	Q1	Outputs VHVCO3 regulator control signal.
5	Q2	Outputs VLVCO3 regulator control signal.
6	Q3	Outputs 6MVCO3 regulator control signal.
7	Q4	Outputs VCO shift signal for SHF, UHF, 144 MHz and 50 MHz.
11	Q8	Outputs 12VCO3 regulator control signal.
12	Q7	Outputs UHVCO3 regulator control signal.
13	Q6	Outputs UHF TX and RX regulator control signal.
14	Q5	Outputs 1200 MHz TX and RX regulator control signal.

4-5-2 I/O EXPANDER IC (RF UNIT; IC3)

Pin number	Port name	Description
4	Q1	Outputs 300 MHz band RX regulator control signal.
6	Q3	Outputs AM mode regulator control signal.
7	Q4	Outputs WFM band RX switching control signal.
11	Q8	Outputs WFM band RX regulator control signal.
12	Q5	Outputs 50 MHz band TX and RX regulator control signal.
13	Q6	Outputs VHF band TX and RX regulator control signal.

• PLL circuit



4-5-3 CPU (LOGIC UNIT; IC1)

Pin number	Port name	Description
1	VIN	Input port for the over-voltage detection from connected battery pack or external power supply.
2	REMOTE	Input port for remote control signals from an optional HM-75A microphone via the [MIC] jack.
3	SD	Input port for the S-meter voltage.
4	CTCIN	Input port for CTCSS decoded signals.
5	LOCKV	Input port for the PLL lock voltage.
6	THERMC	Input port for the tranceiver's internal temparature.
7	SBATT	Input port for the VCC voltage (connected battery voltage).
8	CONT	Outputs control signal for the LCD contrast. High : The LCD contrast is deep.
9	CTCOUT	Outputs CTCSS signals while transmitting.
10	BEEP	Output port for: • Beep audio signals while receiving. • DTMF signals or 1750 Hz Europe tone signal while transmitting. [EUR], [ITA], [UK]
11	BPCPI	Input port for the bias control voltage to judge kinds of battery types. High : Supply the bias control voltage.
12	NOISE	Input port for the noise signal (pulse-type) from the IF IC (RF unit; IC 701, pin 13).
13	PDA2/UL	Outputs data signals to the PLL IC2 (RF unit; IC802, pin 4). Input port for the PLL unlock signal from the PLL IC2 (RF unit; IC802, pin 4).
14	PDA1/UL	Outputs data signals to the PLL IC1 (RF unit; IC801, pin 5). Input port for the PLL unlock signal from the PLL IC1 (RF unit; IC801, pin 5).
15	DAST	Outputs strobe signals to the D/A IC (LOGIC unit; IC5, pin2).
16	IOST	Outputs strobe signals to the I/O IC (RF unit; IC2, pin 1 and IC3, pin 1).
17	PLST2	Outputs strobe signals to the PLL IC2 (RF unit, IC802, pin5).
18	PLST1	Outputs strobe signals to the PLL IC1 (RF unit, IC801, pin 3).
19	CLONEOUT	Output port for the cloning signal.
20	CLONEIN	Input port for the cloning signal.
21	TXC	Outputs T4 regulator control signal. High : While transmitting.
22	R3C	Outputs R3 regulator control signal. High : While receiving.
23	CPUHV	Input port for the reset signal from Q151 (LOGIC unit).
24	CHGC	Outputs control signal for charger circuit (RF unit; Q5). High : While battery is charging.
25	AFON	Outputs control signal for the AF amplifier requlator circuit. High : Activates the AF amplifier circuit.
26	PCON	Outputs +3C regulator control signal (LOGIC unit; Q142 and Q145).
27	TCON	Outputs control signal for the Europe tone and DTMF. Low : Activates the Europe tone. High : Activates DTMF.
28	BLED	Outputs BUSY LED control singal. Low : The BUSY LED is ON.
29	LIGHT	Outputs LCD backlight control signal. High : Lights ON.
30	MICC	Outputs control signal for the regulator secton of MIC amplifier (LOGIC unit; IC301). Low : Activates the MIC amplifier circuit.
31	RM/MM	Outputs AF mute and MIC mute control signals. High : Mute is ON.
32	POWER	Input port for the [POWER] switch.
33	RESET	Input port for the RESET signal from IC142, pin 1 (LOGIC unit).
39	PTT	Input port for the [PTT] switch.
41	CK	Outputs clock signal to the PLL IC1 (IC801), PLL IC2 (IC802), D/A IC (IC5) , I/O IC (IC2, IC3) on the RF unit and EEPROM IC (LOGIC unit; IC2).
42	ESIO	Data bus line for the EEPROM (LOGIC unit; IC2).
43–46	KR3–KR0	Input ports for key matrix.
47, 48	I1, I2	Input ports for Initial matrix.
49–54	KS5–KS0	Outputs port for key matrix.
55, 56	DICK, DIUK	Input port for the up/down signal from the main dial (LOGIC unit; S1).