SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 DUPLEXER CIRCUIT (1F UNIT)

The transceiver has a duplexer (low-pass and high-pass filters) on the first stage from the antenna connector to separate the signals into VHF and UHF signals. The low-pass filter (L10–L12, C16–C22) for VHF signals and high-pass filter (L1–L3, C1–C5) for UHF signals. The separated signals are applied to each RF circuit.

4-1-2 VHF ANTENNA SWITCHING CIRCUIT (1F UNIT)

The antenna switching circuit functions as a low-pass filter while receiving. However, Its impedance becomes very high while transmitting by applying a current to D51 and D52. Thus, transmit signals are blocked from entering the receiver circuits. The antenna switching circuit employs a 1/4 λ type diode switching system. The passed signals are then applied to the RF amplifier circuit on the 2F unit.

4-1-3 VHF RF CIRCUIT (2F UNIT)

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit are applied to the limitter (D55), and are then passed through the band-pass filter (D52, L53). The filtered signal is applied to the RF amplifiers (Q51, Q52). The amplifier consists of a cascade circuit. The amplified signals are passed through the next stage band-pass filter (D53, D54, L54, L55) to suppress unwanted signals. The filtered signals are then applied to the mixer circuit (Q401).

D53 and D54 track the band-pass filters and are controlled by the PLL lock voltage. These diodes tune the center frequency to obtain good image response rejection.

4-1-4 UHF RF CIRCUIT (2F UNIT)

The signals from the antenna switching circuit (1F unit; D551, D552, D722–D724 and Q204) are applied to the limitter (D201), and are then amplified at the the RF amplifier (Q201). The amplified signals are passed through the band-pass filter (FI201), and are then applied to another RF amplifier (Q202). The amplified signals are applied to the 1st mixer circuit (Q401).

Common circuits with VHF band are used later stage from the 1st mixer.

4-1-5 1ST MIXER AND 1ST IF CIRCUITS (2F UNIT)

The mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with a 1st LO (VCO output) frequency. By changing the PLL frequency, only the desired frequency will be passed through a crystal filter at the next stage of the mixer.

The received signals from the VHF or UHF RF circuit are mixed with the 1st LO signal (VCO output signal) at the 1st mixer (Q401) to produce a 45.15 MHz 1st IF signal.

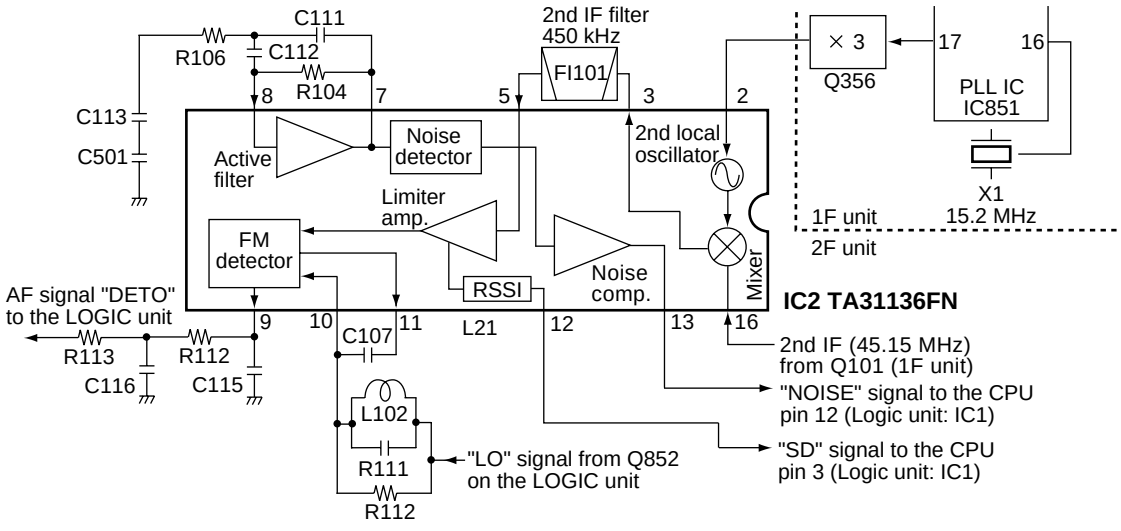
The 1st IF signal is applied to a crystal filter (FI401) to suppress out-of-band signals. The filtered 1st IF signal is amplified at the IF amplifier (Q101) and is then applied to the 2nd mixer circuit (IC101, pin 16).

4-1-6 2ND IF AND DEMODULATOR CIRCUITS (2F UNIT)

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

The FM IF IC (IC101) contains the 2nd mixer, 2nd local oscillator, limiter amplifier, S-meter detector and quadrature detector circuits.

• 2nd IF AND DEMODULATOR CIRCUITS



The 1st IF signal (45.15 MHz) from the IF amplifier (Q101) is applied to the 2nd mixer section of IC101 (pin 16), and is mixed with the 2nd LO signal (45.6 MHZ) for conversion to a 450 kHz 2nd IF signal at the 2nd mixer section.

The 2nd IF signal (450 kHz) from the 2nd mixer section (IC101, pin 3) passes through the ceramic filter (FI101) where unwanted signals are suppressed. It is then amplified at the limiter amplifier section (IC101, pin 5) and applied to the quadrature detector section to demodulate the 2nd IF signal into AF signals.

AF signals output from IC101 (pin 9) are applied to the AF drive amplifier (Q12) on the LOGIC unit. The S-meter output "SD" signal from IC101 (pin 12) is applied to the CPU (LOGIC unit; IC1, pin 3).

4-1-7 AF AMPLIFIER CIRCUIT (LOGIC UNIT)

The AF amplifier circuit, including an AF mute switch, amplifies the demodulated signals to drive a speaker.

The demodulated AF signals ("DETO" signals) from the FM IF IC (IC101) on the 2F unit are applied to the drive amplifier (Q12, pin 3) via the band-pass filter (C44, C45). The band-pass filter suppresses subaudible tones and higher noise signal components.

The amplified signals from Q12 (pin 1) pass through the AF mute switch (Q10) and are then applied to the AF volume control on the 1F unit via the "AF" signal line.

4-1-8 AF POWER AMPLIFIER CIRCUIT (2F UNIT)

The AF signals from the AF volume control ("AFV" signals) are amplified at the AF power amplifier IC (IC151, pin4). The amplified AF signals are applied to the loud speaker via the external speaker jack (1F unit; J902).

4-1-9 NOISE SQUELCH UNIT (2F UNIT)

A noise squelch circuit cuts out AF signals when no RF signal is received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

Some of the noise components in the AF signals from the FM IF IC (IC101, pin 9) are applied to the active filter section (IC101, pins 7 and 8). The variable register (R504) adjusts the active filter input level.

The active filter section amplifies noise components with frequencies of 20 kHz and above. The filtered signals are rectified at the noise detector section and converted into "NOISE" (pulse type) signals at the noise comparator section. The "NOISE" signal is applied to the CPU (LOGIC unit; IC1, pin 12).

The CPU (LOGIC unit; IC1) detects the signal level from the number of the pulses, and outputs an "MM/RM" signal from IC1 pin 44 on LOGIC unit. This signal controls the AF mute switch (LOGIC unit; Q10) to cut the AF signal line.

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT (LOGIC AND 2F UNIT)

The microphone amplifier circuit amplifies audio signals with +6 dB/octave pre-emphasis from the microphone to a level needed for the modulation circuit.

The AF signals from the built-in condenser microphone (LOGIC unit; MC1), or from the [MIC] Jack (1F unit; J901) via the "EXT MIC" line are applied to the limiter amplifier (LOGIC unit; IC12, pin 3) which has +6 dB/octave pre-emphasis characteristics.
The amplified AF signals pass through the splatter filter (IC12, pins 5–7). The filtered signals are applied to frequency deviation pots (2F unit; R308 for VHF, R314 for UHF) and are then applied to the modulation circuit on the DUAL VCO board.

Q32 on the LOGIC unit is the PTT control circuit and outputs a "High" signal to the CPU when transmitting.

4-2-2 MODULATION CIRCUIT (DUAL VCO BOARD)

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals.

The "VMOD" signals change the reactance of a diode (D304) to modulate the oscillated signal at the VHF-VCO circuit (Q304, Q305 and D303).

The "UMOD" signals are applied to the UHF-VCO circuit via the "USHIFT" line. The applied signals change the reactance of a diode (D302) to modulate the oscillated signal at the UHF-VCO circuit (Q301, Q302 and D301).

The VCO output is buffer-amplified at Q306 and then applied to the band switch (D351 and D352) via the LO amplifiers (Q852 and Q351).

4-2-3 POWER AMPLIFIER CIRCUIT (1F UNIT)

Q401 is a drive and Q402 is a power amplifier. They are designed to use both VHF and UHF commonly. They provide more than 6 W for VHF and 6 W for UHF with a 13.5 V DC power source via one power amplifier system.

An RF signal from the band switch (D351 and D352) is buffer-amplified at Q201 (for VHF) or Q701 (for UHF) and then applied to the drive amplifier (PA board; Q401) via the other band switch (D201 and D701). The applied RF signal from the band switch is amplified at a drive amplifier (Q401) and then amplified again at the power amplifier (Q402).

The amplified RF signal is passed through the low-pass filter (VHF) or high-pass filter (UHF), and then applied to the antenna connector via the transmit/receive switching circuit (Q51, D52 and Q202 are for VHF, D551, D552, D722–D724 and Q204 are for UHF).

4-2-4 APC CIRCUIT (1F AND 2F UNITS)

The APC circuit stabilizes transmit output power and selects HIGH and LOW output power. The APC circuit consists of APC sensor, APC control (1F unit) and APC set (2F unit) circuits.

The APC sensor circuit (1F unit; R250) detects a driving current from a drive voltage at the PA board. The detected current is applied to the ope-amplifier IC (1F unit; IC250, pin 2) in the APC control circuit, and compared with a “PSET” voltage which is supplied from the APC set circuit (2F unit; IC301). The output voltage from pin 1 of IC250 is applied to the APC control circuit (1F unit; Q255 base) to control “VGGC” voltage.

The “VGGC” APC control signal is separated for VHF (VGG1) and UHF (VGG2) by resistors. The VGG1 line is for the APC control signal for the drive amplifier and the VGG2 line is for the power amplifier.

Low output power is obtained by changing the “PSET” voltage coming from pin 1 of IC301 on the 2F unit. The “PSET” voltage is controlled by power set pots (2F unit; R302 for VHF, 2F unit; R304 for UHF) and an “H/L” signal via the CPU (LOGIC unit; IC1, pin 56). A thermistor (R266) controls APC reference voltage (“PREF” voltage) to reduce the output power when the temperature is increased.

4-2-5 ANTENNA SWITCHING CIRCUIT (1F UNIT)

The antenna switching circuit applies receive signals to the receiver circuit and transmit signals to the antenna connector.

(1) VHF ANTENNA SWITCHING CIRCUIT

When transmitting, D51 D52 and D202 are turned ON. The signal passes through the low-pass filter (L10–L12, C16–C22) and is then applied to the antenna connector. The low-pass filter suppresses high harmonic components.

(2) UHF ANTENNA SWITCHING CIRCUIT

When transmitting, D722-D724, D551, D552 and Q204 are turned ON. The signal passes through the low-pass (L7–L9, C9–C15) and high-pass (L1–L3, C1–C5) filters and is then applied to the antenna connector. The high-pass filter suppresses low harmonic components.

4-3 PLL CIRCUITS

4-3-1 VHF PLL CIRCUIT (1F UNIT)

The oscillated signal at the VCO circuit (DUAL VCO board; Q304, Q305 and D303) is amplified at a buffer-amplifier (Q306) and is again amplified at another buffer-amplifier (Q352). The amplified signal is applied to the PLL IC (IC851, pin 2), and then divided by serial data from the CPU and phase-detected with the divided reference frequency. The phase difference is output as pulses.

The output signals from IC851 (pin 8) are converted to DC voltages (lock voltage) by the loop filter (R366–R368, C362, and C364) and are then fed back to the VHF VCO circuit to stabilize the VCO frequency.

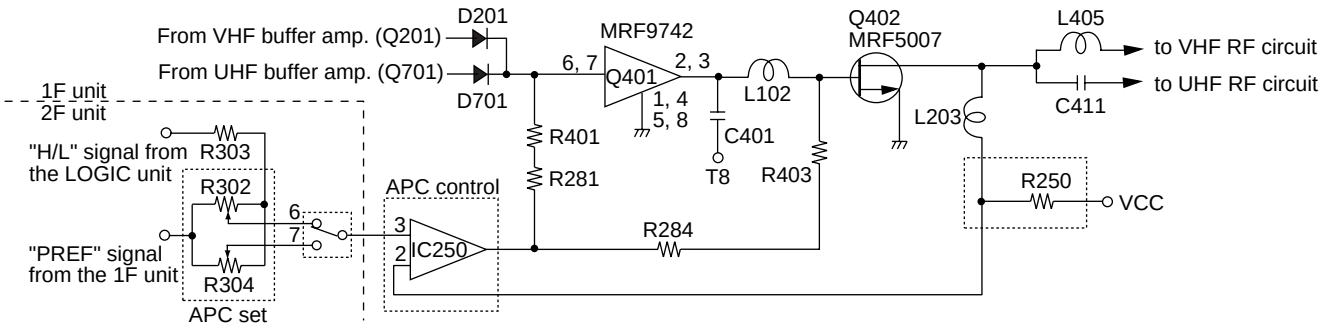
The DC voltage is also applied to the receiver tuned bandpass filters as a “VTUNE” signal.

4-3-2 UHF PLL CIRCUIT (1F UNIT)

The oscillated signal at the VCO circuit (DUAL VCO board; Q301, Q302, D301 and D302) is amplified at a buffer-amplifier (Q306) and is again amplified at another buffer-amplifier (Q352). The amplified signal is applied to the PLL IC (IC851, pin 19), and then divided by serial data from the CPU. It is the phase-detected with the divided reference frequency and the phase difference is output as pulses.

The output signals from IC851 (pin 13) are converted to DC voltages (lock voltage) by the loop filter (R866–R868, C862 and C864) and are then fed back to the UHF VCO circuit to stabilize the VCO frequency.

• APC CIRCUIT



4-4 POWER SUPPLY CIRCUITS

VOLTAGE LINE

LINE	DESCRIPTION
HV	The voltage from the external power supply or attached battery pack.
VCC	The same voltage as the HV line (external power supply or battery pack) which is controlled by the power switch ([POWER] control).
VHT2V	Common 3 V converted from the VCC line by the +3CPU regulator IC (LOGIC unit; IC2). The output voltage is supplied to the +3C, R3 and T4 regulator circuits, etc.
UHT2V	Common 3 V converted from the VCC line by the +3C regulator circuit (LOGIC unit; Q4, Q5, Q40 and D3) using the +3CPU regulator (LOGIC unit; IC2).
R3V	3 V for receiver circuit converted from the VCC line by the R3 regulator circuit (2F unit; Q4, Q5 and D402).
+3S	4 V for transmitter circuit converted from the VCC line by the T4 regulator circuit (1F unit; Q702, Q703 and D702). The T4 regulator circuit is controlled by the CPU (LOGIC unit; IC1, pin 45) via T4 control regulator circuit (1F unit; Q704).

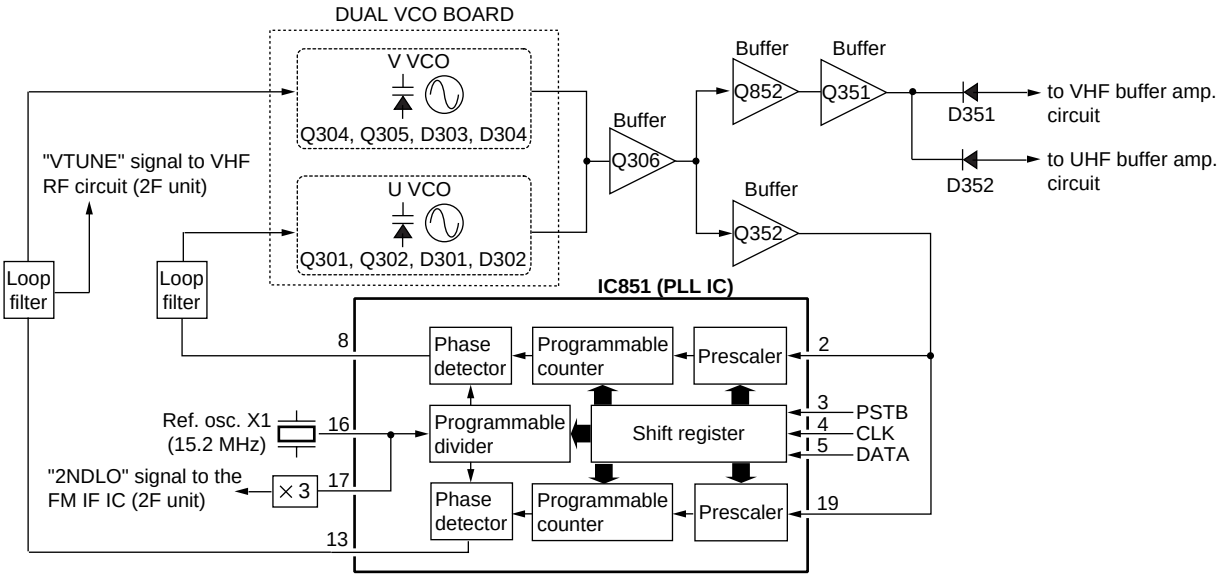
4-5 OTHERCIRCUITS

4-5-1 TONE SQUELCH CIRCUIT (LOGIC UNIT)

A portion of the detected audio signals from the “DETO” line are passed through the low-pass filter (IC13). The filtered signal is then applied to the CPU (IC1, pin 4), and is compared with the programmed tone signal. The CPU (IC1) outputs control signals to the AF mute and AF regulator circuits to open the squelch when a matched tone signal is received.

The programmed subaudible tone signal is output from the CPU (LOGIC unit; IC1, pin 9) directly when transmitting with a tone.

• PLL circuit



4-5 PORT ALLOCATIONS

4-5-1 CPU (LOGIC UNIT; IC1)

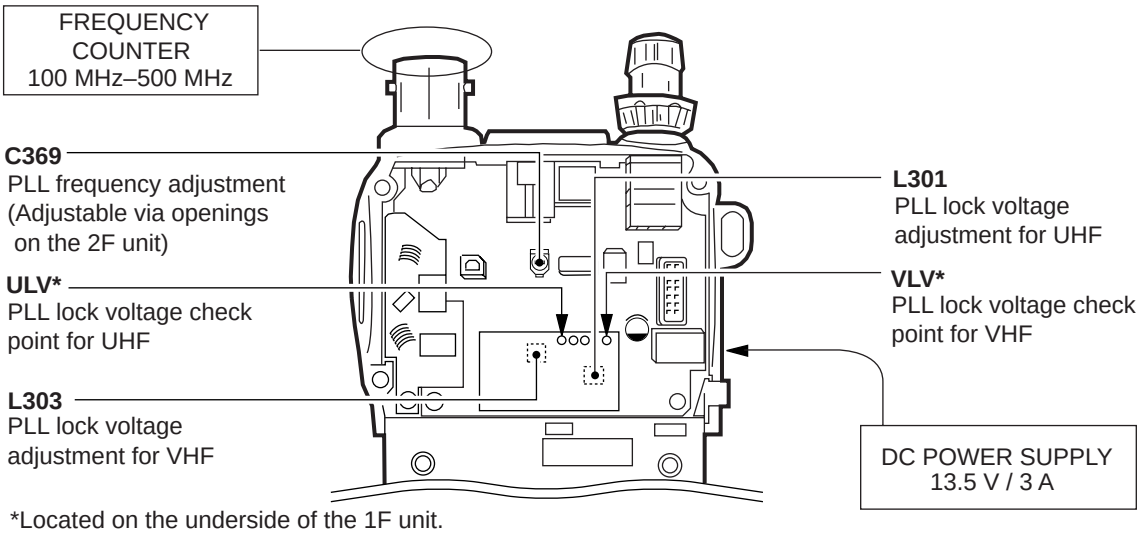
Pin number	Port name	Description
2	REMOTE	Input port for remote control signal from an optional HM-75A microphone via the [EXT MIC] jack.
3	SD	Input port for detected S-meter signals from the IC101 (pin 12) on the 2F unit.
4	CTCIN	Input port for received CTCSS tone signals.
5	PCON	Output port for +3C regulator circuit control signals. "HIGH" : Power ON.
6	PLST	Output PLL strobe signals.
7	PLCK/ECK	Output port for clock signals to PLL and EEPROM ICs.
8	PDA/UL	DATA bus line for PLL. • Outputs PLL DATA when PLL is locked. • When PLL is unlocked, PLL IC releases the port being pulled up, therefore, the CPU receives "HIGH" level signal.
9	CTCSS	Output port for CTCSS tone signals.
10	DTMF	Output port for: • Beep audio signals while receiving. • DTMF signals or 1,750 Hz tone signal while transmitting. (According to versions)
12	NOISE	Input pulse signals for noise squelch from the IC101 (pin 13) on the 2F unit.
17	LOCK	Input port for the [LOCK] switch. "LOW" : [LOCK] switch is ON.
21	DIUD	Inputs up/down signals from the [DIAL] control.
22	DICK	Input port for dial clock signals.
23	POWER	Input port for the [POWER] switch. "Low" : [POWER] switch is pushed.
24	CONT	Outputs LCD contrast control signals.
28–31	KR3–KR0	Input port for key matrix.
32	PTT	Input port for the PTT control circuit. "HIGH" : When transmitting.
33	RESET	Input port for reset circuit (LOGIC unit; IC3, pin 1).
39	CFC	Outputs control signals to the power supply of the CTCSS band-pass filter (LOGIC unit; Q45). "LOW" : Activates the BPF.
40	ESIO	DATA bus line for the EEPROM (LOGIC unit; IC15) data signals.
41	BLED	Outputs [BUSY] LED control signals. "HIGH" : The [BUSY] LED lights.
42	LIGHT	Outputs LCD backlight control signals. "High" : The backlight lights.
43	MICC	Output port for the microphone amplifier (LOGIC unit; IC12). "LOW" : Activates the mic. amplifier.
44	MM/RM	Output a mute signal. [MM] : Microphone mute for DTMF or 1,750 Hz tone while transmitting. [RM] : Audio mute for squelch circuit while receiving. "HIGH" : To mute one of above.
46	TXSEL	Outputs transmit frequency band control signals. "HIGH" : UHF band. "LOW" : VHF band.
47	HVCO	Output port for the UHF band VCO (DUAL-VCO board; Q301, Q302 and D301) control signals. "HIGH" : Activates the UHF-VCO.
48	LVCO	Output port for the VHF band VCO (DUAL-VCO board; Q304, Q305 and D303) control signals. "HIGH" : Activates the VHF-VCO.
49	SHIFT	Output port for SHIFT signals to the shift switches (1F unit; Q354, Q854). "HIGH" : Transmit on VHF. "LOW" : Transmit on UHF.
55	AFON	Outputs control signals to the AF regulator circuit (2F unit; Q151,Q152). "HIGH" : Activates the AF amplifier.
56	H/L	Output port for the TX output power (HIGH or LOW) select signals. "LOW" : HIGH power is selected.

SECTION 5 ADJUSTMENT PROCEDURES

5-1 PLL AND TRANSMITTER ADJUSTMENT

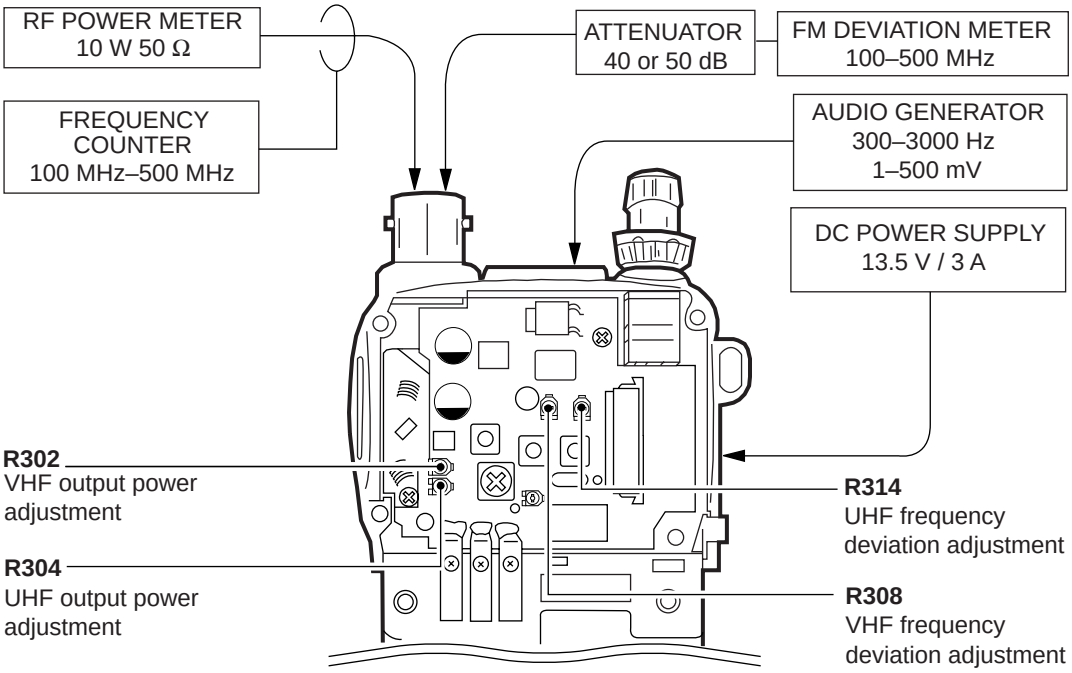
ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT	
			UNIT	LOCATION		UNIT	ADJUST
PLL LOCK VOLTAGE (VHF)	1	• Displayed frequency : 145.000 MHz • Receiving	1F	Connect a digital multimeter or an oscilloscope to the "VLV".	1.3 V	DUAL-VCO	L303
	2	• Transmitting			0.9 V – 1.7 V		Verify
(UHF)	1	• Displayed frequency : 440.000 MHz [USA-3] 430.000 MHz [Other] • Receiving		Connect a digital multimeter or an oscilloscope to the "ULV".	2.2 V		L301
	2	• Transmitting			1.9 – 2.5 V		Verify
PLL REFERENCE FREQUENCY	1	• Displayed frequency : 445.000 MHz [USA-3] 435.000 MHz [Other] • Transmitting	Top panel	Loosely couple a frequnecy counter to the antenna connector.	445.0000 MHz [USA-3] 435.0000 MHz [Other]	1F	C369
OUTPUT POWER	1	• Displayed frequency : 145.000 MHz • Output power: High • Transmitting	Top panel	Connect an RF power meter to the antenna connector.	5.5 W	2F	R302
	2	• Displayed frequency : 445.000 MHz [USA-3] 435.000 MHz [Other] • Output power: High • Transmitting			5.5 – 6.0 W		R304
FM DEVIATION	1	• Displayed frequency : 145.000 MHz • Connect an audio generator to the [MIC] connector and set as: 1 kHz/95 mV • Set the FM deviation meter as : HPF : OFF LPF : 20 kHz De-emphasis : OFF Detector : (P–P)/2 • Output power: High • Transmitting	Top panel	Connect an FM deviation meter to the antenna connector through an attenuator.	± 4.3 kHz	2F	R308
	2	• Displayed frequency : 445.000 MHz [USA-3] 435.000 MHz [Other] • Output power: High • Transmitting			± 4.3 kHz		R314
DTMF DEVIATION (USA-1,SEA only)	1	• Displayed frequency : 445.000 MHz [USA-3] 435.000 MHz [SEA] • Push [D] key while transmitting	Top panel	Connect an FM deviation meter to the antenna connector through an attenuator.	± 3.5 kHz	LOGIC	R147
TONE CALL DEVIATION (EUR, ITA only)	1	• Displayed frequency: 435.000 MHz • Push [TONE] key while transmitting	Top panel	Connect an FM deviation meter to the antenna connector through an attenuator.	± 3.5 kHz	LOGIC	R147

• **1F UNIT**

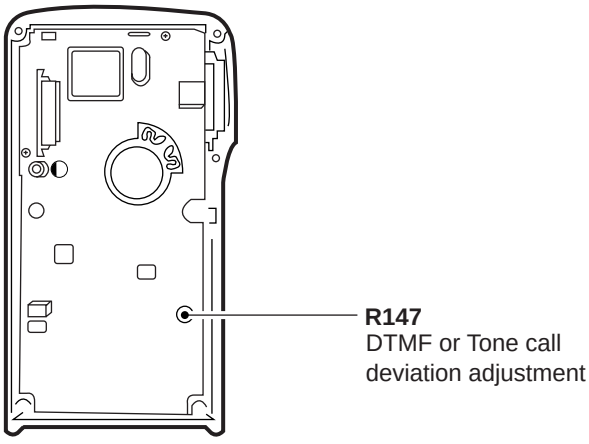


*Located on the underside of the 1F unit.

• **2F UNIT**



• **LOGIC UNIT**

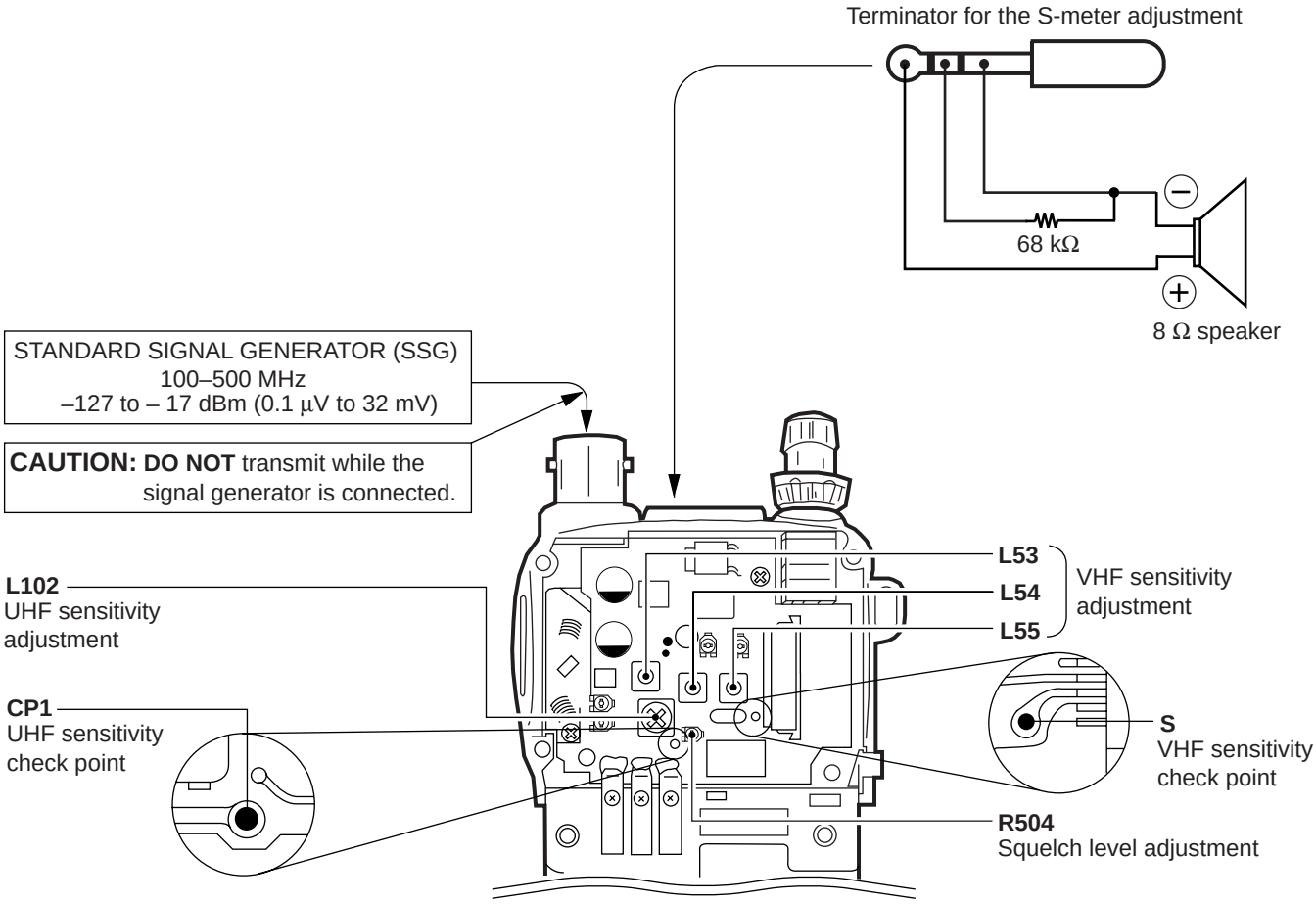


5-2 RECEIVER ADJUSTMENT

ADJUSTMENT		ADJUSTMENT CONDITION	MEASUREMENT		VALUE	ADJUSTMENT POINT	
			UNIT	LOCATION		UNIT	ADJUST
VHF SENSITIVITY	1	• Displayed frequency : 145.000 MHz [EUR] 146.000 MHz [Other] • Connect an SSG to the antenna connector and set as : Level : 1.0 mV* (–47 dBm) Modulation : 1 kHz Deviation : ±3.5 kHz • Receiving	2F	Connect a digital multimeter or oscilloscope to the check point “S”.	Maximum DC voltage	2F	Adjust in sequence L53, L54, L55
UHF SENSITIVITY	1	• Displayed frequency : 445.000 MHz [USA-3] 435.000 MHz [Other] • Connect an SSG to the antenna connector and set as : Level : 1.0 mV* (–47 dBm) Modulation : OFF • Receiving	2F	Connect a digital multimeter or oscilloscope to the check point “CP1”.	1.0 V		L102
SQUELCH LEVEL	1	• Displayed frequency : any • Connect an SSG to the antenna connector and set as : Level : 0.089 µV* (– 128 dBm) Modulation : 1 kHz Deviation : ± 3.5 kHz • Pre-set the R504 to maxmum CW. • Receiving	Seaker		At the point where the AF signal just disappears.	2F	R504
S-METER	1	• Displayed frequency : 443.000 MHz [USA-3] 433.000 MHz [Other] • Connect an SSG to the antenna connector and set as : Level : 0.5 µV* (– 113 dBm) Modulation : 1 kHz Deviation : ± 3.5 kHz • Connect a terminator to the [EXT SP] jack. • Receiving	Front panel			Push and hold the [CALL] key.	
	2	• Set an SSG output level for the S-meter to S3 (4 dots).	SSG	Output level	0.28 to 0.89 µV (– 118 to – 108 dBm)		Verify

*This output level of the standard signal generator (SSG) is indicated as SSG’s open circuit.

• **2F UNIT**


Terminator for the S-meter adjustment
68 kΩ
8 Ω speaker
STANDARD SIGNAL GENERATOR (SSG)
100–500 MHz
–127 to – 17 dBm (0.1 μV to 32 mV)
CAUTION: DO NOT transmit while the signal generator is connected.
L102
UHF sensitivity adjustment
CP1
UHF sensitivity check point
L53
L54
L55
VHF sensitivity adjustment
S
VHF sensitivity check point
R504
Squelch level adjustment