EXPOSITORY STATEMENT

1.	NUMBER OF BANDS	=	1
2.	NUMBER OF CHANNELS	=	Per Manual
3.	TUNING RANGE	=	136.00-174.00MHz
4.	OSCILLATOR RANGE, MHz	=	105.150-143.150MHz
5.	I.F., MHz	=	30.850MHz-0.45MHz
6.	BLOCK DIAGRAM	=	ATTACHED

CIRCUIT DESCRIPTION

1. RECEIVER CIRCUIT

1-1 ANTENNA SWITCHING CIRCUIT

Received signals passed through the low-pass filter (L2, L3, C3-C5) . The filtered signals are applied to the $\lambda/4$ type antenna switching circuit (D8, D32, L16, C77, C78).

The antenna switching circuit functions as a low-pass filter While transmitting. However, its impedance becomes very high while D8 and D32 are turned ON. Thus transmit signals are blocked from entering the receiver circuits. The antenna switching circuit employs a $\lambda/4$ type diode switching system. The passed signals are then applied to the RF amplifier circuit.

1-2 RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through a band pass filter (D10, L26) after amplified at the RF amplifier (Q29) . The filtered signals are amplified at the another RF amplifier (Q12), then applied to the 1st mixer circuit after suppress out-of-band signals at the band pass filter (D11, D12, C92, C94, C96, C236).

D10-D12 employs varactor diodes that track the band pass filters and are controlled by the T4/PWR signal from the CPU (1C8) . These diodes tune the center frequency of an RF pass band for wide bandwidth receiving and good image response rejection.

1-3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, Only the desired frequency will be passed through a crystal filter at the next stage of the 1st mixer.

The signals from the RF circuit are mixed at the 1st mixer (Q13) with a 1st LO signal coming from the VCO circuit to Produce a 30.85MHz 1st IF signal.

The 1st IF signal is applied to a crystal filter(F11) to Suppress out-Of-band signals. The filtered 1st IF signal is applied to the IF amplifier (Q14), then applied to the 2nd mixer circuit (IC2, Pin16).

1-4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF Signal. A double conversion super heterodyne system (which converts receive signal twice) improves the image rejection ratio and obtains stable receiver gain.

The 1st IF signal from the IF amplifier is applied to the 2nd mixer section of the FM IF IC (IC2, Pin16), and is mixed With the 2nd LO signal to be convened to a 450kHz 2nd IF Signal.

The FM IF IC contains the 2nd mixer, limiter amplifier, quadrature detector and active filter circuits. A 30.4 MHz 2nd LO signal is produced at the PLL circuit by dividing it's reference frequency.

The 2nd IF signal from the 2nd mixer (IC2, Pin3) passes through a ceramic filter (F12) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier (IC2, Pin5) and applied to the quadrature detector (IC2, Pins 10, 11) to demodulate the 2nd IF signal in to AF signals.

1-4 AF CIRCUIT

AF signals from the FM IF IC (IC2 pin 9) are applied to the mute switch (IC4, Pin 1) via the AF filter circuit (IC3b, Pins 6, 7) . The out put signals from pin 11 are applied to the AF power amplifier (IC5, Pin 4) after passed through the [VOL] control (VR board, R1).

The AF signals from the [VOL] control are applied to the AF power amplifier circuit (IC5, Pin4) to obtain the specified audio level. The amplified AF signals, output

from pin 10, are applied to the internal speaker (SP1) via the 【EXT SP】 jack when no plug is connected to the jack.

1－5 SQUELCH CIRCUIT

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF Signals, the squelch switches the AF mute switch.

A portion of the AF signals from the FM IF IC (1C2, Pin 9) are applied to the active filter section (1C2, Pin8) where noise components are amplified and detect with an internal noise detector. The squelch input level adjustment pot (R92) is connected in parallel to the active filter input (pin 8) to control the input noise level.

The trigger Circuit converts the detected signals to a HIGH Or LOW signal and applies this (from pin 13) to the CPU (1C8, Pin 19) as the "NOIS" signal. When the CPU receives a HIGH level "NOIS" signal, the CPU controls the "MMUT" line to cut the AF signals at the mute switch IC (1C4). At the same time, the "AF ON" line controls the AF regulator circuit (Q15, Q16) to cut out the VCC power source for the AF power amplifier (1C5).

2. TRANSMITTER CIRCUITS

2－1 MICROPHONE AMPLIIER CIRCUIT

The microphone amplifier circuit amplifies audio signals with +6dB／octave pre－emphasis characteristics from the microphone to a level needed for the modulation circuit.

The AF signals from the microphone are applied to the microphone amplifier circuit (IC3c, Pin 10). The amplified AF signals are passed through the low－Pass filter circuit (IC3d, Pins 13, 14) via the mute switch (1C4, Pins 2-4) . The filtered AF signals are applied to the modulator circuit after Passed through the mute switch (IC4, Pins 8－10) and the deviation adjustment pot (R119).

2－2 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signal.

The audio signals (SHIFT) change the phase at D6 to modulate an oscillated signal at the VCO (Q7, Q8). The oscillated signal is amplified at the buffer-amplifiers (Q4, Q6), then applied to the T/R switching circuit (D3, D4).

2-3 DRIVE/POWER AMPLIFIER CIRCITS

The signal from the VCO circuit passes through the T/R switching circuit (D3) and is amplified buffer (Q3), drive (Q2) and power amplifier (Q1) to obtain 5.5 W of RF power (at 9.6 V DC/typical). The amplified signal passes through the antenna switching circuit (D1), and low-pass filter (L2, L3, C3-C5) and then applied to the antenna connector (J1).

The bias current of the drive (Q2) and power amplifier (Q1) is controlled by the APC circuit to stabilize the output power.

2-4 CURRENT DETECTOR CIRCUIT

The current detector circuit (Q9, Q28) detects total driving current of the drive and the power amplifiers, using the current sensor (R161) . The deferential amplifier (Q9) detects voltage deference of the current sensor input and output voltages, then outputs control voltage to the APC circuit.

2-5 APC CIRCUIT

The APC circuit (IC3a, Q37) provides stable output power from the drive and the power amplifiers even when the input voltage or temperature changes ; and, Selects HIGH or LOW output power.

The output voltage from the current detector circuit is applied to the inverting amplifier (IC3a, Pin 2), and "T4/PWR" signal from the CPU (IC8, Pins 54-59) is applied to the other input for reference.

When the output power or the driving current changes, input voltage of the deferential amplifier (Q9 pin 1) will be decreased. In such case, input voltage of the inverting amplifier (pin 2) is increased to stabilize the output power.

Q37 is controlled by the "TXC" signal from the CPU (IC8, Pin 50) to select HIGH or LOW output power.

3. PLL CIRCUIT

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL circuit contains VCO circuit (Q7, Q8, D5, D6). The oscillated signal is amplified at the buffer-amplifiers (Q5, Q6) and then applied to the PLL IC (IC1, Pin2).

The PLL IC contains prescaler, Programmable counter, programmable divider, Phase detector and charge pump, etc. The entered signal is divided at the prescaler and Programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency.

If the oscillated signal is drifts, the phase of its changes from the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

A portion of the VCO signal is amplified at the buffer-amplifier (Q4, Q6) and is then applied to the receive 1st mixer or transmit buffer-amplifier circuit via the T/R switching diode (D3, D4).