IC-R75 CIRCUIT DESCRIPTION

3-1 RECEIVER CIRCUITS

3-1-1 RF SWITCHING CIRCUIT (MAIN UNIT)

The IC-R75 has two antenna connectors. RF signals enter either the [50 Ω ANT.] or [450 Ω ANT.] connector.

RF signals from the [50 Ω ANT.] connector are applied to the antenna switching circuit (RL121), and then pass through the low-pass filter (L131, L132, C131–C136).

RF signals from the [450 Ω ANT.] connector are passed through the L101 to exchange the impeadance value, and are then applied to the antenna switching circuit (RL121). The signals are applied to the low-pass filter (L131, L132, C131–C136).

Each RF signals from the [50 Ω ANT.] connector or [450 Ω ANT.] connector are chosen by the antenna switching circuit (RL121).

3-1-2 RF FILTER CIRCUIT (MAIN UNIT)

The filtered signals are applied to the RX attenuator switching circuit (RL141). Either the signals bypass or pass through the attenuator circuit. The signals are attenuated at 20 dB when passing through the attenuators. The attenuator system excludes non-linear components between an antenna connector and an attenuator to prevent strong signals from causing distortion. The signals are then applied to the RF filters. The MAIN UNIT has 8 RF bandpass fileters for signals above 2.0 MHz and 2 low-pass filters for signals below 2.0 MHz.

(1) Below 1.6 MHz

The signals are applied to the low-pass filter consisting of C170–C175, L171–L173 via the limitter circuit (D141, D142). A diode is removed at the entrance of the low-pass filter. This device prevents the diode from causing distortion when receiving very strong signals. A switching diode (D172) is turned on when the “B0” line is “HIGH”.

(2) Above 1.6 MHz

The signals are applied to the high-pass filter consisting of C161–C163, L161–L164. This filter suppresses strong signals below 1.6 MHz such as broadcasting stations.

The filtered signal between 1.6 MHz and 2.0 MHz are applied to the low-pass filter (C182–C187, L182, L183) via the switching diode (D181). The switching diodes (D181, D182) are turned ON when the “B1” line is “HIGH”.

The filtered signals above 2.0 MHz are applied to one of 8 bandpass filters depending on the receive frequencies.

After passing through a bandpass or low-pass filter, the signals are applied to the pre-amplifier circuit (Q381, Q382, IC391).

(3) FILTER SWITCHING CIRCUIT

The RF bandpass filter corresponds to the BPF switching voltage (B0–B9) based on the CPU via the shifit registor (IC551, IC552) and driver (IC561, IC562). The switching voltage of the BPF exit ot improve multi-signal and strong signal characteristics.

3-1-3 PRE-AMPLIFIER CIRCUIT (MAIN UNIT)

The pre-amplifier circuit uses low noise junction FETs (Q381, Q382) or wideband amplifier (IC391) to provide gain over a wide frequency range.

When the [P.AMP] switch is turned “PREAMP 1”, the signals from the RF filter are amplified by the junction FETs pre-amplifier circuit (Q381, Q382).

When the [P.AMP] switch is turned “PREAMP 2”, the signals from the RF filter are amplified by the wideband pre-amplifier circuit (IC391).

When the [P.AMP] switch is turned “PREAMP OFF”, the signals from the RF filter bypass the pre-amplifiers through D371 and D372.

The amplified or bypassed signals are applied to the 1st mixer circuit (Q441, Q442) via the low-pass filter (L431, L432 and C431–CC436). The low-pass filter attenuates at 50 MHz to suppress image frequency.

3-1-4 1ST MIXER AND IF CIRCUITS (MAIN UNIT)

The filtered signals are mixed with a 69.0415–129.0115 MHz 1st LO signal to produce a 69.01 MHz 1st IF signal at the 1st mixer circuit (Q441, Q442).

The 1st mixer circuit employs a balanced mixer using low-noise junction FETs (Q441, Q442) to expand the dynamic range.
The 69.0415–129.0115 MHz 1st LO signal is applied to an LO amplifier (Q411) from the PLL unit via J411, and then passes through the low-pass filter (L421, L422, C422–C425). The filtered signal is applied to the 1st mixer circuit.

The 1st IF signal is applied to the crystal bandpass filter(FI-461) to suppress out-of-band signals. The filtered signal is amplified at a 1st IF amplifier (Q471), and then applied to a 2nd mixer circuit (D491)

3-1-5 2ND MIXER AND IF CIRCUITS (MAIN UNIT)

The 1st IF signal is mixed with a 60.0 MHz 2nd LO signal to produce 9 MHz 2nd IF signal at the 2nd mixer (D491, C492, L491, L492). The 6.0 MHz 2nd LO signal is applied to the 2nd mixer from the PLL unit via J491.

The 9 MHz 2nd IF signal is applied to the crystal bandpass filter (FI701) to suppress unwanted signals.

The filtered signal enters the noise blanker gate (D711–D714). The signal is applied to L712 to obtain clear reception and is then amplified at the 2nd IF amplifier (Q721). The signal passes through a loose resonator circuit (C726, L721) and then is applied to one of the two crystal bandpass filters.

When the [FIL] switch is turned “2F3K”, the filter is selected FI761 which covering the 2.4 kHz bandwith.

When the [FIL] switch is turned “2FOP”, the filter is selected an optional filter.

When the [FIL] switch is turned “2FTH”, the signal from the 2nd IF amplifier bypass the crystal bandpass filters through D771 and D773.

The filtered or bypassed signal is amplified at the buffer amplifier (Q801) and applied to the 3rd mixer circuit (IC811).

3-1-6 NOISE BLANKER CIRCUITS (MAIN UNIT)

The IC-R75 uses a trigger noise blanker circuit which removes pulse-type noise signals at the noise blanker gate (D711–D714).

The 2nd IF signal passes through the crystal bandpass filter (FI701) to suppress unwanted signals. A portion of the output signal is applied to a noise amplifier circuit (IC731, Q731, Q733) and detected at a noise detector circuit (D731). The detected voltage is applied to a noise blanker gate control circuit (Q735–Q737, D732).

The threshold level of the noise blanker gate control circuit (Q735–Q737, D732) is set at 1.0 V on SSB mode (In case of AM mode, is set at 1.6 V). When the detected voltage exceeds the threshold level, Q737 outputs a blanking signal to activate the noise blanker gate (D711–D714).

A portion of the detected voltage is applied to the noise blanker AGC circuit (Q732, Q734). The noise components are fed back to the noise amplifier (IC731). The time constant of the noise blanker AGC circuit is determined by R737, R744 and C739. This AGC circuit does not operate to detect pulse-type noise.

When the operating frequency or mode is changed, the “UNLC” signal is applied to the noise blanker gate control circuit (D732). The noise blanker gate prevents PLL click noise.

3-1-7 3RD MIXER AND IF CIRCUITS (MAIN UNIT)

The 2nd IF signal is mixed with a 9.4665 MHz 3rd LO signal to produce a 450–456 kHz 3rd IF signal at the 3rd mixer (IC811).

The 9.4665 MHz 3rd LO signal is applied to the 3rd mixer IC (IC811, pin 10) from the PLL unit via J811. The 450–456 kHz 3rd IF signal is applied either to one of the 3 ceramic bandpass filters (FI851, FI861, FI871) or to an optional crystal bandpass filter to suppress unwanted signals.

When the [FIL] switch is turned “3F3K”, the filter is selected FI851 which covering the 2.4 kHz bandwith.

When the [FIL] switch is turned “3F6K”, the filter is selected FI861 which covering the 6 kHz bandwith.

When the [FIL] switch is turned “3F15”, the filter is selected FI871 which covering the 15 kHz bandwith.

When the [FIL] switch is turned “3FOP”, the filter is selected an optional crystal bandpass filter.

When the mode is selected SSB mode, the filtered 3rd IF signal is amplified at the 3rd IF amplifier (Q891), and is then applied to the 3rd IF amplifier (Q911) via the receiver total gain control circuit (R898). The amplified signal is applied to the SSB demodulator circuit.

When the mode is selected FM mode, the filtered 3rd IF signal is amplified at the 3rd IF amplifier (Q891), and is then applied to the FM demodulator circuit.

When the mode is selected AM mode, the filtered 3rd IF signal is amplified at the 3rd IF amplifier (Q891), and is then applied to the 3rd IF amplifier (Q911) via the receiver total gain control circuit (R898). The amplified signal is applied to the AM demodulator circuit.

1st, 2nd and 3rd IF amplifiers (Q471, Q721, Q891) are controlled by AGC bias voltage.

3-1-8 BFO CIRCUIT (PLL UNIT)

The BFO (Beat Frequency Oscillator) circuit consists of Q1, X1, Q201 and IC 201 on PLL unit. The oscillator provides a beat frequency signal to the SSB demodulator circuit (MAIN UNIT; IC1101) for demodulating the 3rd IF signal into an AF signal.
The 30 MHz signal is oscillated at Q1 and X1 for the system clock signal of the DDS IC (IC201). The oscillated signal is amplified at Q201 and is applied to the DDC IC (IC201, pin 7) to produce the 455 kHz BFO signal.
The 455 kHz signal passes through the low-pass filter (L201, L202, C202–C207) via the D/A converter, and is then mixed with the 3rd IF signal at the SSB demodulator circuit (MAIN unit; IC1101).

3-1-9 DEMODULATOR CIRCUIT (MAIN UNIT)

The demodulator circuit consists of 3 detector circuits.

(1) SSB DEMODULATOR CIRCUIT

A product detector (IC1101) demodulates SSB, RTTY and CW signals into an AF signal. The 3rd IF signal from the IF amplifier (Q911) is mixed with the BFO signal at the product detector (IC1101) to be demodulated into an AF signal. The AF signal passes through the AF input mode selector switch (IC1201).

(2) FM DEMODULATOR CIRCUIT

A FM detector (IC1001, X1001) demodulates the FM signal into an AF signal. The 3rd IF signal from the IF amplifier (Q891) is amplified at the 3rd IF amplifier (Q1001), and is then applied to the FM detector (IC1001, X1001) to demodulate the 3rd IF signal. The demodulated signal is applied to the de-emphasis circuit (IC1211D) to produce the FM AF signal. The AF signal passes through the AF input mode selector switch (IC1201).

The FM detector outputs “FMNL” signal from IC1001, pin 14 is applied to the CPU (LOGIC unit; IC101, pin 94) to control the noise squelch level.

(3) AM DEMODULATOR CIRCUIT

The AM demodulater circuit (IC2001) has the envelope detect function and the synchronous detect function.
An AM detector (IC2001) demodulates the AM signal into an AF signal. The 3rd IF signal from the IF amplifier (Q911) is amplified at the buffer amplifier (Q1031), and is then applied to the AM demodulater circuit (IC2001)to demodulate the 3rd IF signal into the AM AF signal. The AF signal which is the AM envelope detect the AF signal or the AM synchronous detect AF signal passes through the AF input mode selector switch (IC1201).

3-1-10 AF INPUT MODE SELECTOR SWITCH (MAIN AND LOGIC UNITS)

The AF input mode selector switch (MAIN unit; IC1201) consists of 4 analog switches. The switches are selected mode signals of “AFS1” and “AFS2” from the CPU (LOGIC unit; IC101) via the shift registor (MAIN unit; IC1601), and are selected by the squelch control signal from the CPU (LOGIC unit; IC101). The AF signal is output from IC1201 (MAIN unit; pin 13).

3-1-11 AF AMPLIFIER CIRCUIT (MAIN AND FRONT UNITS)

The AF signal output is passed though the low-pass filter (IC1211) to suppress unwanted signals. The filtered signal is mixed with “BEEP” signal at the AF level variable circuit (MAIN unit; IC1251), and is then applied to the AF amplifier circuit and the AF level variable circuit (IC1251).
The AF level variable circuit controls the AF level by the “AF GAIN” (R141) on the VR BOARD. The AF signal is applied to the AF mute circuit to suppress the noise when “AF GAIN” (R141) level is minimum, and is then power-amplified at IC1291 on the MAIN unit to drive the speaker.

The one of the AF amplified signal is output “AAFO” signal to record the AF signal to the AF recording jack (PLL unit; J3).

3-1-12 AGC AND S-METER CIRCUITS (MAIN UNIT)

The AGC (Automatic Gain Control) circuit reduces signal fading and keep the audio output level constant. The receiver gain is determined by voltage on the AGC line (Q1063, collector). When strong signals are received, the AGC circuit decreases the voltage on this line.

The 3rd IF signal is amplified at the IF amplifier (Q911). A portion of the 3rd IF signal is applied to the buffer amplifier (Q1031) to convert the impedance. The amplified IF signal is detected at the AGC detector (D1061) via the C1061, and enters the base of the AGC amplifier (Q1063) to control the voltage on the AGC line.

The AGC mode is selected by the receiver mode or AGC swtich on the front panel using the delay control circuit (Q1064–Q1066). The MDAT signal from the CPU (LOGIC board; IC101, pin 21) is applied to the shift resistor (IC1601, pin 2) to produce the AGSS and the AGFS signals. The AGSS signal is applied to the Q1064, the AGFS signal is applied to the Q1065, the AGRS signal from the CPU (LOGIC unit; IC101, pin 80) is applied to the Q1066 to control the delay control circuit.
The AGRS signal resets the AGC circuit when IC-R75 is working the memory scaning.

When the AGC switch is selected “OFF”, the Q1061 do not supply the voltage to the AGC amplifier (Q1063) via the “AGOS” line, determining the time constant to deactivate the AGC circuit.

A portion of the AGC bias voltage is amplified at the S-Meter amplifier circuit (IC1211C, D831), and then applied to the CPU (LOGIC unit; IC101, pin 95) via the “SML” line. Thus, the CPU controls S-Meter display.

3-1-13 SQUELCH CIRCUIT (MAIN AND LOGIC UNIT)

The “SML” signal is applied to the CPU (LOGIC unit; IC101, pin 91) from the meter amplifier circuit (IC1211C, D831). The CPU compares “SML” signal with the level of SQL volume on the VR BOARD to control the “SQL” signal.
The CPU is output the “SQLS” signal from pin 81, and then applied to the AF selector circuit (MAIN unit; IC1201, pin 6) which has also the squelch gate circuit.

3-2 PLL CIRCUIT

3-2-1 GENERAL DESCRIPTION

The PLL unit generates a 1st LO signal (69.0415–129.0115 MHz variable), 2nd LO signal (60 MHz) and 3rd LO signal (9.4665 MHz) used in the MAIN and BFO units.
The IC-R75 uses a DDS (Direct Digital synthesizer) system. The DDS system provides rapid lockup time and high quality frequency oscillation.

3-2-2 REFERENCE OSCILLATOR CIRCUIT (PLL CIRCUIT)

The 30 MHz reference oscillator circuit consists of X1 and Q1. The 30 MHz reference frequency is oscillated to produce all of the LO signals.

3-2-3 1ST LO CIRCUIT (PLL AND MAIN UNIT)

The 30 MHz reference frequency is applied to the DDS-IC (PLL unit; IC21, pin 40) to oscillate the 1st LO signal. The reference frequency is compared to the DDS output signal (PLL unit; IC21, pin 46) to oscillate the PLL lock voltage. The PLL lock voltage controlls the oscillate frequency of the VCO1 and VCO2 circuit.

The oscillated signal at the VCO1 and VCO2 circuit is amplified at the LO-amplifier (PLL unit; Q91), and passes through the low-pass filter (PLL unit; Q92, D91, D92, L91, L93, C96–C100, C102, C103) to supperss high harmonic components. The low-pass filter controlls the cut-off frequency of less than 29.999 MHz and more than 30.000 MHz by switching C102 and C103 “ON” and “OFF” respectively.

The filtered signal is applied to the LO-amplifier (MAIN unit; Q411), and is then applied to the 1st mixer circuit (MAIN unit; Q441, Q442) via the low-pass filter (MAIN unit; L421, L422, C422–C425).

The reference frequency from the LO-amplifier (PLL unit; Q91) is also divided by 4 at IC22, and is amplified at the IC23. The signal is applied to the DDS-IC (PLL unit; IC21, pin 88) for the clock signal.

3-2-4 2ND LO CIRCUIT (PLL AND MAIN UNIT)

The 30 MHz reference frequency from the Q1 and X1 on the PLL unit is multiplied by 2 at Q2 on the PLL unit. The 60 MHz 2nd LO signal is obtained at the L4 and L5 on the MAIN unit, and is then applied to the 2nd mixer circuit (MAIN unit; D491) via the 3dB attenuator (MAIN UNIT; R491–R493).

3-2-5 3RD LO CIRCUIT (PLL AND MAIN UNIT)

The 30 MHz reference frequency is oscillated at the Q1 and X1 on the PLL unit, and is then amplified at the Q151 on the PLL unit. The amplified signal is applied to the 10 bits DDS-IC (PLL unit; IC151, pin 7) for the clock signal to produce the 9.4665 MHz 3rd LO signal. The 3rd LO signal is applied to the D/A converter circuit, and passes through the low-pass filter (PLL unit; L151, L152, C152–C157) to suppress spurious components. The filtered 9.4665 MHz 3rd LO signal is applied to the 3rd mixer circuit (MAIN unit; IC811, pin 10)

3-2-6 BFO LO CIRCUIT (PLL AND MAIN UNIT)

The 30 MHz reference frequency is amplified at the Q201 on the PLL unit, and is applied to the 10 bits DDS-IC (PLL unit; IC201, pin 7) for the clock signal to produce the 455 kHz BFO LO signal. The BFO LO signal is applied to the D/A converter circuit, and passes through the low-pass filter (PLL unit, L201, L202, C202–C207) to suppress spurious components. The filtered 455 kHz BFO LO signal is applied to the BFO mixer circuit (MAIN unit; IC1101, pin 10).

3-2-7 VCO CIRCUIT

The VCO circuit consists of the VCO1 circuit (PLL unit; Q71, Q72, D71) and VCO2 circuit (PLL unit; Q81, Q82, D81).
The VCO1 controls less than displayed frequency of 29.999 MHz to use the PLL lock voltage from the DDS-IC.
The VCO2 controls more than displayed frequency of 30.000 MHz to use the PLL lock voltage from the DDS-IC.

3-3 LOGIC CIRCUIT

The LOGIC circuit consists of the CPU, the reset circuit, backup battery circuit, and so on.

3-3-1 CPU (LOGIC UNIT)

The CPU (IC101) contains 8-bit one chip CPU. The CPU controls the operating frequency, mode, function, display, panel switches, panel volumes.

The panel switches are connected the CPU input port to the function of the panel switch or are connected some functions of panel switches to the A/D converter input port in the CPU.

The CI-V signal which is used for communicate to the personal computer is controlled by the level control circuit (IC401A, IC401B, Q401 and so on).

The CPU has the clock function. Thus, the CPU and the clock function have the crystal separately. The CPU has the 9.8304 MHz crystal (X112) for the CPU clock, and then the oscillated 9.8304 MHz signal is applied to the IC101, pin 7 and 8. The clock function has the 32.768 kHz crystal (X111). The oscillated 32.768 kHz signal is applied to the CPU (IC101, pin 4 and 5).

When the power is “OFF”, the EEPROM (IC231) is used for keep on saving the data of memory channels, and so on.

3-3-2 RESET CIRCUIT (LOGIC UNIT)

The reset circuit consists of Q391, D381, D382, D393, IC391 and IC392. When IC-R75 is supplied 13.8 V to connect the AC adapter, the “HV” signal is applied to the IC391, pin 2. The signal which is output from the IC391, pin 1 is applied to the IC392, pin 1. The signal is applied to the Q391, and is then output to the CPU (IC101, pin 9) as “CRES” reset signal.
A portion of the output signal from the IC392 is input to the CPU (IC101, pin 82) as “BKUP” signal to backup the clock data.

3-3-3 BACKUP SWITCH CIRCUIT (LOGIC UNIT)

IC-R75 has a backup switch circuit (Q511 and Q512). When the power is ON, the “H5V” signal is applied to Q512, pin 4, and then Q511 is OFF. When the AC adapter is disconnected, the “BATT” signal from the battery (MAIN unit; BT1521) is applied to the Q511, and then Q512 is OFF.
The output signal is applied to the CPU (IC101, pin 31) as “B5V” signal to keep on working the clock function.
The backup battery is not used while the AC adapter is connected.