CIRCUIT DISCPRIPTION

PLL

19.200MHz reference signals from X1 are fed to IC3, and are be came 5KHz or 6.25KHz reference signals for phase detector.
The output signals from VCO1 and VCO2 are fed to pin19 and pin2 of IC3 through C257 and C115 for phase detection.
The phase detected signals from pin13 and pin8 of IC3 are filtered by loop filter, and fed to VCO

19.200MHz signals from X1 are amplified by buffer amplifier inside IC3, and are came out from pin17 of IC3. This signals are used as 3rd LO signals
D18 is varactor diode, and used for controlling X1 frequency

VCO1 consists of Q28 and Q30, and generates 267.2-550MHz
The output signals from VCO are amplified by IC4 and are fed to both IC3 and Q40

VCO2 consists of Q6, L45, D17, C80, C207 and C208, and generates 260MHz signals for assisting 5KHz or 6.25KHz offset problem

This PLL also employs frequency doubler, DBL1 and DBL2.
DBL1 are multiplying 274.85-400MHz signals from VCO1.
DBL2 are multiplying 380.45-521.65MHz signals from VCO1
Both output signals from boubler are fed to mixer as 1st LO signals

Receiver

Incoming 2 meter signals (118-175MHz) are amplified by Q14, and filtered by band pass filter, which consists of L28, D1, L1 and D2.
Incoming 430MHz signals (330-470MHz) are amplified by Q35, and are filtered by band pass filter, which consists of L61, D4, L60 and D5
Incoming signals between 30-118MHz, also between 175-330MHz are amplified by Q36.
Incoming signals between 470-833MHz are amplified by Q24
Incoming signals between 833-1300MHz are amplified by Q26
Incoming signals between 0.5-30MHz are fed to one of three band pass filter, and then are amplified by Q505

The amplified incoming signals from front end are fed to 1st mixer, and are converted to 266.7MHz 1st IF signals.
1st IF signals from mixer are filtered by FI1, 1st IF filter, and are fed to 2nd mixer for generating 19.65MHz 2nd IF signals.
The output signals from 2nd IF mixer are filtered again by FI3. However if radio was setected wide FM mode, The radio

bypasses FI3 filter.

The filtered incoming 2nd IF signals are amplified by Q5, are fed to IC2.
IC2 is IF IC chip, and it consistes of 3rd mixer, IF limiter amplifier, demodulator and RSSI.
The incoming 2nd IF signals at IC2 are mixed with 3rd LO signals from PLL, are put out from pin3 of IC2 as 450KHz 3rd IF signals.
In the narrow FM mode, incoming 3rd IF signals are filtered by FI2, and are amplified / demodulated by IC2 and L12.
The demodulated audio signals are came out from pin9 of IC2
In the wide FM mode, incoming 3rd IF signals are fed to pin5 of IC2 without filtering, and are amplified / demodulated by IC2 and L12.
The demodulated audio signals are came out from pin9 of IC2
Q41 adds R55 to R54 for wide FM demodulation.
In the AM mode, incoming 3rd IF signals are filtered by FI2, are amplified by Q1 and then are demodulated by Q4.
Also this demodulation circuit are used as AGC.

In the narrow FM mode, the incoming demodulated audio signals are filtered by de-emphasis filter and high pass filter, and are amplified by Q31
In the wide FM mode, the incoming demodulated audio are amplified by Q31 without filtering the signals.
In the AM mode, the incoming demodulated audio are filtered by high pass filter, and are amplified by Q31.

The amplified audio signals at Q31 are pass through Q37, IC14,Q36 and IC15, and drives speaker.
Q37 mute circuit and IC14 electronics volume circuit are controlled by IC1 through AMUTE and VRC signal line.

The signals from WFMS line are filtered by IC9 low pass filter, and are fed to remote line of IC11.
IC11 will puts out beep signals, and will turns off Tone SQL if tone is matched.

X1 and IC11 generates clock signals.
IC5 detects DC power condition, and when turning DC power on, IC5 will send reset signals to reset port on IC11.

IC2 is EEPROM and it stores radio information.
DS2 is lamp, and it controlled by IC11 and Q38.

IC10, L1 and D4 are DC to DC converter and it generates 3.5V.
IC3 and IC4 are regulater