Theory of Operation

MAIN unit

1.Receive Block

1-1 Antenna Switch

Radio frequency signals input from the antenna circuit pass through the LPF (made up of L13, L14, C107~109 and C111),
and are routed to the RF Amp after passing through the antenna switch, (made up of D10, D15, L15 and C197~C198).

1-2 RF Amp

Radio frequency signals from the antenna switch pass through the 2nd stage BPF (made up of D19, L16, L17, L19, L20, C198~C204 and C206~C210),
and are input to Q27 via C211. The unwanted bandwidth signals of the Radio frequency signal is eliminated in the 3rd stage BPF (made up of D20, L21, L22, L24, L25, C213~C218 and C220~C224). The signal that has passed through the BPF is input to the 1st Mixer Q1, is mixed with the 1st Lo, and is output as the 1st IF (21.7 MHz) signal.

1-3 IF Amp

The signal from Q1 is further filtered for unwanted bandwidth signals in the crystal filters FI1 and FI2. The signal amplified in the Q2 IF Amp is input to pin 16 of IC1. IC1 has a 2nd Local Oscillator, 2nd Mixer, a limiter and a Quadrature Detector inside it. The 21.25 MHz 2nd Lo included in the IC2 crystal oscillation buffer (pin 17) is input to IC1 pin 2 and mixed with the 1st IF, then a 450 kHz 2nd IF signal is output to pin 3. The components of the 450 kHz signal only are selected by the ceramic filter FI3, and re-input to pin 5, then after detection by the Quadrature Detector, is output as an AF signal from pin 9.In the Quadrature Detector, X1 and R14 are used as a Phase Delay and as an unadjusted detection circuit.

1-4 Squelch

The signal output from pin 9 and split at C52 has its amplitude adjusted by R16, and is input to the noise amp. The noise component only is amplified in the noise amp (made up of R18~R20, C27 and C28) inside the internal amp of IC1, and is output as DC voltage from the internal noise detection circuit. The noise detection output voltage is input to the LOGIC unit's IC1 A/D board, and then is compared with the voltage from the VR-B unit to control the squelch.

1-5 AF Amp

The signal output from pin 9 is mixed with a frequency characteristic of -6 dB /oct from the de-emphasis circuit that is made up of R101 and C140. It passes through IC5 where the amplitude is adjusted by R1, and then is input to IC9. IC9 outputs about 5W at a 4-ohm load in the AF Power Amp. The audio signal output from IC9 is relayed through either the internal or external speaker.

2.Transmission Block

2-1 Mic Amp, IDC and Splatter Filter

The audio signal input to the mic is filtered at +6 dB/oct characteristics by the pre-emphasis circuit (made up of R121 and C159). It is amplified in IC7C, and for signals that require amplitude limitation, signal components over 3kHz are eliminated by the splatter filter (IC7D). Finally, the signal passes through R138, which adjusts for maximum modulation, and is added to the VCO input modulation and begins FM modulation.

2-2 Driver Amp

The output from the VCO passes through the RX/TX switchover type diode switch D6, and is amplified by Q10 and Q11. Q11 is the Driver Amp that amplifies the signal to the necessary level for input to IC3, and in the collector, supplies the voltage from the APC circuit that keeps the output constant by adjusting to the changes in the output voltage. Also, Q14 controls the Q15 base voltage and Q16 comparative voltage respectively by the TMUT signal from the CPU. And while preventing transmission of unwanted waves at TX startup, also prevents transmission in the case the PLL becomes unlocked.

2-3 RF Power Amp

IC3 is a power module that generates about 35W of output from a 300mW input, and is controlled by the output of pin 2.

2-4 APC

The IC3 output voltage that is made by both L12 terminals is detected in D8 and D9, and input to Q15. Q15 output changes the Q12 collector’s voltage to maintain a stable voltage output.

3.VCO, PLL Block

3-1 VCO

When transmitting, the varactor diodes D3 and D5, or L5, C52 and C53 decide the oscillating frequency, and that is changed to FM modulation by making D2 into an opposite bias state.

When receiving, D2 is in an ON condition and passes through C52, and the oscillated frequency shifts to low to make an AC like ground. After oscillation at Q5 and Q6, the signal passes through the buffer amp Q7 and Q9 and is output.

3-2 PLL

IC2 is a two system dual PLL IC that contains a prescaler, programmable counter, divider phase detector and charge pump. The reference frequency of 21.25 MHz is oscillated from X2. When transmitting, the PLL loop is made from the loop filter and charge pump that comes from R29~R31 and C41~C42.

4.Power Circuit Block

The 13.8V input from the power terminal passes through the VR-A unit's R1 switch as an HV line, and is re-applied as an HVS line to the MAIN unit. When 13.8V is put to the HVS line, it is converted to 5V at the three terminal regulator IC8. Q24 and Q25 controlled by the SEND signal from the CPU, controls the transmit part 5V (T5), and Q22 and Q23 controlled by the RCV signal from the CPU, controls the receive part 5V (R5).

5.WX Alert Decoder Block

The AF signal output from IC1 is input to the CPU (Logic unit IC1) A/D port via the LPF Q28, and the 1050 Hz signal is detected by decode software.

6.DSC Decoder Block

The AF signal output from IC1 is input to the FSK decoder at pin 2 in IC6. The decode is output from pin 7 and input to the CPU (Logic unit IC1).

LOGIC unit

1. CPU

IC1 is an 8-bit single chip microcomputer, and it contains the LCD driver, Serial I/O, timer, A/D converter, programmable I/O, ROM and RAM.

2. System Clock Oscillating Circuit

X1 is IC1's system clock (9.830 MHz).

3. Reset Circuit

IC6 is a special reset IC, and it outputs a low pulse to the CPU reset terminal when the power is turned ON.

4. ICF3/HM-127 Communication Interface Circuit

IC5 switches over the ICF3/HM-127 line. When communicating with the HM-127, IC5's 2 and 6 pins become "H", and perform data communication depending on the RRXD and RTXD lines. When communication with the ICF3 format,
IC5's 2 and 6pins become "L", and it becomes a transceiver (made up of Q6, Q9 and D2) that performs data communication between the CPU and external apparatus.

5. Low Battery Detection

The power voltage divided at R74 and R75 is monitored in IC1.

6. Dimmer Circuit

Each LED's (DS3~DS8) brightness is controlled in four stages by the dimmer circuit that is made up of Q2~Q4 and the CPU board.

7. DCS Encode

The DSC FSK signal made in the CPU is converted to an analog signal in the rider type A/D converter that is made up of R55~R73 and Q8,