IC-M1V CIRCUIT DESCRIPTION

1-1 RECEIVER CIRCUITS

1-1-1 ANTENNA SWITCHING CIRCUIT (RF UNIT)

The antenna switching circuit functions as a low-pass filter while receiving and as resonator circuit while transmitting. The circuit does not allow transmit signals to enter receiver circuits.

Received signals from the antenna connector pass through the low-pass fileter (L15–L17, C72–C77), and then the antenna switching circuit (D9, D11, D12).
The filtered signals are then applied to the RF amplifier (Q13).

1-1-2 RF AND 1ST MIXER CIRCUITS (RF UNIT)

The 1st mixer circuit converts the received signals to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only the desired frequency will be passed through a pair of crystal filters at the next stage of the 1st mixer.

The signals from the antenna switching circuit are passed through the tunable bandpass filter (D13, D14) and amplified at the RF amplifier (Q13). The amplified signals are passed through another tunable bandpass fileter (D15–D18), and then applied to the 1st mixer circuit (Q14).

The filtered signals are mixed at the 1st mixer (Q3) with a 1st LO signal coming from the PLL circuit to produce a 21.7 MHz 1st IF signal. The 1st IF signal is passed through a pair of crystal filters (FI1,FI2) and is then amplified at the IF amplifier (Q15).

1-1-3 2ND IF AND DEMODULATOR CIRCUITS (MAIN AND RF UNITS)

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double convertion superheterodyne system (which converts receive signal twice) improves the image rejection and obtain stable receiver gain.

The 1st IF signal is applied to a 2nd mixer section of the FM IF IC (MAIN unit; IC2, pin 16). The signal is then mixed with a 2nd LO signal for conversion to a 450 kHz 2nd IF signal.

IC1 contains the 2nd mixer, limiter amplifier, quadrature detector and active filter circuits. A 21.25 MHz 2nd LO signal is produced at the PLL circuit by dividing it's reference frequency.

The 2nd IF signal from the 2nd mixer (MAIN unit; IC1, pin 3) passes through a ceramic filter (MAIN unit; FI1 and FI2) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier (MAIN unit; IC1, pin 5) and applied to the quadrature detector (MAIN unit; IC1, pin 10 and 11) to demodulate the 2nd IF signal into AF signals.

1-1-4 AF CIRCUIT (MAIN UNIT)

AF signals from the FM IF IC (IC1, pin 9) are fed to the optional voice scrambler unit to demodulate scrambled audio or are bypassed around the unit via the analog switch (IC5).

The AF signals (detected signals) are passed through the analog switch (IC5, pin 8) and are then applied to the active low-pass filter (IC4, pin 9 and 10).

The filtered AF signals are passed through the [VOL] control (VR unit; R1) and then another analog switch (IC3, Q3). The passed signals are applied to the AF power amplifier (IC2).

1-1-5 SQUELCH CIRCUIT (MAIN UNIT)

• NOISE SQUELCH

The noise squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

A portion of the AF signals from the FM IF IC (IC1, pin 9) are applied to the active filter section (IC1, pin 8). The active filter section amplifies and filters noise components. The filtered signals are applied to the noise detector section and output from IC1 (pin 12) as the "SD" signal.

The "SD" signal from IC2 (pin 12) is applied to the CPU (IC9, pin 98) to analyze the noise condition, and then outputs the "BEEP" signal from the CPU (IC9, pin 78) to low-pass filter (IC4, pin 10).
The filtered signal is passed through the analog switch, and then applied to the AF amplifier (IC2). The amplified AF signal is output to the internal speaker or the external speaker jack.

• TONE SQUELCH

The tone squelch circuit detects AF signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the AF signals from the FM IF IC (IC1, pin 9) passes through the low-pass filter (IC4) via the analog swtich (IC5) to remove AF (voice) signals and is applied to the CTCSS decoder inside the CPU (MAIN unit; IC9, pin 97) via the "TONE" line to control the AF mute switch.

1-2 TRANSMITTER CIRCUITS

1-2-1 MICROPHONE AMPLIFIER CIRCUIT (MAIN UNIT)

The microphone amplifier circuit amplifies audio signals with +6 dB/octave pre-emphasis characteristics from the micrphone to a level needed for the modulation circuit.

The AF signals from the microphone are passed through the pre-emphasis circuit (R31, C36) and are then applied to the microphone amplifier (IC4, pin 13). The amplified AF signals are applied to the optional voice scrambler unit to scramble the audio via the "MICOUT" signal, or are bypassed around the unit via an analog switch (IC5, pin 4).

The amplified AF signals are amplified again at the limiter-amplifier (IC4, pin 2) and then applied to the low-pass filter (IC4, pin 6). The filtered audio is applied to the RF unit as the "MOD" signal.

1-2-2 MODULATION CIRCUIT (RF UNIT)

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals.

The audio signals (MOD) change the reactance of D4 to modulate an oscillated signal at the transmitter VCO (Q4, Q5). The oscillated signal is amplified at the buffer-amplifiers (Q6, Q8).

1-2-3 DRIVE/POWER AMPLIFIER CIRCUITS (RF UNIT)

The signal from the VCO circuit passes through the transmit/receive switching circuit (D7, D8) and is applied to the buffer-amplifier (Q9). The amplified signal is amplified by the pre-driver (Q10) and the power amplifier (Q11) to obtain 5W of RF power (at 7.4 V). The amplified signal passes through the antenna switching circuit (D9), and low-pass filter (C72–C77, L15–L17) and is then applied to the antenna connector.

The bias current of the power amplifier (Q11) is controlled by the APC circuit to stabilize the output power.

1-2-4 APC CIRCUIT (RF AND MAIN UNITS)

The APC circuit provides stable output power from the power amplifier even when the input voltage or temperature changes, and, selects HIGH, LOW or EXTRA LOW output power. The APC circuit consists of an APC sensor and APC control circuits.

• APC SENSOR CIRCUIT (RF UNIT)

The APC sensor circuit (D10, C80, C81, R53, R54) detects the transmit output power level and converts it to DC voltage as an "TXDET" signal. The detected signal is applied to the APC control circuit on the MAIN unit.

• APC CONTROL CIRCUIT (MAIN UNIT)

The "TXDET" signal from the APC sensor circuit is applied to the CPU (IC9, pin 96) to control the input voltage of the RF power amplifier IC (RF unit; IC1, pin 3). When the output power changes, the CPU (IC9) controls the "POWCON" line to stabilize the output power via the D/A converter (IC2).

IC3 is controlled by the CPU (IC9) to select HIGH, LOW or EXTRA LOW output power.

1-3 PLL CIRCUIT (RF UNIT)

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL circuit contains a VCO (Q4, Q5, D4, D6). The oscillated signal is amplified at the buffer-amplifier (Q7) and then applied to the PLL IC (IC1, pin 2).

The PLL IC contains two prescalers, programmable counters, programmable dividers, phase selectors and charge pumps, etc. The entered signal is divided at one of the prescaler and programmable counter sections by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency.

If the oscillated signal drifts, the phase of its frequency changes from the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

A portion of the VCO signal is amplified at the buffer-amplifiers (Q6, Q8) and is then applied to the receive 1st mixer (Q14) or transmit driver via the TX/RX switching diode (D7, D8).

The lock voltage is also used for the receiver tunable bandpass filter to match the filter's center frequency to the desired receive frequency. The lock voltage is amplified at the buffer-amplifier (Q1) and then applied to the CPU (MAIN unit; IC9, pin 93).

The amplified signal is controlled by the CPU (MAIN unit; IC9), and is then applied to bandpass filters (D13, D14, and D15–D18) as "T1", "T2", "T3", "T4" signals via the D/A converter (IC2).