CIRCUIT DESCRIPTION

1-1 RECEIVER CIRCUITS

1-1-1 ANTENNA SWITCHING CIRCUIT

Received signals are passed through the low-pass filter (L1-L3, C3-C6, C7). The filtered signals are applied to the antenna switching circuit (D406, D8).

The antenna switching circuit functions as a low-pass filter while receiving. However, its impedance becomes very high while D406 and D8 are turned ON. Thus transmit signals are blocked from entering the receiver circuits. The antenna switching circuit employs a diode switching system. The passed signals are then applied to the RF amplifier circuit.

1-1-2 RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit are amplified at the RF amplifier (Q12) after passing through the tuneable bandpass filter (D10, L17, C83, C85, C86). The amplified signals are applied to the 1st mixer circuit (Q13) after out-of-band signals are suppressed at the tuneable bandpass filter (D401, L18, C405, C406, C89, D11, L402, C91, C92, D12, L19, C96, C97, C94).

Varactor diodes are employed at the bandpass filters that track the filters and are controlled by the CPU (IC17) via the expander IC (IC10) using T1-T4 signals. These diodes tune the center frequency of an RF passband for wide bandwidth receiving and good image response rejection.

1-1-3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only the desired frequency will be passed through a crystal filter at the next stage of the 1st mixer.

The signals from the RF circuit are mixed at the 1st mixer (Q13) with a 1st LO signal coming from the VCO circuit to produce a 47.25 MHz 1st IF signal.

The 1st IF signal is applied to a pair of crystal filters (FI1) to suppress out-of-band signals. The filtered 1st IF signal is applied to the IF amplifier (Q400), then applied to the 2nd mixer circuit (IC2, pin 16).

1-1-4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double conversion superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

The 1st IF signal from the IF amplifier is applied to the 2nd mixer section of the FM IF IC (IC2, pin 16), and is mixed with the 2nd LO signal to be converted to a 450 kHz 2nd IF signal.

The FM IF IC contains the 2nd mixer, limiter amplifier, quadrature detector and active filter circuits. A 2nd LO signal (46.8 MHz) is produced at the PLL circuit by dividing It's reference frequency.

The 2nd IF signal from the 2nd mixer (IC2, pin 3) passes through a ceramic filters (FI2 and FI3) during narrow channel spacing selection or passes through FI2(bypassing FI3) only during wide channel spacing selection. It is then amplified at the limiter amplifier section (IC2, pin 5) and applied to the quadrature detector section (IC2, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

1-1-5 AF CIRCUIT

AF signals from the FM IF IC (IC2 pin 9) are applied to the mute switch (IC4, pin 1) via the AF filter circuit

(IC3b, pins 6, 7). The output signals from pin 11 are applied to the AF power amplifier (IC5, pin 4) after being passed through the [VOL] control (VR board, R1).

The applied AF signals are amplified at the AF power amplifier circuit (IC5, pin 4) to obtain the specified audio level. The amplified AF signals, output from pin 10, are applied to the internal speaker (SP1) via the [SP] jack when no plug is connected to the jack.

1-1-6 SQUELCH CIRCUIT

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch switches the AF mute switch.

A portion of the AF signals from the FM IF IC (IC2, pin 9) are applied to the active filter section (IC2, pin 8) where noise components are amplified and detected with an internal noise detector. The squelch level adjustment pot (R92) is connected in parallel to the active filter input (pin 8) to control the input noise level.

The active filter section amplifies noise components. The filtered signals are rectified at the noise detector section and converted into "NOIS"(pulse type) signals at the noise comparator section. The "NOIS" signal is applied to the CPU (IC17, pin 32).

The CPU detects the receiving signal strength from the number of the pulses, and outputs an "RM" signal from pin 84. This signal controls the mute switch (IC4) to cut the AF signal line.

1-2 TRANSMITTER CIRCUITS

1-2-1 MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit amplifies audio signals with +6 dB/octave pre-emphasis characteristics from the microphone to a level needed for the modulation circuit.

The AF signals from the microphone are applied to the high-pass filter circuit (IC25,pIn 3) and microphone amplifier circuit (IC3c, pin 10). The amplified AF signals are passed through the low-pass filter circuit (IC3d, pins 13, 14) via the mute switch (IC4, pins 2-4). The filtered AF signals are applied to the modulator circuit after being passed through the mute switch (IC4, pins 8-10) and the deviation adjustment pot (R119).

1-2-2 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signal.

The audio signals change the reactance of a diode (D404) to modulate an oscillated signal at the VCO circuit (Q7). The oscillated signal is amplified at the buffer-amplifiers (Q4, Q6), then applied to the T/R switching circuit (D3, D4).

1-2-3 DRIVE/POWER AMPLIFIER CIRCUITS

The signal from the VCO circuit passes through the T/R switching circuit (D3) and is amplified at the buffer(s) (Q3, Q403), drive (Q2) and power amplifier (Q1) to obtain 4 W of RF power (at 9.6 V DC). The amplified signal passes through the antenna switching circuit (D1), and low-pass filter and is then applied to the antenna connector.

1-2-4 CURRENT DETECTOR CIRCUIT

The current detector circuit (Q9, Q28) detects the total driving current of the drive and the power amplifiers, using the current sensor (R161). The differential amplifier (Q9) detects the voltage difference of

the current sensor input and output voltages, then and the CPU (IC17, pin 41).

1-2-5 POWER DETECTOR CIRCUIT

The power detector circuit (D2) detects the transmit power output level and converts it to DC voltage. The detected signal is applied to the APC circuit.

1-2-6 APC CIRCUIT

The APC circuit (IC19, Q37) protects the drive and the power amplifiers from excessive current drive, and selects HIGH or LOW output power.
The power detector circuit (D2) is applied to the differential amplifier (IC19, pin 3), and the "T4" signal from the expander (IC10, pin 14), controlled by the CPU (IC17), is applied to the other input for reference.
The bias current of the drive (Q2) and the power amplifier (Q1) is controlled by the APC circuit.

When the driving current is increased, input voltage of the differential amplifier (pin 2) will be increased. In such cases, the differential amplifier output voltage (pin 1) is decreased to reduce the driving current.

1-3 PLL CIRCUIT

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL circuit contains the VCO circuit (Q7, Q8). The oscillated signal is amplified at the buffer-amplifiers (Q5, Q6) and then applied to the PLL IC (IC1, pin 5).

The PLL IC description, featuring fractional-N division with selectable modulo 5 or 8
implemented in the main synthesizer to allow the phase detector comparison frequency to
be five or eight times the channel spacing.
this feature reduces the overall division ratio yielding a lower noise floor and faster
channel switching. The phase detector comparison frequency up to 5MHz.
A triple modulus prescaler (divide by 64/65/72) Is Integrated on chip with a maximum Input
Frequency of 1.0 G Hz.
The PLL IC contains a prescaler, programmable counter, programmable divider, phase detector and charge pump, etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency.

If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

A portion of the VCO signal is amplified at the buffer-amplifier (Q4) and is then applied to the receive 1st mixer or transmit buffer-amplifier circuit via the T/R switching diode (D3, D4).