4－1－1 ANTENNA SWITCHING CIRCUIT

The antenna switching circuit functions as a low-pass filter while receiving and a resonator circuit while transmitting.
The circuit does not allow transmit signals to enter receiver circuits.

Received signals enter the antenna connector (J1) and pass through the low-pass filter. The filtered signals are passed through the $\lambda/4$ type antenna switching circuit (D3-D5) and apply the RF circuit.

4－1－2 RF AND 1ST MIXER CIRCUITS

The 1st mixer circuit converts the received signal to fixed frequency of the 1st IF signal with the PLL output frequency.By changing the PLL frequency,only the desired frequency will be passed through a pair of crystal filters at the next stage of the 1st mixer.

The signals from the antenna switching circuit are passed through the tunable bandpass filter (L7,L8) and amplified at the RF amplifier (Q2). The amplified signals are again passed through the tunable bandpass filter (L10,L11) and applied to the 1st mixer.

The filtered signals are mixed at the 1st mixer (Q3) with the 1st LO signal coming from the Rx VCO circuit to produce 1st IF signal. The 1st IF signal is passed through the matching circuit (L13, L14) and the pair of crystal filters (FI1). The filtered signal is amplified at the 1st IF amplifier (Q4) and applied to the 2nd IF circuit.

4－1－3 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double-conversion superheterodyne system improves the image rejection ratio and obtains stable receiver gain.

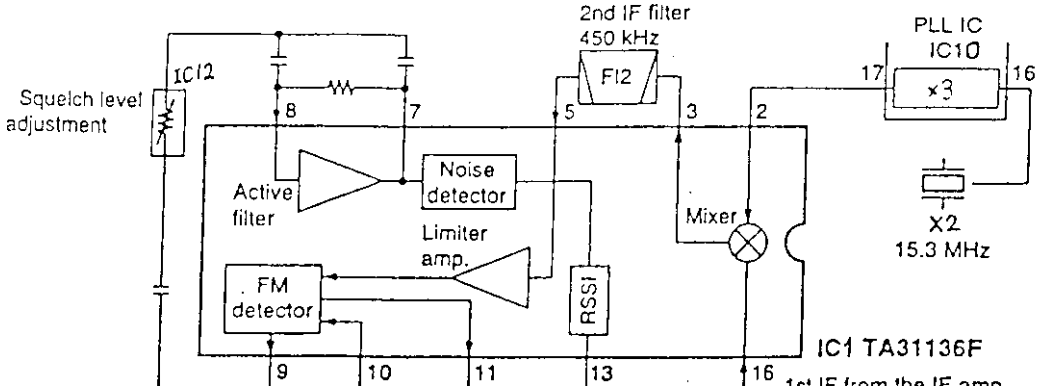
The 1st IF signal from Q4 is applied to the 2nd mixer section of IC1 (pin 16) and is then mixed with the 2nd LO signal for conversion to 450 kHz 2nd IF signal.

IC1 contains the 2nd mixer, 2nd local oscillator, limiter amplifier,quadrature detector and audio amplifier.A 2nd LO signal(45.9MHz) is produced at the PLL circuit by dividing it's reference frequency.

2nd IF signal from the 2nd mixer (IC1 pin 3) passes through the ceramic filter to suppress unwanted heterodyned frequency signals. It is then amplified at the limiter amplifier section (IC1 pin 5) and applied to the quadrature detector section (IC1 pins 7, 8 and X1) to demodulate the 2nd IF signal into AF signals.
The ceramic filter FI2 and FI3 switched by D12,D13,Q7 NWC signal.
The Q5 signal switched to IC1 input signal for switching wide band width and narrow band width.

The AF signals are output from IC1 (pin 9) and are then applied to the AF circuit.

• 2nd IF AND DEMODULATOR CIRCUITS



4－1－4 AF CIRCUIT

AF signals from IC1 (pin 9) are amplified at the AF amplifier (IC7) and are then applied to IC6. IC 6C/D are high-pass filters whose characteristics are controlled by the "AFHPF" line. When "AFHPF" is "High," the cut off frequency is shifted higher to remove CTCSS or DTCS signals.

The filtered signals from IC6 are applied to the electronic volume controller (IC12) via the AF mute switch (IC11) and are then passed through the deemphasis circuit (IC-4A) with frequency characteristics of -6 dB/octave,

Output signals from IC4 (pin 1) are applied to the AF power amplifier (IC9) to drive the speaker.

4－1－5 RECEIVE MUTE CIRCUITS

· NOISE SQUELCH

A squelch circuit cuts out AF signals when no RF signal is received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

The "NOIS" signal from IC1 is applied to the CPU. Then the CPU analyzes the noise condition and controls the "RMUT" and "AFON" ports to cut off the AF signal using AF switches (Q32, Q41).

· CTCSS AND DTCS

A portion of the AF signals from the AF amplifier (IC7) pass through the low-pass filters(Front unit) and are then amplified at the tone amplifier (Front Q5). The signals are applied to the CTCSS decoder inside the CPU to control the "RMUT" and "AFON" ports.

When the DTCS system is in use, the amplified signals are converted into digital signals, then applied to the DTCS decoder inside the CPU .

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit amplifies the audio signals with +6 dB/octave pre-emphasis characte ristics from the microphone to a level needed for the modulation circuit.

AF signals (MIC) from the FRONT unit via J3 (pin 39) are applied to the amplifier (IC8). While tran smitting, the MMUT signal from the IC13 is "High" and the AF signals pass to the microphone amplifie r circuit.

The AF signals from FRONT are applied to the microphone amplifier IC (IC8B) via the preamplifier . The amplified signals are applied to the limiter amplifier in IC8A.

The IC7A input signal changed by Q35 transistor for wide or narrow switch
Selected wide band width when Q35 NWC signal is L-level.

The entered signals (IC8A) are pre-emphasized with +6 dB/octave at a limiter amplifier, then passed through a splutter filter. The output signals from IC7A pass through the level controller (IC12) and are then applied to the modulation circuit (D21).

4－2－2 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone AF signals.

The AF signals from IC11 change the reactance of D21 to modulate the oscillated signal at the Tx VCO circuit (Q25). The modulated signal is amplified at the buffer amplifiers (Q28,Q30) and is then applied to the drive amplifier circuit.

The CTCSS/DTCS signals from FRONT are amplified at IC6B, and are applied to the reference oscillator circuit (X2) to modulate the oscillated signal.

4－2－3 DRIVE/POWER AMPLIFIER CIRCUITS

The signal from the buffer amplifier (Q30) is passed through the Tx/Rx switching circuit (D18,D19), and amplified by the driver (Q19-Q21) and the power module (IC5) to obtain 35 W of RF power.

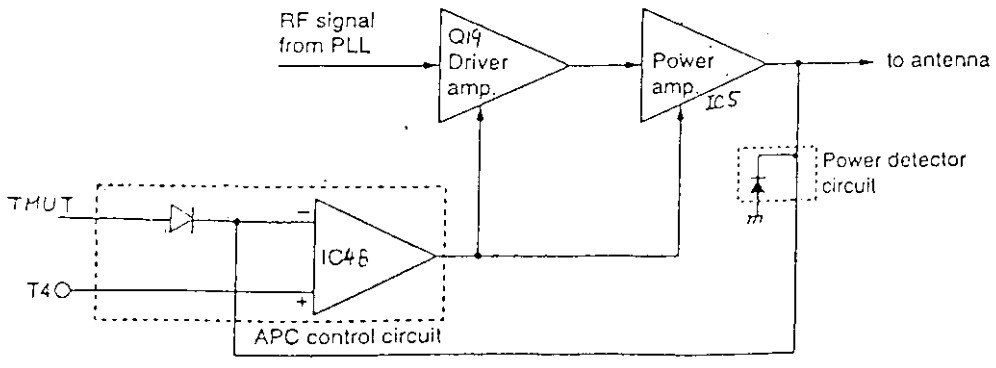
The amplified signal is passed through the antenna switching circuit (D3), low-pass filter and APC detector, and is then applied to the antenna connector.

4－2－4 APC CIRCUIT

The APC circuit protects the power module (IC5) from a mismatched output load and stabilizes the output power.

The APC detectorcircuit detects forward signals and reflection signals at D1 respectively. The combined voltage is at a minimum level when the antenna impedance is matched at 50Ω and is increased when it is mismatched.

The detected voltage is applied to the inverse amplifier (IC4B pin 6), and the power setting voltage (T4) is applied to the other input (IC4B pin 5). When antenna impedance is mismatched, the detected voltage exceeds the power setting voltage. Then the output voltage of the inverse amplifier (IC4B pin 7) controls the input current of the power module (IC5)



4-3 PLL CIRCUITS

4－3－1 PLL CIRCUIT

A PLL circuit provides stable oscillation of the transmit frequency and the receive 1st LO frequency. The PLL circuit consists of the PLL IC (IC10), charge pump and loop filter and employs a pulse swall ow counter.

Signals from the VCO through buffer amplifiers Q29 are prescaled in the PLL IC (IC10) based on the divided ratio (Ndata). The PLL IC detects the out-of-step phase using the reference frequenc y and outputs it from pin 8. The output signal is passed through the charge pump and loop filters and is then applied to the VCO circuit as the lock voltage.

The lock voltage is also used for the receiver tunable bandpass filters to match the filter's center frequency to the desired receive frequency. The lock voltage is amplified at the buffer amplifier (Q33) and is then applied to the bandpass filters (D7-D10).

4－3－2 VCO CIRCUIT

The VCO circuit contains a separate Rx VCO (Q23, D20, D34) and Tx VCO (Q25, D22, D33). The oscillated signal is amplified at the buffer amplifiers (Q28,Q30) and is then applied to the Tx/ Rx switching circuit (D18, D19). Then the Rx signal is applied to the 1st mixer (Q3) via and the Tx signal to the driver (Q21).

A portion of the signal from Q28 is amplified at the buffer amptifier(Q29) and is then feedback to the PLL IC (IC10 pin 2) as the comparison signal.