RECEIVER CIRCUITS

ANTENNA SWITCHING CIRCUIT

Received signals are passed through the low-pass filter (L1, L2, L3, C1, C2, C6, C7, C8).
The filtered signals are applied to the antenna switching circuit (D2, D5, D6, D41).
The antenna switching circuit functions as a low-pass filter while receiving.
However, its impedance becomes very high while D2, D5 D6 and D41 are turned ON. Thus transmit signals are blocked from entering the receiver circuits. The antenna switching circuit employs a diode switching system. The passed signals are then applied to the RF amplifier circuit.

RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.
The signals from the antenna switching circuit are amplified at the RF amplifier (Q2) after passing through the tunable band-pass filter of 2 steps (D8, L7, D4, L8). The amplified signals are applied to the 1st mixer circuit (Q3) after out-of-band signals are suppressed at the tunable band-pass filter of 2 steps (D9, L9, D10, L11).
Varactor diodes are employed at the band-pass filters that track the filters and are controlled by the CPU (Front IC1) via the D/A IC (IC6) using T1-T2 signals. These diodes tune the center frequency of an RF pass-band for wide bandwidth receiving and good image response rejection.

1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with a PLL output frequency. By changing the PLL frequency, only the desired frequency will be passed through a crystal filter at the next stage of the 1st mixer.
The signals from the RF circuit are mixed at the 1st mixer (Q3) with a 1st LO signal coming from the VCO circuit to produce a 46.35 MHz 1st IF signal.
The 1st IF signal is applied to crystal filter (FI1) to suppress out-of-band signals. The filtered 1st IF signal is applied to the IF amplifier (Q4), then applied to the 2nd mixer circuit (IC1, pin 16).

2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double conversion superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain.
The 1st IF signal from the IF amplifier is applied to the 2nd mixer section of the FM IF IC (IC1, pin 16), and is mixed with the 2nd LO signal to be converted to a 450 kHz 2nd IF signal.
The FM IF IC contains the 2nd mixer, limiter amplifier, quadrature detector and active filter circuits. A 2nd LO signal (45.9 MHz) is produced at the PLL circuit by three times reference frequency. The 2nd IF signal from the 2nd mixer (IC1, pin 3) passes through a ceramic filter (FI2) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier (IC1, pin 5) and applied to the quadrature detector (IC1, pins 10, 11) to demodulate the 2nd IF signal into AF signals.

AF CIRCUIT

AF signals from the FM IF IC (IC1 pin 9) are applied to the AF filter circuit (IC5). The output signals from AF filter circuit are applied to the AF amplifier (IC15) after being passed through the D/A IC (IC6) control CPU (Front IC1).

The applied AF signals are amplified at the AF power amplifier circuit (IC8, pin 1) to obtain the specified audio level. The amplified AF signals, output from pin 4, are applied to the internal speaker when no plug is connected to the external speaker jack.

SQUELCH CIRCUIT

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch switches the AF mute switch.

A portion of the AF signals from the FM IF IC (IC1, pin9) are applied to the active filter section (IC1, pin 8) where noise components are amplified and detected with an internal noise detector. The squelch level adjustment pot (IC6, pin 1) is connected in parallel to the active filter input (pin 8) to control the input noise level.

The active filter section amplifies noise components. The filtered signals are rectified at the noise detector section and converted into "NOIS" (pulse type) signals at the noise comparator section. The "NOIS" signal is applied to the CPU (Front IC1,pin 53).

The CPU detects the receiving signal strength from the number of the pulses, and outputs an "AFON" signal from CPU (Front IC1) pin43. And CPU (Front IC1) controls the mute switch (Q36) to cut the AF signal line.

TRANSMITTER CIRCUITS

MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit (Front IC5) amplifies audio signals with +6 dB/octave pre-emphasis.

MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signal.

The audio signals change the reactance of a diode (D18) to modulate an oscillated signal at the VCO circuit (Q13). The oscillated signal is amplified at the buffer-amplifiers (Q11, Q10), then applied to the T/R switching circuit (D14, D15).

DRIVE/POWER AMPLIFIER CIRCUITS

The signal from the VCO circuit passes through the T/R switching circuit (D14,D15) and is amplified at the drive (Q8) and power amplifier (IC3) to obtain 25 W of RF power (at 13.2 V DC). The amplified signal passes through the antenna switching circuit (D2), and low-pass filter and is then applied to the antenna connector.

Power control port (VCC1) of power amplifier (IC3) is controlled by the APC circuit.

POWER DETECTOR CIRCUIT

The power detector circuit (D1,11) detects the transmit power output level and converts it to DC voltage. The detected signal is applied to the APC circuit.

APC CIRCUIT

The signal output from the power detector circuit (D1,11) is applied to the operational amplifier (IC2, pin 3), and the "T2" signal from the D/A (IC6, pin 22), controlled by the CPU (Front IC1), is applied to the other input for reference.

PLL CIRCUIT

A PLL circuit employs fractional-N synthesizer system and provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider.

The PLL circuit contains the VCO circuit (Q13, Q14). The oscillated signal is amplified at the buffer-amplifiers (Q11, Q12) and then applied to the PLL IC (IC4, pin 8).

The PLL IC contains a prescaler, programmable counter, programmable divider, phase detector and charge pump, etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency.

If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

A portion of the VCO signal is amplified at the buffer-amplifier (Q11) and is then applied to the receive 1st mixer or transmit buffer-amplifier circuit via the T/R switching diode (D14, D15).