IC-A23/A5 Circuit Description

1. RF Board

(PLL/VCO)

VCO consists of Q31,Q32 and D24, and Q34 and D25 are oscillator shift circuit for receive mode. The signals form VCO are amplified by Q29 and Q30, and a fed to pin 8 of IC-3.

IC-3 is PLL IC, and the signals from Q30 are divided by 1/N data, which set by the serial data from CPU, and then are fed to phase detector.

X2 is reference crystal oscillator, and the signals from oscillator are divided by reference programable counter, and then are out from IC-3 as phase pulse

The signals from IC-3 are pass through loop filter, and are fed to D24 on VCO for controlling oscillating frequency signals.

2. Receiver

(RF)

The incoming signals from antenna are pass through low pass filer, consists of L1-L3 and C3-C7, and are fed to antenna switching circuit

The antenna switching circuit uses quarter wave diode switching circuit, and in receive mode, D1, D8 and D9 are turned off.

The incoming signals from the antenna switching circuit are pass through the band pass filter, which consists of D13, C58, C60 and L18, and are fed to Q11.

The amplified signals from Q11 are filtered by the band pass filter, which consists of D14-D16, C70-C79, and are fed to Q12.

Q12 is 1st mixer and mixes the incoming receive signals with 1st LO signals, and puts out 30.05MHz, 1st IF signals.

(1st IF)

The incoming signals from 1st mixer is filtered by FI-1 (Crystal filter), and are fed to Q13 and IC-1.

(2nd IF)

IC-1 is 2nd IF IC, and the IC contains 2nd LO oscillator, 2nd mixer, IF amplifier, FM detector and S-meter circuit.

The incoming 1st IF signals (30.5MHz) from Q13 are fed to the IC-1 and are mixed with 2nd LO signals (29.6MHz) from PLL reference crystal for generating 2nd IF signals.

The incoming 2nd IF signals (450MHz) are filtered by FI-2 (Ceramic filter), and are fed to AM or FM demodulating circuit through Q15.
For FM mode, the signals from Q15 are amplified by IC-1 and pin 9 of IC-1 puts out AF signals after de-modulated by FM detector.
For AM mode, the signals from Q15 are amplified by Q16 nad Q17, and then are de-modulated by Q18.

(AF)
The de-modulated incoming signals are path through IC2 (Analog switch), amplified by amplifier (IC-510), filtered by low pass filter (IC-510), amplified by IC-14, volume controlled by IC-505, amplified by IC-6 and the fed to speaker

(SQL)
The s-meter signals from pin 12 of IC-1 are amplified by IC-13, and fed to pin3 of CPU.
The SQL control signals from CPU are fed to Q35 and Q36, and controls IC-6

3. Transmitter

(TX)
The transmitting signals from VCO are amplified by Q30, Q27 and Q28, and are fed to AM modulator circuit (D5) through D6.
The modulated transmitting signals from D5 are amplified by Q6,Q4,Q3 and Q2, and are fed to antenna through antenna switching circuit (D1) and high and low pass filer.

(ALC)
ALC voltage signals are detected by D2 and D3, and are amplified by Q5, and then fed to D4 for controlling transmit output power.

(Transmit Audio)
The incoming microphone audio are filtered by low pass filter (IC-510) and are fed to the D5 as transmit modulating signals

4. Power supply

(Internal/External switching circuit)
When the radio is used with battery pack, Q24 is turned on.
When external DC is apply to the radio, Q24 is turned off
D19 and D22 is reverse voltage protector

(Battery Pack Charging Circuit)
The charging circuit consists of D20,D21 Q22 and Q23.

5. Logic

(Reset)
IC-2 detect DC power voltage, and sends reset signals to pin33 of CPU when the radio is turned on

(Clock Oscillator)
X1 on CPU generates CPU clock signals

(Lamp)
Pin7 of IC-8 controls LCD and keyboard lighting on the front panel through Q1, Q2, Q8

(Clone)
Clone is done by pin 19 and 20 on CPU Q5 and D11

(MIC AMP)
When PLL switch is repressed, incoming mic audio are amplified by IC-9, and fed to IC-15.

(PTT)
Q10 detects PLL controls, and sends the status signals to CPU

(DC regulator)
The radio is supplying 5V DC to IC-1 and IC-7 through IC-3.
When radio is on, pin54 on CPU controls Q6,Q4 and Q7, and supplying 5V DC to other circuit.

(VOR)
The frequencies are selected between 108MHz and 117.975MHz, pin4 on IC-8 becomes high level, and supplying DC power to VOR circuit through Q15.
Also the voltages from Q15 are divided by R75 and R76, and are fed topin3 of IC-12, and supplying biased voltage from pin1 to other op amp.
The VOR detected signals from RF board are fed to pin5 n IC-12 through VORDET line.
Amplified signals from pin7 on IC-12 are filtered by 9960Hz band pass filter and 30Hz

band pass filter

(30Hz Band Pass Filter)
This band pass filter consists of R83, R85-R88, C112-C113 and IC12, and filtered signals are converted the square wave signals by IC-14, and are fed to VORC line on CPU

(9960Hz Band Pass Filter)
This band pass filter consists of R79-R81, C108-C109 and IC-12, and filtered signals are 9960Hz reference signals, which modulated by 30Hz with 480Hz deviation.
Those reference signals are amplified by IC-11.
When pin1 of IC-11 is 0V, D16 is on, and C102 will be discharged. At same time pin7 of IC11 will be high.
When pin1 of IC-11 is 2V, C102 will be charged through C62, and pin7 of IC-11 will become low level to high level, and becomes PWM signals.
This PWM signals are filtered by LPF (R63, C114), pass through phase detector (IC-13, R66-R68, C115) and IC-14, and are fed to CPU as VORS signal line.

(OFF FLAG)
When Incoming signals are not VOR signals nor low level signals, pin7 of IC-12 becomes low level, and Q13 sends high level signals to CPU for turning on the VOR OFF FLAG

(Battery Pack protecting circuit)
When the temperature gets below 0 degrees C, R37 send signals to pin 5 of CPU, and cuts RF output power to half.