Circuit Description.

1. The MAIN Unit:

Reception

The input signal from the antenna connector passes through the low-pass filter (L2,L3, L48, C1~C6, C330~C331), and is applied to the antenna switching circuit.

The antenna switching circuit uses a λ/4 type diode switch that does not consume any electric current when receiving. When receiving, all of the diodes (D1~D3) are turned off and operate as a low-pass filter. The input signal passes through this low-pass filter (L4, L5, C7~C9, C362), and is applied to the RF amplifier circuit.

The input signal passes through the AGC interlocking RF attenuators (D38, Q73, L52, R295 which attenuate when there is excessive input), then pass through the band-pass filters (L8, L27, C10, C21, C164, C165) and tunable varactor bandpass filters (D6, D37, L9, L49, C23, C342, C405, C406), which suppress unwanted out-of-band signals. Then, the signal is applied to the RF amplifier (Q1).

The amplified signal passes through the tunable varactor bandpass filters (D7, D8, L10, L11, C28, C31, C407,C533), and is input into the first gate of the 1st-mixer circuit (Q2). The 1st Lo has been input into the second gate of (Q2), and mixes the received signal frequencies to a 38.85 MHz 1st IF signal.

The 1st IF suppresses unwanted out-of-band signals in either Wide Mode (FI1) or Narrow Mode (FI2), then is amplified in the IF amp (Q3) and applied to the IF IC (IC 40) pin 16. The IF IC contains the 2nd mixer. The applied signal from pin 16 is mixed with a tripled frequency from the PLL IC reference oscillator (X1 12.8 MHz) at (Q83, Q84), that is used for the 2nd Lo signal (38.4 MHz), for a conversion to a 450 kHz 2nd IF signal that is output from pin 3. That output signal passes through ceramic filters (Wide Mode=FI3, Narrow Mode=FI4) that suppress unwanted out-of-band signals, which after being amplified in the 2nd IF AMP (Q4~Q6), are applied to the AM detector section at (Q7).

Depending on the current flowing in (Q7), the (Q77) IF AGC AMP and the (Q78) RF AGC AMP are activated, and the gain is controlled.

The (Q4) output is also applied to the IF IC pin 5. The IF IC RSSI and (Q78) AGC AMP output is synthesized by the OP amplifier (IC11), and turned into a squelch signal.

The AF output detected in (Q7) passes through the low-pass filter (IC31), then through the (IC22) MOD/AF switch and, after being amplified in the AF AMP (IC42), passes through the RMUTE (IC6) where the AF level is adjusted by the electronic volume (IC13). It then passes through the mute SW (IC30), and is branched into speaker and ACC.

The speaker passes through the AF mute SW (IC28) and AF/MOD SW (IC48), then is applied to the buffer amplifier and the FET driver (IC47) pin 5, which drives the power MOS FET (Q92, Q93) and then is power amplified in the AF amplifier. That output passes through the SP SW (Q94) and is output from the SP jack (J7), but if no SP is connected to (J7), the (J7) plug-in switch switches to the internal SP, conducts level adjustment (R209,R445,R446) and is power amplified in the AF amplifier to drive the internal SP. The other ACC is power amplified in the AF AMP (IC37) to drive the ACC

speaker (headset etc.).
The bandpass filter conducts tracking with the varactor. The tuning voltage added to the varactor power amplifies (Q79) the PLL lock voltage at the high impedance input FET, so that it does not affect the PLL circuit. With these circuits, it is possible to obtain a good image ratio across wide bandwidths.

Transmission

The Lo produced in the VCO is amplified in the buffer amplifier (Q14, Q15), then passes through the Lo SW (D10, D11) and is power amplified to the necessary level in the PA in the YGR (Q42).

The amplified signal is power amplified in the PRE DRIVE (Q20, Q21) and POWER AMP (Q51), then passes through the APC detector circuit (D4, D5, L6, C12~C17) and ANT SW (D3), then the higher harmonics are attenuated in the LPF and applied to the ANT.

The APC compares the detector circuit's voltage and the APC set voltage (R150) in the differential amplifier (IC50), then with the (Q11, Q98) APC driver, controls the PRE DRIVE (Q20, Q21) amplification so that the APC set voltage and detector voltage are the same, which stabilizes the power output.

PLL

The PLL loop consists of the VCO and (IC2). The VCO output is applied to the buffer amplifier at (Q14, Q15), and becomes the Lo. The other output is amplified in the (Q12) AMP, and applied to the PLL IC. In the PLL IC, the reference oscillator (X1) oscillates at 12.8 MHz. This is divided into frequencies of 25kHz from the CPU data (front unit IC1), and this is phased with the same data from the CPU in the VCO of 25kHz divided frequencies. The lock voltage outputs only the difference of these from the charger pump. The lock voltage from (IC2) becomes DC in the (R61, R62, C59, C60) loop filter, and is output in the VCO LV line.

VCO

The VCO contains separate transmitting and receiving circuits. The transmitting circuit consists of the (Q44) oscillating circuit and the varactor diode (D64). The oscillating frequency is changed by the DC bias in the oscillating circuit's cathode (D64). The receiving circuit consists of the (Q59) oscillating circuit and the varactor diodes (D65). The oscillating frequency is changed by the DC bias in the oscillating circuit's cathode (D65).

The transmission output is applied to the buffer circuit (Q43), and becomes the VCO output. Transmission/reception VCO is operated by switching. That switching is conducted by matching the VCO power operation in (Q58).

Modulation Circuit

The microphone signal passes through the IN/EXIT SW (IC16), and after the mic sensitivity (R110) has been set, the gain is controlled in the ALC AMP (IC4), and then it passes through the MOD/AF (IC22) and splatter filter (IC19). After it passes through MOD/AF SW (IC48) and the modulation has been set in (R121), it is power amplified in the AF AMP (IC44) FET driver (IC47) and power MOS FET (Q92, Q93), and then is modulated in the transmission output stage and becomes output

modulation. (IC44, IC17, Q92, Q93 have the same use for reception.)

Power Circuit

In the power circuit, a switch breaker is used with the use of two power sources possible, DC 12V and DC 24V, that do not need to be switched over manually.

2. The Front Unit:

Reset Circuit (Front Unit)

With the reset IC (IC2), because the CPU (IC1) reset port (pin 9) voltage is slower than the power voltage, the CPU (IC1) can be reset when the power is turned on.

Clock Oscillation Circuit

The CPU clock oscillation circuit consists of pin 6 and pin 7 of the CPU and the crystal vibrator (X1).

Lamp Circuit

With the EXPAND (IC5) fourth and fifth outputs, the LCD brightness is controlled at (Q1, Q5~Q7), and that brightness can be adjusted to three levels.

CLONE Circuit

With the CLONE circuit which consists of (Q2, Q3, IC3), serial data can be input into pin 70 of the CPU, or output from pin 71. The circuit can read or write data with another radio unit or computer and memory etc.