CIRCUIT DESCRIPTION

1 RECEIVER CIRCUITS

1-1 RF SWITCHING CIRCUIT

(CTRL AND RF UNIT)

The RF switching circuit leads receive signals to band-pass filters from an antenna connector while receiving. However, the circuit leads the signal from the RF power amplifier to the antenna connector while transmitting.

RF signals from [ANT 1] or [ANT 2] pass through the antenna selector (RL3), transmit/receive switching relays (RLI,RL2, RL4), and low-pass filter (L27, L28, C63-C66, COOS), and are then applied to the RF unit via J2.

The signals from the CTRL unit either bypass or are applied to the 6 dB (RF unit, RL121, R152) and/or 12 dB (RF unit, RL122, R154) attenuators via the antenna selector. By selecting the attenuators, 0 (bypass), 6, 12 and 18 dB attenuations are obtained. The signals are then applied to the RF filters.

When the [RX ANT] is selected, the RF signals are passed through the low-pass filter (RF unit, L181) L182, C183-C187), then applied to the antenna selector (RF unit,RL101).

1-2 RF BANDPASS FILTER CIRCUIT (RF UNIT)

RF band-pass filters pass only the desired band signals and suppress any undesired band signals. The RF circuit has 11 band-pass filters and 1 low-pass filter.

(1) 0.03-1.6 MHz

The signals pass through the attenuator (R181, R182, R183), low-pass filter (L181-L183, C181-C185, and are then applied to the RF amplifiers (Q501,Q601).

(2) 1.6-60 MHz

The signals pass through the high-pass filter (L171-L174, C171-C174) to suppress excessively strong signals below 1.6 MHz. The filtered signals are applied to one of 11 band-pass filters as below, and then applied to or bypass the pre-amplifier circuit.

1-3 PRE-AMPLIFIER CIRCUITS (RF UNIT)

The IC-756 has 2 gain levels of pre-amplifier circuits. One has 10 dB gain over a wide band frequency range and the other one has 16 dB gain for the 21-28 MHz bands.

When the [PREAMP] switch is set to [PREI] or [PRE2], the signals are applied to the pre-amplifier 1 (Q441, Q442) or pre-amplifier 2 (lC451) circuit, respectively. Pre-amplified or bypassed signals are applied to the RF amplifier circuits.

1-4 RF AMPLIFIER AND 1st MIXER CIRCUITS (RF UNIT)

The 1st mixer circuit mixes the receive signals with the 1st Lo signal to convert the receive signal frequencies to a 69 MHz 1st IF signal. The IC-756 has two 1st mixer circuits for the dual-watch function.

The signals from the pre-amplifier circuit, or signals which bypass the pre-amplifiers, are divided at L501. Each signal is applied to a 30 MHz cut-out low-pass filter, RF amplifier (Q501, Q601) and then to a 1st mixer (Q611/Q612-Q614 or Q511/Q512-Q514).

Each 1st LO signal (69.0415-129.0115MHz) enters the RF unit from the PLL unit via J101 or J201.
The Lo signals are amplified at the Lo amplifier (Q561 or Q661), filtered by a low-pass filter, and then applied to each 1st mixer.

1-5 1st IF CIRCUIT (RF UNIT)

The 1st IF circuit filters and amplifies the 1st IF signal. The 1st IF signal combined at L201 is applied to an MCF (Monolithic Crystal Filter; FII8la) to suppress out-of-band signals.

The converted 1st IF signal level is adjusted at PIN attenuators (D532,D535, D531 or D632,D635, D631) controlled by the [BAL] controller for the dual-watch function. The signal is applied to the 1st IF amplifier (Q551 or Q651) and then combined at L653.

The combined signal passes through the MCF (FI711a) and is amplified at Q721. The amplified signal is filtered at the other MCF (FI711b) and then applied to the 2nd mixer

circuit.

1-6 2nd MIXER CIRCUS (RF UNIT)

The 2nd mixer circuit mixes the filtered 1st IF signal and 2nd Lo signal (60.00 MHz) for conversion to the 2nd IF.

The 1st IF signal from the MCF (FI711b) is converted into a 9 MHz 2nd IF signal at the 2nd mixer circuit .

The 2nd IF signal is applied to the MCF (MAIN unit, FI132) to suppress undesired signals such as the 2nd LO signal, and then applied to the noise blanker gate.

1-7 NOISE BLANKER CIRCUIT (MAIN UNIT)

The noise blanker circuit detects pulse-type noise, and turns OFF the signal line when the noise appears.

The 2nd IF signal from the MCF (FI132) is applied to the noise blanker gate (D112). A portion of the signal from FI132 is amplified at the noise amplifiers (Q271-Q273), then detected at the noise detector (D271) to convert the noise components to DC voltages.

The signal is then applied to the noise blanker switch (Q276,Q278). At the moment the detected voltage exceeds Q276's threshold level, Q278 outputs a blanking signal to close the noise blanker gate (D112). The T8V and PLL unlock signal are also applied to Q278, to control the noise blanker gate.

Some DC voltage from the noise detector circuit is fed back to the noise amplifier (Q271,Q272) via the DC amplifiers (Q273, Q275). The DC amplifiers function as an AGC circuit to reduce average noise. Therefore, the noise blanker function shuts off pulse-type noise only.

1-8 2nd IF CIRCUS (MAIN UNIT)

The 2nd IF circuit amplifies and filters the 2nd IF signal.

The 2nd IF signal from the noise blanker gate (D112) is amplified at the IF amplifier (Q271-Q273) and applied to a 2nd IF filter which is selected in the filter selection mode.

CIRCUIT DESCRIPTION

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When the [RX ANT] is selected, the RF signals are passed through the low-pass filter (RF unit, L181) L182, C183-C187), then applied to the antenna selector (RF unit,RL101).

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(2) 1.6-60 MHz

The signals pass through the high-pass filter (L171-L174, C171-C174) to suppress excessively strong signals below 1.6 MHz. The filtered signals are applied to one of 11 band-pass filters as below, and then applied to or bypass the pre-amplifier circuit.

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When the [PREAMP] switch is set to [PREI] or [PRE2], the signals are applied to the pre-amplifier 1 (Q441, Q442) or pre-amplifier 2 (lC451) circuit, respectively. Pre-amplified or bypassed signals are applied to the RF amplifier circuits.

1-4 RF AMPLIFIER AND 1st MIXER CIRCUITS (RF UNIT)

The 1st mixer circuit mixes the receive signals with the 1st Lo signal to convert the receive signal frequencies to a 69 MHz 1st IF signal. The IC-756 has two 1st mixer circuits for the dual-watch function.

The signals from the pre-amplifier circuit, or signals which bypass the pre-amplifiers, are divided at L501. Each signal is applied to a 30 MHz cut-out low-pass filter, RF amplifier (Q501, Q601) and then to a 1st mixer (Q611/Q612-Q614 or Q511/Q512-Q514).

Each 1st LO signal (69.0415-129.0115MHz) enters the RF unit from the PLL unit via J101 or J201.
The Lo signals are amplified at the Lo amplifier (Q561 or Q661), filtered by a low-pass filter, and then applied to each 1st mixer.

1-5 1st IF CIRCUIT (RF UNIT)

The 1st IF circuit filters and amplifies the 1st IF signal. The 1st IF signal combined at L201 is applied to an MCF (Monolithic Crystal Filter; FII8la) to suppress out-of-band signals.

The converted 1st IF signal level is adjusted at PIN attenuators (D532,D535, D531 or D632,D635, D631) controlled by the [BAL] controller for the dual-watch function. The signal is applied to the 1st IF amplifier (Q551 or Q651) and then combined at L653.

The combined signal passes through the MCF (FI711a) and is amplified at Q721. The amplified signal is filtered at the other MCF (FI711b) and then applied to the 2nd mixer

circuit.

1-6 2nd MIXER CIRCUS (RF UNIT)

The 2nd mixer circuit mixes the filtered 1st IF signal and 2nd Lo signal (60.00 MHz) for conversion to the 2nd IF.

The 1st IF signal from the MCF (FI711b) is converted into a 9 MHz 2nd IF signal at the 2nd mixer circuit .

The 2nd IF signal is applied to the MCF (MAIN unit, FI132) to suppress undesired signals such as the 2nd LO signal, and then applied to the noise blanker gate.

1-7 NOISE BLANKER CIRCUIT (MAIN UNIT)

The noise blanker circuit detects pulse-type noise, and turns OFF the signal line when the noise appears.

The 2nd IF signal from the MCF (FI132) is applied to the noise blanker gate (D112). A portion of the signal from FI132 is amplified at the noise amplifiers (Q271-Q273), then detected at the noise detector (D271) to convert the noise components to DC voltages.

The signal is then applied to the noise blanker switch (Q276,Q278). At the moment the detected voltage exceeds Q276's threshold level, Q278 outputs a blanking signal to close the noise blanker gate (D112). The T8V and PLL unlock signal are also applied to Q278, to control the noise blanker gate.

Some DC voltage from the noise detector circuit is fed back to the noise amplifier (Q271,Q272) via the DC amplifiers (Q273, Q275). The DC amplifiers function as an AGC circuit to reduce average noise. Therefore, the noise blanker function shuts off pulse-type noise only.

1-8 2nd IF CIRCUS (MAIN UNIT)

The 2nd IF circuit amplifies and filters the 2nd IF signal.

The 2nd IF signal from the noise blanker gate (D112) is amplified at the IF amplifier (Q271-Q273) and applied to a 2nd IF filter which is selected in the filter selection mode.

The filtered signal is amplified at the buffer-amplifier (Q274), then applied to the 3rd mixer circuit.

1-9 3rd MIXER AND 3rd IF CIRCUITS
(MAIN UNIT)

The 3rd mixer circuit mixes the 2nd IF signal and the 3rd LO signal to obtain the 3rd IF (455 kHz) signal.

The 2nd IF signal from the buffer-amplifier (Q274) is applied to the 3rd mixer circuit (IC151). The 3rd LO signal from the PLL unit is applied to the 3rd mixer (lC151). The mixed signal is output from pin 3, then applied to one of the 3rd IF filters.

The filtered signal is amplified at the IF amplifier (IC201b), then applied to the AM demodulated, the 4th mixer circuit or the FM demodulated circuit after being amplified at the other IF amplifier (IC-201b).

1-10 DSP RECEIVER CIRCUIT (DSP BOARD)

The DSP (Digital Signal Processors board enables digital noise reduction, digital PSN (Phase Shift Network) demode-lation, digital automatic notch and digital APF (Audio Peak Filter).

The IF signal then passed through the analog switch (lC2291). The switched signal is level shifted at IC2052 after being passed though the low-pass filter (lC2052, IC2351) then applied to the A/D convector (lC2351).

The converted signal is applied to the DSP ICs (IC2001) for demodulation, automatic notch, audio peak filter and noise reduction, etc. The output signal is applied to the D/A convector (lC2351,2371a) and converted into analog audio signals.

The converted audio signals are passed through the low-pass filter (lC2401), analog switch (lC2372, pins 3, 4) then applied to the MAIN unit after passed through the low-

pass filter (IC2471a).

1-11 TWIN PBT CIRCUS (RF AND MAIN UNITS)

The PBT (Pass-Band Tuning) circuit shifts the center frequency of IF signal to electronically narrow the pass-band width. The IC-756 has 2 PBT circuits.

The twin PBT circuit shifts the 2nd and 3rd IF within ±1.5 kHz. As a result, the 2nd and 3rd IF are shifted from the center frequencies of the 2nd and 3rd IF filters. This means 2nd or 3rd IF signals do not pass through the center of the 2nd or 3rd IF filter. Therefore, the overlap of the 2nd/3rd or 3rd/4th IF filter appears to be narrowed. Since the 3rd and 4th LO frequencies are also shifted the same value as the 2nd and 3rd IF shifts, frequencies are corrected at the detector.

In the IC-756, the 1st LO frequency is shifted to change the 2nd IF because a fixed 2nd LO frequency (60.00 MHz) is used. The 1st IF filter (RF unit, FI81) has a 15 kHz pass-band width and does not affect PBT operation.

1-12 AGC CIRCUIT (MAIN UNIT)

The AGC (Automatic Gain Control) circuit reduces IF amplifier gain to keep the audio output at a constant level.

The receive gain is determined by the voltage on the AGC line.
IC2461 supplies minus voltage to the AGC line and sets the receiver gain with the [RF/SQL] control.

The 3rd IF signal from the buffer-amplifier (IC2471b) is detected at the AGC detector and is then applied to the AGC amplifier (IC2461), -5 V is applied to the AGC amplifier's emitter to activate the AGC line using minus voltage.

When receiving strong signals, the detected voltage increases and the AGC voltage decreases via the AGC amplifier (IC2461). As the AGC voltage is used for the bias voltage of the IF amplifiers, IF amplifier gain is decreased.

When the strong signals disappear, the AGC line voltage is released by C228,C229 , R265 and R266 while in SSB, CW or RTTY mode. While in AM or FM mode, C243 or R267 is connected in parallel to obtain appropriate AGC characteristics, respectively.

1-13 SQUELCH CIRCUIT (MAIN UNIT)

The squelch circuit mutes audio output when the S-meter signal is lower than the [RF/SQL] setting level.

The S-meter signal is applied to the main CPU and is compared with the threshold level set by the [RF/SQL] control. The [RF/SQL] setting signal is applied to the main CPU via the A/D converter (SUB-LOGIC unit, IC501) and sub CPU (SUB-LOGIC unit, lC3). The com-pared signal is applied to the analog switch (lC507, pin 9) to open or close the squelch.

In addition, the noise squelch signal from the FM IF IC (FMNL) is applied to the main CPU in FM mode.
A portion of the AF signals from the FM IF IC (IC306, pin 9) are applied to the active filter section (pin 8) where noise components are amplified. The signals are rectified at the noise detector section and then output from pin 14. The resulting signal is applied to the main CPU via the FMNL signal line.

1-14 AF AMPLIFIER CIRCUIT (MAIN UNIT)

The AF amplifier amplifies the audio signals to a suitable driving level for the speaker.

The AF signals from the AF selector are amplified at the IC332 amplifier section and volume is controlled by the AFGV signal at the VCA section. The volume controlled AF signals are passed through the low-pass filter then applied to the AF power amplifier (lC332) via the AF mute switch (IC331).

The amplified audio signals are passed through the [PHONES] and [EXT SP] jacks then applied to the internal speaker when no plug is connected to the jacks.

The AF mute switch is controlled by the [AF] control via the sub and main CPUs.

2 TRANSMITTER CIRCUITS

2-1 MICROPHONE AMPLIFIER CIRCUIT (MAIN UNIT)

The microphone amplifier circuit amplifies microphone audio signals to a level needed for the DSP (PSN), FM and AM modulation circuits.

Audio signals from the [MIC] connector (pin 1) are amplified at the audio amplifier section in IC451, then applied to the VCA section via the analog switch (IC3002).
The gain controlled signal are applied to the DSP circuit after the tone level is adjusted at the tone control circuit (IC451), or applied to the FM IDC circuit (IC3005) after being pre-emphasized at IC451.

The VCA section in IC3002 controls microphone gain from the [MIC GAIN] control using the MIGV signal from the main CPU via the D/A converter (LOGIC board, IC809).

2-2 VOX CIRCUIT (MAIN UNIT)

The VOX (Voice-Operated-Transmission) circuit sets transmitting conditions according to voice input.

A portion of the amplified audio signals from the AF amplifier section in IC451 are again amplified at the AF amplifier section in IC362, gain controlled at the VCA section then applied to the main CPU after passing through the level comparator circuit as the VOXS signal.

The VOXV signal is applied to the VCA section in IC451 from the main CPU via the I/O expander (IC2003, pin 4) to adjust VOX actionable sensitivity. This is controlled by the VOX gain set in the VOX SET mode.

2-3 DSP TRANSMITTER CIRCUIT (DSP BOARD)

The microphone audio signals from the tone controller (MAIN unit, IC451) are applied to the buyer-amplifier via J401, pin 9. The amplified audio signals are applied to the low-pass filter (lC301) to limit the transmit pass-band width. The filtered signals are then applied to the analog switch (D212), then passed through the low-pass filter (lC419d, IC419a). The filtered signals are applied to the DSP ICs (lC425, IC429) via the A/D converter (lC408) after the level is shifted at lc419b.

By combining IC414b and IC415, the modulation level for SSB and AM modulation is adjusted.

A portion of the filtered signal from the low-pass filter (lC412) is passed through the analog switch (IC415, pins 1, 2, 15) then applied to the MAIN unit via J401, pin 5 for the monitor function.

The PSN modulated signals are applied to the D/A converter (lC409, IC419c) then passed through the low-pass filter (lC4ll) to produce the transmit IF signal. The IF signal is applied to the 4th mixer circuit (MAIN unit, IC201) via J401, pin 13.

2-4 FM MODULATOR CIRCUIT (MAIN UNIT)

The microphone audio signals from the VCA section in IC2211 are applied to the IDC circuit (lC301b) after passing through the pre-emphasis circuit (lC301a). The sub-audible tone signal (67.0-254. 1 Hz) generated by the 4th LO circuit (PLL unit, IC751) is also applied to the IDC circuit via the low-pass filter (C305) when the [TONE] is ON.

The IDC circuit limits the audio pass-band width and the signals are output from pin 7. The signals are applied to the deviation control circuit (Q301) to select a maximum deviation level (wide or narrow) and applied to the FM oscillator circuit (Q303).

The audio signal from the deviation control circuit change the reactance of D303 to obtain FM modulation.

The modulated signal is applied to the 3rd mixer circuit (IC51) via the buffer-amplifier (Q302) and LO switch (D63).

2-5 SPEECH COMPRESSOR CIRCUIT
(MAIN UNIT)

The speech compressor compresses the microphone audio signals to increase the average talk power.

When the [COMP] switch is ON, the audio signals from the AF amplifier section in IC502 (pin 4) are applied to the VCA circuit (lC512). The output signals from pin 9 are applied to the compressor amplifier (IC5II) to obtain an average audio level.

The amplified signals are applied to the VCA section in IC502 (pin 7) via the analog switch (IC513, pins 6, 1).

2-6 IF AMPLIFIER AND MIXER CIRCUITS
(MAIN AND RF UNITS)

The modulated 4th IF signals from the DSP circuit (DTIF: 15.625 kHz) are applied to the 4th mixer circuit (MAIN unit, IC201) to be converted into 455 kHz 3rd IF signals after passing through the T/R switch (MAIN unit, D212). The mixed signal is output from pin 3 and amplified at the IF amplifier (MAIN unit, Q201) after unwanted signals are sup-pressed at the ceramic band-pass filter (MAIN unit, FI204.
The amplified 3rd IF signal is applied to the 3rd mixer circuit (MAIN unit, IC51).

The applied 3rd IF signal is mixed with the 3rd LO signal applied from the DDS circuit (PLL unit, IC701) via the LO switch (MAIN unit, D62) to produce a 9 MHz 2nd IF signal. The 2nd IF signal is applied to the IF amplifier (MAIN unit, Q52) after out-of-band signals are suppressed at the band-pass filter (MAIN unit, FI51). The amplified signal is applied to the 2nd mixer circuit in the RF unit via J53.

The 2nd IF signal is mixed with the 60 MHz 2nd LO signal, coming from the PLL unit, at the 2nd mixer circuit (D302) to obtain a 69 MHz 1st IF signal. The 1st IF signal is passed through the MCF (FI81b) to cut-off the undesired signals then amplified at the IF amplifier (Q301) via the T/R switch (D301). The amplified 1st IF signal is applied to the balanced mixer circuit (RF unit, Q381, Q382).

The operating (transmitting) frequency is produced at the balanced mixer circuit (Q381, Q382) by mixing the 1st IF and 1st LO signals. The mixed signal is then applied to the

RF circuit.

2-7 RF CIRCUIT (RF AND PA UNITS)

The RF circuit amplifies operating (transmitting) frequency to obtain 100 W of RF output.

The signal from the balanced mixer circuit is amplified at the wide-band YGR amplifier (RF unit, IC801) after passing through one of 11 band-pass (Refer to page 4-1 for band-pass filters used) and high-pass filters, and is then applied to the PA unit via J821.

The signal applied from the RF unit is amplified at the pre-drive (Q1), drive (Q2, Q3) and power amplifiers (Q4, Q5) in sequence to obtain a stable 100 W of RF output power. The amplified signal is applied to one of 7 low-pass filters In the FILTER unit.

2-8 LOW-PASS FILTER CIRCUIT (FILTER UNIT)

The low-pass filter circuit contains 7 Chebyschev low-pass filters to suppress the higher harmonic components.

The signal from the power amplifiers in the PA unit is applied to one of the low-pass filters, which is selected by the I/O expander (lCII) in the CTRL unit via the buffer-amplifier (CTRL unit, IC12).

The filtered signal is then applied to one of 2 antenna connectors via the CTRL only/and TUNER unit/s.

2-9 ALC CIRCUIT (MAIN UNIT)

The ALC (Automatic Level Control) circuit controls the gain of IF amplifiers in order for the transceiver to output a constant RF power set by the [RF POWER] control even when the supplied voltage shots, etc.

The RF power level is detected at one of the APC detector circuits (CTRL unit, D1) to be converted into DC voltage and applied to the MAIN unit as the FOR signal.

The FOR signal from the CTRL unit is applied to the comparator (lC602a, pin 2). The POCV signal, controlled by the [RF POWER] control via the I/O expander (lC509, pin 8), is also applied to the other input (pin 3) for reference. The compared signal is output

from pin 1 and applied to the IF amplifiers in the MAIN (Q52) and RF (Q301) units to control amplifying gain.

When the FOR signal exceeds the POCV voltage, ALC bias voltage from the comparator controls the IF amplifiers. This adjusts the output power to a specified level from the [RF POWER] control until the FOR and POCV voltages are equalized.

In AM mode, the comparator operates as an averaging ALC amplifier. Q603 turns ON and the POCV voltage is shifted for 40 W AM output power (maximum) through R617.

The ALC bias voltage is also applied to the ALC meter amplifier (IC602c, pin 9) to obtain an ALC meter signal (ALCL). The amplified signal is applied to the main CPU (IC801, pin 79) to drive the S/RF meter via the sub CPU on the FRONT unit.

An external ALC input from the [ALC] jack or [ACC] sockets is applied to the buffer amplifier (Q605). External ALC operation is identical to that of the internal ALC.

The FOR signal is also applied to the power meter amplifier (IC601b, pin 5). The amplified signal is applied to the main CPU (IC801) as an FORL signal to drive the S/RF meter when the power meter is selected.

2-10 APC CIRCUIT (MAIN UNIT)

The APC (Automatic Power Control) circuit protects the power amplifiers on the PA unit from high SWR and excel-sive current.

The reflected wave signal appears and increases when the connected antenna is mismatched to 50 Ω. The APC detector circuit (CTRL unit, D2, L1) detects the reflected signal, and applies it to the APC circuit (IC602d, pin 13) as a REF signal.

When the REF signal level increases, the APC circuit decreases the ALC voltage to activate the APC.

For the current APC, the power transistor current is obtained by detecting the voltages (ICH and ICL) which appear at both terminals of the current detector (PA unit, R28).

The detected voltages are applied to the differential amplifier (IC602b, pins 5, 6). When the current of transistors is increased, the amplifier controls the ALC line to prevent excessive current flow.

A portion of the REF signal is applied to the SWR meter amplifier (IC601a, pin 3). The amplified signal is applied to the main CPU (IC801) as an REFL signal to drive the S/RF meter when the SWR meter is selected.

4-2-11 TEMPERATURE PROTECTION CIRCUIT
(PA UNIT)

The cooling fan (MF1) is activated while transmitting or when the temperature of the power amplifier exceeds the preset value. The temperature protection circuit consists of 010-013 and R50.

While transmitting, Q10 and Q12 are turned ON, and provide a voltage to the cooling fan to rotate at medium speed. The thermistor detects the temperature of Q5, and activates Q11 and Q13 to accelerate the cooling fan when the detected temperature exceeds 60℃ (140 F). The cooling fan rotates at hi h speed at 8O℃ (176 F) or more.

The thermistor keeps the cooling fan rotating even while receiving until the Q5 temperature drops to 60℃ (140 F) or below.

2-12 MONITOR CIRCUIT (MAIN UNIT)

The microphone audio signals can be monitored to check voice characteristics.

A portion of the microphone audio signals from the amplifier (DSP board, IC414b) via the low-pass filter (IC503d) or the VCA section in IC502 are applied to the analog switch (IC508). The selected audio signals are applied to IC509 (pin 2), and the output signal from pin 9 are applied to the AF amplifier circuit (IC506, pin 7).

3 PLL CIRCUITS
3-1 GENERAL

The PLL unit generates a pair of 1st LO frequencies (69.04-129.0115 MHz) for dual-watch and spectrum scope functions; a 2nd LO frequency (60 MHz), 3rd LO frequency

(9.465 MHz), 4th LO frequency (439.375 kHz) and sweep LO frequency for the spectrum scope function, CW side (300-900 Hz) and FM sub-audible (67.0-254.1 Hz) tones.

The 1st LO PLLS adopt a mixer-less dual loop PLL system and has 3 VCO circuits. The Los, except the 2nd, use DDSs while the 2nd LO uses the fixed frequency of the crystal oscillator.

3-2 1st LO PLL CIRCUIT

The 1st LO PLLS contain a main and reference loop as a dual loop system. Both PLLS have equivalent circuits- this manual describes only the 1st LO PLL A circuit.

The reference loop generates a 10.506 to 10.543 MHz frequency using a DDS circuit, and the main loop generates a 69.04 to 129.0115 MHz frequency using the reference loop frequency.

(1) REFERENCE LOOP PLL

The oscillated signal at the reference VCO (Q151, D151) is amplified at the amplifiers (Q152, Q102) and is then applied to the DDS IC (lCI01, pin 46). The signal is then divided and detected on phase with the DDS generated frequency.

The detected signal output from the DDS IC (pin 56) is converted into DC voltage (lock voltage) at the loop filter (R135-R137, C121) and then fed back to the reference VCO circuit (Q151, D151).

(2) MAIN LOOP PLL

The oscillated signal at one of the main loop VCOs (VCO-A board, Q201, D201, Q221, D221, 0251, D251) is amplified at the buffer amplifier (VCO-A board, Q301) and is then applied to the PLL IC (lC381, pin 4). The signal is then divided and detected on phase with the reference loop out-put frequency.

The detected signal output from the PLL IC (pin 13) is converted into a DC voltage (lock voltage) at the loop filter and then fed back to one of the VCO circuits (VCO-A board, Q201, D201,Q221, D221,Q251, D251).

The oscillated signal is amplified at the buffer amplifier (Q301) and then applied to the RF unit as a 1st LO A signal after being passed through the band-pass filter (L352,

C351- C353).

3-3 2nd LO AND REFERENCE OSCILLATOR CIRCUITS

The reference oscillator (X51, Q51) generates a 30.0 MHz frequency for the 5 DDS circuits as a system clock and for the LO output. The oscillated signal is doubled by 2 at the doubler circa (Q71, Q81) and the 60.0 MHz frequency is picked up at the double tuned filter (L8l, L82). The 60.0 MHz signal is applied to the RF unit as a 2nd LO signal.

3-4 3rd and 4th LO CIRCUITS

The DDS ICs (lC701 for 3rd, IC751 for 4th) generate a 10-bit digital signal using the 30 MHz system clock. The digital signal is converted into an analog wave signal at the D/A converter (R701-R720 for 3rd, R751-R770 for 4th). The converted analog wave is passed through the band-pass filter (L702, L703, C709-C713 for 3rd, L752, L753, C759-C763 for 4th) and then applied to the MAIN unit as the 3rd or 4th LO signal.

The 4th LO circuit generates not only the 4th LO signal but also the sub-audible tone and CW side tone signals.

3-5 MARKER CIRCUIT

The divided signal at the DDS circuit (lC101) is used for the marker signals with the IC-756.

The reference signal for the DDS circuit (30.0 MHz) is divided by 2 to produce an acceptable frequency signal, 15MHz, with the programmable divider then divided again by 150 to obtain 100 kHz cycle square-wave signals.

The generated marker signals are output from pin 68 of the DDS IC (lCI01) and then applied to the RF unit via the mute switch (lC192) and J851 as the MKR signal.

4 ANTENNA TUNER CIRCUITS

4-1 MATCHING CIRCUIT (TUNER UNIT)

The matching circuit is a T-network. Using 2 tuning motors, the matching circuit

obtains rapid overall tuning speed.

Using relays (RL1-RL15), the relay control signals from the antenna tuner CPU (CTRL unit, IC5) via the buffer amplifier (IC1, IC2) ground one of the taps of L3-L12 and add capacitors (C27- C43). After selecting the coils and capacitors, 2motors (CTRL unit, M1, M2) adjust C44 and C45 using the antenna tuner CPU (CTRL unit, IC5) and the motor driver (CTRL unit, IC7) to obtain a low SWR (Standing Wave Ratio).

4-2 DETECTOR CIRCUIT (CTRL UNIT)

(1) SWR detector

Forward and reflected power are picked up by a current transformer (L1), detected by D2 and D1, and then amplified at IC1a and IC1b, respectively. The amplified voltages are applied to the antenna tuner CPU (IC5, pins 2, 3). The CPU detects the SWR.

(2) Reactance components detector

Reactance components are picked up by comparing the phases of the RF current and RF voltage. The RF current is detected by L4 and R16) buffer-amplified at IC14e and IC2a and then applied to the phase comparator (IC3a). RF volt-ages are detected by C12-C14 and then applied to the phase comparator (IC3b) after being amplified at the buffer-amplifiers (IC14c, IC2b). The output Signal from the phase comparator (IC3a, pin 6 for RF current, IC3b pin 7 for RF voltage) is rectified at D7 and D6 for conversion into DC voltage. The rectified voltage signals are combined, then amplified at the inverter amplifier (IC4b), then applied to the antenna tuner CPU (IC5, pin 64).

A C-MOS IC is used for the buffer-amplifier (IC14) to improve functionable sensitivity; the inverter amplifier (IC4) is very responsive even with a low signal level input. Together, these ensure quick and stable signal detection even at low RF signal level input.

(3) Resistance components detector

Resistance components are picked up by L8, and detected by D8, D9 and Q5. The detected resistance components are amplified at the inverter amplifier (IC4a), and then applied to the antenna tuner CPU (IC5, pin 1).

4-3 MOTOR CONTROL CIRCUIT

The control circuit of the internal antenna tuner consists of the CPU, EEPROM*, tuning motors and tuning relays. * Electronically-Erasable Programmable Read Only Memory.

(1) CPU and EEPROM (CTRL unit)
The antenna tuner CPU (IC5) controls the tuning motors via the motor driver (IC7) and tuning relays, and memorizes the best preset position in 100 kHz steps. The memory con-tents are stored in the EEPROM (IC6) without a backup battery.

(2) Tuning motors (CTRL unit)
A motor driver (IC7) rotates the tuning motors (M1, M2) to obtain a low SWR.

(3) Tuning relays (TUNER unit)

According to the operating frequency band and antenna condition, tuning relays select the capacitors and coils.

5 SCOPE CIRCUITS

5-1 SCOPE RECEIVER CIRCUIT (RF UNIT)

A portion of the 69 MHz 1st IF signal from the 1st mixer circuit (Q261, Q262: while receiving) or IF amplifier (Q301: while transmitting) is amplified at the IF amplifier (Q942), then passed through the band-pass filter (L941, L942) to suppress unwanted signals. The filtered signal is mixed with the 60 MHz 2nd LO signal at the mixer circuit (IC941, pin 6) to produce the 9 MHz IF signal after being amplified at the IF amplifier (0943). The mixed IF signals are applied to the FM IF IC (IC901, pin 16).

The applied 9 MHz IF signal is mixed with the sweep LO signals from the PLL unit at the FM IF IC (IC901), which includes the RSSI terminal. The mixed IF signals are filtered at the ceramic band-pass filter (FI942) then applied to the limiter amplifier section in the FM IF IC (IC901, pin 5).
The applied IF signals are converted into DC voltages according to the applied IF signal strength at the RSSI section in the IC.

The converted voltages are amplified at IC961a then applied to the MAIN unit as the

SCPL signal.

Some of the DC voltages from the FM IF IC are amplified at IC961b to produce AGC voltages for the IF amplifiers (Q941, Q942), producing wider dynamic range.

By sweeping LO signals (SLO) applied to the mixer section in the FM IF IC, the spectrum scope function is activated.

5-2 SWEEP LO CIRCUS (PLL UNIT)

The sweep LO signals (SLO) are generated by the DDS IC (lC801) using the 30 MHz system clock. A 10-bit digital signal is converted into analog wave signals at the D/A converter (R8O1- R820). The converted analog wave is passed through the band-pass filter (L802, L803, C809- C813) then applied to the RF unit after being amplified at the LO amplifier.

6 LOGIC CIRCUITS

6-1 BAND SELECTION DATA
(RF, CTRL AND PLL UNITS)

To select the correct band-pass, low-pass filters and VCOs on the RF, MAIN, FILTER and PLL units, the main CPU (MAIN unit, IC801) outputs the following band selection data via the I/O expander (RF unit, IC1, IC21, CTRL unit, IC11), A/D convector (MAIN unit, lC810) or DDS IC (PLL unit, IC101, lC401) depending on the displayed frequency.

The D/A convector (MAIN unit, IC809) output signal from pin 9 is amplified at IC813c (pins 8-10) to obtain the band volt- age for external equipment via the [ACC 2] connector pin 4.