1 RECEIVER CIRCUITS

1-1 HF/50 MHz RF CIRCUIT

(FILTER, MAIN AND HPF BOARDS)

HF/50 MHz RF filters pass only the desired band signals and suppress any undesired band signals. The HF/50 MHz RF circuit has 7 low-pass filters and 7 high-pass filters for specified band use.

HF/50 MHz RF signals from the [ANT1] connector, pass through one of 7 low-pass filters as below, the transmit/ receive switching relay (FILTER unit; RL1) and low-pass filter (FILTER unit; L1, L2, C1-C5), and are then applied to the MAIN board via J1 (FILTER unit).

The signals from the FILTER board are applied to or bypass the 20 dB attenuator (R122, R125, R126). The signals pass through the high-pass filter (L132, L133, C132-C137) to suppress strong signals below 1.6 MHz and are then applied to the HPF board via the “TOAT” terminal.

(1) 0.03-2 MHz and 30-40 MHz

The signals pass through a low-pass filter (L101, L102, C101-C105), and then applied to the preamplifier circuit on the MAIN board.

(2) 2-30 MHz

The signals from the low-pass filter (L101, L102, C101-C105) are applied to one of 6 high-pass filters as at right above and are then applied to the preamplifier circuit on the MAIN board.

(3) 40-60 MHz

The signals pass through the low-pass filter (L172, L173, C172-C176) and the high-pass filter (L174, L175, C177-C181) via D171 and are then applied to the preamplifier circuit on the MAIN board.

1-2 VHF AND UHF RF CIRCUIT (PA UNIT)

The VHF and UHF RF circuit passes and amplifies only the desired band signals and suppresses any undesired band signals. The VHF RF circuit has a preamplifier and band-pass filters.

The VHF RF signals from the [ANT2] connector pass through the low-pass filter (L263, L264, L265, C274-C277) and antenna switching circuit (D261, D291, D292, D293). The signals are amplified at the preamplifier circuit (Q403) between the band-pass filters (D406, D407 and D410).

The UHF RF signals from the [ANT2] connector pass through the high-pass filter (L316, L317, C326-C327), pass through the low-pass filter (L314, L315, C322-C325) and antenna switching circuit (D341, D342, D343). The signals are amplified at the preamplifier circuit (Q453) between the band-pass filters (D454, D456).

The filtered signals are applied to the MAIN board via J481 (PA unit) and are then applied to the preamplifier circuit.

1-3 PREAMPLIFIER CIRCUIT (MAIN BOARD)

The preamplifier circuit in the IC-706MKIIG has approx. 15dB gain over a wide-band frequency range.

When the preamplifier is turned ON, the signals from the RF circuit are applied to the preamplifier (IC151) via D2182. Amplified or bypassed signals are applied to the 1st mixer circuit (D271).

1-4 1ST MIXER CIRCUIT (MAIN BOARD)

The 1st mixer circuit mixes the receive signals with the 1st LO signal to convert the receive signal frequencies to a 69 or 70.7 MHz 1st IF.

The signals from the preamplifier circuit, or signals which bypass the preamplifier, are applied to a low-pass filter and then to the 1st mixer (D271).

The 1st LO signals (69.0415-539.0115 MHz) enter the MAIN board from the PLL unit via J281. The LO signal is amplified at IC-281, filtered by a low-pass filter, and then, applied to the 1st mixer.

1-5 1ST IF CIRCUIT (MAIN BOARD)

The 1st IF circuit filters and amplifies the 1st IF signals. The 1st IF signals are applied to a Crystal Filter (FI511) to suppress out-of-band signals.

The 69 MHz 1st IF signals (except WFM) pass through the crystal filter (FI511), however, the 70.7 MHz 1st IF signal (WFM) passes through a band-pass filter (L501-L504, C501-C506). Then the filtered signals are applied to the IF amplifier (IC281).

The AGC voltage is supplied to the transmit/receive switching circuit (D521, D522) and D521/D522 function as PIN attenuators for AGC operation.

The amplified signals are then applied to the 2nd mixer circuit (D551) via the band-pass filter (L542-L546, C542-C545).

1-6 2ND MIXER CIRCUIT (MAIN BOARD)

The 2nd mixer circuit mixes the 1st IF signals and 2nd LO signal (60.00 MHz) to convert the 1st IF to a 2nd IF.

The 1st IF signals from the band pass filter (L542-L546, C542-C545) are converted to 9 MHz or 10.7 MHz 2nd IF signals at the 2nd mixer (D551).

The 2nd IF signals are applied to the band-pass filter (FI561) to suppress undesired signals, such as the 2nd LO signal, and are then applied to the noise blanker gate (D561, D562).

While in WFM mode, the IF signals pass through the low-pass filter (L601, C601-C603), IF amplifier (Q601), ceramic filter (FI611) and IF amplifier (Q611). The signals are then applied to the WFM demodulator circuit (IC631).

1-7 NOISE BLANKER CIRCUIT (MAIN BOARD)

The noise blanker circuit detects pulse type noise, and turns OFF the signal line when noise appears.

A portion of the signals from FI561 are amplified at the noise amplifiers (Q621, Q638, amplifier section of IC631), then detected at the noise detector (D632) to convert the noise components to DC voltages.

The converted voltages are then applied to the noise blanker switch (Q634, Q635). At the moment the detected voltage exceeds Q634's threshold level, Q635 outputs a blanking signal to close the noise blanker gate (D561, D562) by applying reverse-biased voltage.

The detected voltage from D632 is also applied to the noise blanker AGC circuit (Q631, Q633) and is then fed back to the noise amplifier (IC631) as a bias voltage. The noise AGC circuit prevents closure of the noise blanker gate for long periods by non-pulse-type noise. The time constant of the noise blanker AGC circuit is determined by R637.

The 2nd IF signals from the noise blanker gate are then applied to the 2nd IF circuit.

1-8 2ND IF CIRCUIT

The 2nd IF circuit amplifies and filters the 2nd IF signals.

The 2nd IF signals from the noise blanker gate (D561, D562) are amplified at the IF amplifier (IC571) via the Tx/Rx switch (D572) and applied to a 2nd IF filter as shown below.

The filtered or bypassed signals are applied to the buffer amplifier (Q721), IF amplifiers (Q731, Q741) and buffer amplifier (Q751) to obtain a detectable level at the demodulator circuit

The amplified signals from the buffer amplifier (Q751) are shared between the SSB/CW/RTTY detector (IC841), AM detector (D761) and AGC detector (D771). Output signals from Q721 are applied to the FM IF IC (IC791).

1-9 IF SHIFT CIRCUIT (MAIN BOARD)

The IF shift circuit shifts the center frequency of IF signals to electronically shift the center frequency.

The IF shift circuit shifts the 1st LO and BFO within • 1.2 kHz in SSB/CW/RTTY modes or • 250 Hz in CW-N/RTTY-N modes. As a result, the 2nd IF (also 1st IF) is shifted from the center frequency of the 2nd IF filter (FI671, FI681 or optional IF filters). This means 2nd IF signals do not pass through the center of the 2nd IF filter. Therefore, the higher or lower frequency components of the IF are cut out. Since the BFO frequency is also shifted the same value as the 1st IF, frequency is corrected at the detector.
In the IC-706MKIIG, the 1st LO frequency is shifted to change the 2nd IF because a fixed 2nd LO frequency (60 MHz) is used. The 1st IF filter (FI671) and crystal filter (FI561) have 15 kHz pass-band widths, and do not affect IF shift operation.

1-10 AGC CIRCUIT (MAIN BOARD)

The AGC (Automatic Gain Control) circuit reduces IF amplifier gain to keep the audio output at a constant level. The receiver gain is determined by the voltage on the AGC line (Q776 collector).

The 2nd IF signal from the buffer amplifier (Q751) is detected at the AGC detector (D771) and applied to the AGC amplifiers (IC881b, Q9). IC881b sets the receiver gain with the [RF/SQL] control via the “RFGC” signal line.

When receiving strong signals, the detected voltage increases and the AGC voltage decreases via the DC amplifier (Q776). The AGC voltage is used for the bias voltage of the transmit/receive switching PIN diodes (D521, D522, D572, D573) to attenuate the received signals.

When AGC slow is selected, C775 and R778 are connected in parallel to obtain appropriate AGC characteristics.

1-11 S-METER CIRCUIT (MAIN BOARD)

The S-meter circuit indicates the relative received signal strength while receiving by utilizing the AGC voltage which changes depending on the received signal strength.

The output voltage of the AGC amplifier (IC811b, pin 1) is applied to the main CPU (IC2001, pin 30) as an S-meter signal via the “SMV” signal line. The FM S-meter signal from the FM IF IC (IC797, pin 12) is also applied to the main CPU (IC2001, pin 30) via Q774.

The S-meter signal from the main CPU (IC2001) is applied to the sub CPU and is then displayed on the S-meter readout.

1-12 SQUELCH CIRCUIT (MAIN BOARD)

The squelch circuit mutes audio output when the S-meter signal is lower than the [RF/SQL] control setting level.

The S-meter signal is applied to the main CPU (IC2001 pin 30) in SSB/CW/RTTY modes and is compared with the threshold level set by the [RF/SQL] control. The [RF/SQL] setting is picked up at the sub CPU (DISPLAY board; IC1, pin 99). The main CPU compares the S-meter signal and [RF/SQL] setting, and controls the AF selector switch (IC861) to cut out AF signals via IC2122a.

In FM mode, a portion of the AF signals from the FM IF IC (IC797, pin 9) are applied to the active filter section (pin 8) where noise components above 20 kHz are amplified. The signals are rectified at the noise detector section and then output from pin 14. The noise squelch signal from pin 14 is applied to the main CPU (pin 31) via the “NSQV” signal line. The CPU then controls the AF selector switch (IC861).

1-13 DEMODULATOR CIRCUITS (MAIN BOARD)

(1) SSB/CW/RTTY modes

The 2nd IF signals from the buffer amplifier (Q751) are mixed with the BFO signal from the PLL unit at the product detector (IC841, pin 6). The detected AF signals from IC841 (pin 3) are applied to the AF selector switch (IC861, pin 12).

(2) AM mode

The 2nd IF signals from the buffer amplifier (Q751) are detected at the AM detector (D761). The detected AF signal is applied to the AF selector switch (IC861, pin 15).

(3) FM/FM NARROW modes
The 2nd IF signals from the buffer amplifier (Q721) are applied to the FM IF IC (IC797, pin 16) where the IF signals are converted into 455 kHz IF signals. The signals pass through FI6 and are applied to the quadrature detector section. X1 is used for quadrature detector. The detected AF signals from pin 9 are then applied to the AF selector switch (IC861, pin 14) via the de-emphasis circuit (IC811a).

(4) WFM mode
The 2nd IF signals from the IF amplifier (Q601) pass through FI611, are amplified at Q611 and are then applied to the FM IF IC (IC631, pins 2, 3) where the IF signals are converted into AF signals. The detected AF signals from pin 8 are then applied to the AF selector switch (IC861, pin 11).

1-14 AF SELECTOR SWITCH (MAIN BOARD)
The AF signals from one of the detector circuits are applied to the AF selector switch (IC861). IC861 consists of dual 4-channel analog switches which are selected with a mode signal and the squelch control signal.

1-15 AF AMPLIFIER CIRCUIT (PLL UNIT)
The AF amplifier amplifies the demodulated signal to a suitable driving level for the speaker.

The AF signals from the AF selector switch (MAIN board; IC861) are applied to the PLL unit via the “AFI” signal line. The CW side tone/beep tone and optional synthesized voice are also applied to the PLL unit via the “AFBP” signal line.
The AF signals from the MAIN board are applied to the VCA (Voltage Controlled Amplifier) circuit (IC201). The AF gain setting from the main CPU is converted to DC voltage at the D/A converter (MAIN board IC2201) and applied to the VCA control terminal (IC201, pin 8) via the “AFGC” signal line. The output AF signal from IC281 (pin 9) is power-amplified at IC5 to drive the speaker.

2 TRANSMITTER CIRCUITS
2-1 MICROPHONE AMPLIFIER CIRCUIT
(MAIN BOARD)
The microphone amplifier circuit amplifies microphone input signals and outputs the amplified signals to the balanced modulator or FM modulation circuit.

Audio signals from the front or rear panel [MIC] connector enter the microphone amplifier IC (IC931, pin 22) and are then amplified at the microphone amplifier or speech compressor section. Compression level is adjusted with the [COMP GAIN] control (R945).

The amplified or compressed signals are applied to the VCA section of IC931. The microphone gain setting from the D/A converter (IC2201, pin 11) is applied to the VCA control terminal (IC931, pin 10). The resulting signals from pin 9 are then applied to the buffer amplifier (Q961). External modulation input from the [ACC] socket (pin 11) is also applied to Q961.

While in SSB mode, the amplified signals from the buffer amplifier (Q961) are applied to the AF selector switch (IC971) and then to the balanced modulator (IC1041).

While in AM/FM mode, the amplified signals from the buffer amplifier (Q961) are applied to the limiter amplifier (IC981a) and splatter filter (IC981b). The signals are then applied to the AF selector switch (IC971) in AM mode or to the varactor diode (D1012) in FM mode.

2-2 VOX CIRCUIT (MAIN BOARD)
The VOX (Voice-Operated-Transmission) circuit sets transmitting conditions according to voice input. The microphone amplifier IC (IC931) includes the VOX circuit.

The microphone signals from IC931 (pin 19) pass through the [VOX GAIN] control (IC-2001) and are then applied to the VOX comparator section (IC931, pin 18) to switch the keying input of the main CPU (IC2001, pin 15). When voice levels exceed the reference level, the VOX circuit sets the transceiver to

transmit.

On the other hand, a speaker drive signal from the AF power amplifier (PLL unit IC231) is applied to the anti-VOX comparator section (IC931, pin 14) via the [ANTI VOX] control (IC-2001). When the audio output level increases, this comparator cuts outs the VOX comparator via the MUTE terminal (IC931, pin 16).

2-3 BALANCED MODULATOR (MAIN BOARD)

The balanced modulator converts the AF signals from the microphone amplifier to a 9 MHz IF signal with a BFO (Beat Frequency Oscillator) signal.

Microphone signals from the AF selector switch (IC971) are applied to the balanced modulator (IC1041 pin 6). The BFO signal from the PLL unit is applied to IC1041 (pin 8) as a carrier signal.

IC1041 is a double balanced mixer IC and outputs a double side band (DSB) signal with -40 dB of carrier suppression. R1041 and R1045 adjust the balanced level of IC1041 for maximum carrier suppression. The resulting signal passes through a 9 MHz IF filter (FI4 in SSB/CW/RTTY modes) to suppress unwanted side-band signals.

In AM mode, R1042 is connected to upset the balance of IC1041 via Q1041 for leaking the BFO signal as a carrier signal. The CW keying/RTTY TX signal is applied to IC1041 pin 6.

2-4 FM MODULATION CIRCUIT (MAIN BOARD)

The microphone signals from Q961 are applied to the limiter amplifier (IC981a) and the splatter filter (IC981b). The 1750 Hz European tone signal from the main CPU (IC2001 pin 40) is also applied to IC981a pin 2 for European repeaters. The sub-audible tone signal (67.0-254.1 Hz) from the main CPU (IC2001 pin 37) is also applied to IC981b pin 5 for repeater use.

The resulting signals are applied to the VCO circuit (Q1011, D1012) via R1003 to change the reactance of the varactor diode (D1012) for FM modulation. The modulated signal is buffer-amplified at Q1013 and bypasses the 9 MHz IF filter.

2-5 TRANSMITTER IF CIRCUIT (MAIN BOARD)

The 9 MHz IF signal from the modulation circuit passes through the 9 MHz IF filter (FI671 in SSB/CW/RTTY modes; FI681 in AM/FM-N modes; through in FM mode). The signal is amplified at IC571, and then passes through the total gain adjustment volume (R579), and the crystal filter (FI561). The signal is then applied to the 2nd mixer (D551).

The signal is mixed with the 2nd LO signal (60 MHz) and converted to a 69 MHz IF signal at the 2nd mixer (D551). The 69 MHz IF signal passes through a band-pass filter, the IF amplifier (IC281) and the 69 MHz IF filter (FI511) and is then converted to the displayed frequency at the 1st mixer (D271) with the 1st LO signal. The mixers (D271, D551) and IF amplifiers (IC281, IC571) are used commonly for both receiving and transmitting.
The ALC voltage is supplied to the transmit/receive switching circuit (D521/D522 and D572/D573). D521/D522 and D572/D573 function as PIN attenuators for ALC operation.

2-6 RF CIRCUIT
(PA UNIT, MAIN AND HPF BOARD)

The RF circuit amplifies the displayed frequency signal to obtain 100 W of RF output power for HF/50 MHz bands and 20 W for the 144 MHz band.

The HF/50 MHz RF signal from the 1st mixer (D271) via the low-pass filter enters the HPF board and then passes through one of 6 high-pass filters (Refer to 3-1 for used RF high-pass filter.). The 50 MHz RF signal passes through a low-pass filter additionally. The filtered signal returns to the MAIN board, is amplified at the YGR amplifier (IC231), and is then applied to the PA unit.

The 144 MHz RF signal from the 1st mixer (D271) via the low-pass filter (L251-253, C253-259) bypasses the filters and passes through the high-pass filter (L182-L184, C181-C186) in the MAIN board. The signal is amplified at the RF amplifier (IC222) and YGR amplifer (IC231) and is then applied to the PA unit.

The signal from IC231 enters the PA unit and is amplified at the drive amplifiers (Q101, Q121) in sequence. The amplified signal is applied to the band switch (RL1).

The HF/50 MHz RF signal from the band switch (RL1) is amplified at a power amplifier (Q171, Q172) to obtain a stable 100 W of RF output power. The power amplified signal is then applied to the [ANT1] connector via one of the low-pass filters in the FILTER board.

For the 144 MHz RF signal from the band switch (RL1), 50 W of RF output power is obtained at the power amplifier (Q231) and the signal is applied to the [ANT2] connector via the antenna switching circuit and low-pass filter.

For the 430 MHz RF signal from the band switch (RL1), 20 W of RF output power is obtained at the power amplifier (Q231) and the signal is applied to the [ANT2] connector via the antenna switching circuit and low-pass filter.

2-8 ALC CIRCUIT (MAIN BOARD)

The ALC (Automatic Level Control) circuit reduces the gain of IF amplifiers in order for the transceiver to output a constant RF power set by the RF power setting even when the supplied voltage shifts, etc.

The HF/50 MHz RF power signal level is detected at the power detector (FILTER board; D9), buffer-amplified at IC1b and applied to the MAIN board as the “FOR” voltage. The 144 MHz RF power signal level is detected at the power detectors (PA unit; D312, D313) and applied to the MAIN board as the “VFOR” voltage.

The “FOR” and “VFOR” voltages are combined to the “FORV” voltage and then applied to IC1091b (pin 6). The “POC” voltage from the D/A converter (IC2201, pin 12), determined by the RF power setting, is applied to IC1091b (pin 5) as the reference voltage.

When the “FORV” voltage exceeds the “POC” voltage, ALC bias voltage from IC1091a (pin 1) controls the PIN diodes (D521, D522, D572, D573) using Q1092. This adjusts the output power to the level determined by the RF power setting until the “FORV” and “POC” voltages are equalized.

In AM mode, IC1091a operates as an averaging ALC amplifier with Q1091 and C1091. Q1071 turns ON and the “POC” voltage is shifted for 40 W AM output power (maximum, 8 W for 144 MHz band) through R499.

The ALC bias voltage from IC1091a is also applied to the main CPU (IC2001 pin 34) as “ALCV” voltage for ALC meter indication.

An external ALC input (minus voltage) from the [ACC] socket (pin 6) is shifted to plus voltage at D 1131 and is applied to the buffer amplifier (Q1131). External ALC operation is identical to that of the internal ALC.

2-9 APC CIRCUIT (MAIN BOARD)

The APC (Automatic Power Control) circuit protects the power amplifiers on the PA unit from high SWR and excessive current for the HF/50 MHz bands.

The reflected wave signal appears and increases on the antenna connector when the antenna is mismatched. The HF/50 MHz reflected signal level is detected at D10 (FILTER board), buffer-amplified at IC1a and applied to the MAIN board as the “REFV” voltage.

When the “REFV” signal level increases, IC1091c decreases the ALC voltage via IC1091a to activate the ALC.

For the current APC, the driving current at the power amplifier is detected in the voltages (“ICH” and “ICL”) which appear at both terminals of a 0.012ƒ ¶resistor (R201) on the PA unit. The detected voltages are applied to the differential amplifier (IC1091d pins 12, 13). When the current of the power amplifier exceeds 22 A, IC7d controls the ALC line via IC7a to prevent excessive current flow.

2-10 RF, ALC, SWR METER CIRCUITS
(MAIN BOARD)

While transmitting, RF, ALC or SWR meter readings are available and can be selected with the [MET] switch.

(1) Power meter

The “FOR” and “VSOR” voltages are combined to “FORV” voltage and it is then applied to the main CPU (IC2001 pin 32) for indicating the output power.

(2) ALC meter

The ALC bias voltage from IC1091a pin 1 is applied to the main CPU (IC2001 pin 34) for indicating the ALC level.

(3) SWR meter

The “FORV” and “REFV” voltages are applied to the main CPU pins 32 and 33, respectively. The main CPU compares the ratio of “FORV” to “REFV” voltage and indicates the SWR for the [ANT1] connector.

3 PLL CIRCUITS

3-1 GENERAL

The PLL unit generates a 1st LO frequency (69.0415-269.0115 MHz), a 2nd LO frequency (60 MHz), a BFO frequency (9.01 MHz), an FM 3rd LO frequency (9.4665/9.4650 MHz) and a TX FM PLL reference frequency (9.0115/9.0100 MHz).

The 1st LO PLL adopts a mixer-less dual loop PLL system and has 2 VCO circuits. The BFO uses a DDS and the 2nd LO uses a fixed frequency double that of the crystal oscillator.

3-2 1ST LO PLL CIRCUIT

The 1st LO PLL contains a main loop and reference loop forming a dual loop system.

The reference loop generates a 10.6605 to 10.683 MHz frequency using a DDS circuit, and the main loop generates a 69.0415 to 134.50575 MHz frequency using the reference loop frequency.

While operating on 60 MHz and above, the output is doubled at D531 for oscillating a wide frequency range.

(1) REFERENCE LOOP PLL

The oscillated signal at the reference VCO (Q1, D1) is amplified at the amplifiers (Q21, Q51) and is then applied to the DDS IC (IC101, pin 46). The signal is then divided and detected on phase with the DDS generated frequency.

The detected signal output from IC101 (pin 56) is converted into a DC voltage (lock voltage) at the loop filter (R133, R134, C133) and then fed back to the varactor diode (D1) in the VCO circuit.

(2) MAIN LOOP PLL

The oscillated signal at one of the main loop VCOs (Q301, Q331, Q361) is amplified at the buffer amplifiers (Q10) and is then applied to the PLL IC (IC21 pin 8). The signal is then divided and detected on phase with the reference loop output frequency.

The detected signal output from IC451 (pin 2) is converted into a DC voltage (lock voltage) at the active loop filter and then fed back to one of the varactor diodes (D301, D331) in the VCO circuits. While operating on 60 MHz and above, the VCO output is doubled at D531 and amplified at Q10.

The oscillated signal passes through a low-pass or band-pass filter and is then applied to the MAIN board as a 1st LO signal.

3-3 2ND LO AND REFERENCE OSCILLATOR CIRCUITS

The reference oscillator (X502, Q521) generates a 30.0 MHz frequency used for the 1st LO and BFO circuits as a system clock and for the 2nd LO signal.

The oscillated signal is buffer-amplified at Q661, doubles at Q681 and the 60 MHz frequency is picked up at the band-pass filter (L681, L682). The 60 MHz signal is applied to the MAIN board as a 2nd LO signal.

3-4 BFO CIRCUIT

The DDS IC (IC901) generates a 10-bit digital signal. The signal is converted to an analog wave signal at the D/A converter (R951-R970). The analog wave is passed through the high-pass filter and low-pass filter. The 9 MHz BFO signal is then applied to the MAIN board via the “BFO” signal line.

While transmitting in RTTY mode, the RTTY keying signal is applied to IC901 pin 3 to shift the generated frequency and to obtain 2 frequencies for FSK operation.

While receiving in FM or FM narrow mode, the BFO circuit generates a 9.4665 MHz frequency as the 3rd LO signal.

While transmitting in FM or FM narrow mode, the BFO circuit generates a 9.0115 MHz or 9.0100 MHz frequency as the TX FM PLL reference frequency, respectively.

¥ BFO frequency