SECTION 4 CIRCUIT DESCRIPTION

4-1 RECEIVER CIRCUITS

4-1-1 DUPLEXER CIRCUIT

The transceiver has a duplexer (low-pass and high-pass filters) on the first stage from the antenna connector to separate the signals into VHF and UHF signals. The low-pass filter (L15, L16, L78, C70–C72) is for VHF signals and the high-pass filter (L44, L45, L82, C189, C190, C493) is for UHF signals. The separated signals are applied to each RF circuit.

4-1-2 VHF ANTENNA SWITCHING CIRCUIT

The antenna switching circuit functions as a low-pass filter while receiving. However, its impedance becomes very high while transmitting by turning ON diode (D18). Thus transmit signals are blocked from entering the receiver circuits. The antenna switching circuit employs a 1/4λ type diode switching system. The passed signals are then applied to the VHF RF amplifier circuit.

4-1-3 VHF SQUELCH ATTENUATOR CIRCUIT

The attenuator circuit attenuates the signal strength to a maximum of 10 dB to protect the RF amplifier from distortion when excessively strong signals are received.

The current flow of the antenna switching circuit (D18) is controlled by the [SQL] control via Q33. When the [SQL] control is rotated clockwise deeper than 12 o'clock, the current of D18 is increased. In this case, D18 acts as an attenuator.

4-1-4 VHF RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through the tunable bandpass filter (D15, L25, L26, C115–C117). The filtered signals are amplified at the VHF RF amplifier (Q16) and are then enter another 3-stage tunable bandpass filter (D11–D14, L20–L21, C94, C96–C105) to suppress unwanted signals. and improve the selectivity. The filtered signals are applied to the VHF 1st mixer circuit (Q15).The tunable bandpass filters (D11–D13, D15) employ varactor diodes to tune the center frequency of the RF passband for wide bandwidth receiving and good image response rejection. The PLL lock voltage is used for control voltage of these varactor diodes. The PLL lock voltage is amplified at the DC-amplifier (Q18) and then applied to the CPU (IC19, pin 99). The CPU outputs the control signal to the varactor diodes via the D/A converter (IC3).

4-1-5 VHF 1ST MIXER CIRCUIT

The 1st mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with a 1st LO (V-VCO output) frequency.

The signals from the VHF RF circuit are mixed with the 1st LO signal at the 1st mixer circuit (Q15) to produce a 15.65 MHz 1st IF signal.

4-1-6 VHF 1ST IF CIRCUIT

By changing the PLL frequency, only the desired frequency will pass through a pair of crystal filters at the next stage of the mixer.

The 1st IF signal from the VHF 1st mixer circuit is applied to a pair of crystal filters (FI1) to suppress out-of-band signals via a matching circuit (R61, C88). The filtered signal is amplified at the IF amplifier (Q40) and is then applied to the VHF 2nd mixer circuit (IC28).

4-1-7 VHF 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

The FM IF IC (IC28) contains the 2nd local oscillator, 2nd mixer, limiter amplifier, quadrature detector, and noise detector circuits, etc.

The 1st IF signal from the 2nd IF amplifier is applied to the 2nd mixer section of IC28 (pin 16), and is mixed with a 15.2 MHz 2nd LO signal generated by the reference oscillator circuit (X1, IC2) to produce a 450 kHz VHF 2nd IF signal.

The 2nd IF signal from the 2nd mixer passes through the 2nd IF filter (FI4) (during wide channel spacing selection, or passes through FI5 during narrow channel spacing selection; [EUR], [ITA] versions only), where unwanted signals are suppressed. It is then amplified at the limiter amplifier section (IC28, pin 5) and applied to the FM detector section (X2, IC28, pins 10, 11) for demodulation the 2nd IF signal into AF signals.

The FM detector circuit employs a quadrature detection method (liner phase detection), which uses a ceramic discriminator (X2) for phase delay to obtain a non-adjusting circuit. The detected signal from IC28 (pin 9) is applied to the AF circuit.

4-1-8 VHF AF AMPLIFIER CIRCUIT

The AF amplifier circuit amplifies the detected signals to drive a speaker. The AF circuit includes an AF mute circuit for the squelch.

AF signals from FM IF IC (IC28, pin 9) pass through the AF selector (IC21, pins 9, 8), and are then applied to the low-pass (Q83, R370–R373, C406–C409) and high-pass (Q84, R375–R379, C415–C418) filters. The filtered signals are level adjusted at the volume control IC (IC10), and are amplified at the AF power amplifier (IC12, pin 2) passing through the V-AF mute switch (Q70).

The output signal from IC12 (pin 11) drives the external or internal speaker.

4-1-9 VHF SQUELCH CIRCUIT

• NOISE SQUELCH

A noise squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

Some of the noise components in the AF signals from the FM IF IC (IC28, pin 9) are passed through the active filter section (IC28, pin 8, 7), and then applied to the noise detector section (IC28). The variable resister (R196) adjusts the input level of the active filter, and the level is used for squelch threshold reference. The detected noise signals are applied to the CPU (IC19 pin 97) via the "VSQL" line.

The [SQL] (CONTROL unit; R154) controls the input level of the sub-CPU (CONTROL unit; IC10, pin 59) in DC voltage. The sub-CPU reads the angle of the [SQL] rotation, then send the squelch data to the CPU incorporated in the RDATA line. Then the CPU controls V-AF mute switch (Q70) via the "VAMUTE" line.

Even when the squelch is closed, the V-AF mute switch (Q70) opens at the moment of emitting beep tone.

• TONE SQUELCH

The tone squelch circuit detects AF signals and opens the squelch only when receiving a signal containing a matching subaudible tone (CTCSS). When tone squelch is in use, and a signal with a mismatched or no subaudible tone is received, the tone squelch circuit mutes the AF signals even when noise squelch is open.

A portion of the AF signals from the FM IF IC (IC28, pin 9) passes through the active filter (IC20) to remove AF (voice) signals via the AF selector (IC29, pins 5, 4), and is then applied to the CTCSS decoder inside the CPU (IC19, pin 1) via the "TONEIN" line to control the AF mute switch.

4-1-10 UHF RF CIRCUIT

The UHF RF signals are passed through part of a duplexer (high-pass filter; L44, L45, L82, C189, C190, C493). The signals are then passed through the low-pass filter (L42, L43, C187, C463), antenna switching circuit (D37, D39, D72), and then amplified at the RF amplifier (Q44). A bandpass filter (FI3) is used at the next stage of the RF amplifier. The RF switch (D35, D33) turns on the UHF RF circuit when UHF signals are received.

4-1-11 UHF 1ST MIXER AND 1ST IF CIRCUITS

The filtered signals from the bandpass filter (FI3) are applied to the 1st mixer circuit (Q43). The applied signals are mixed with a 1st LO signal which comes from the U-VCO circuit (Q20, Q21) to produce a 46.05 MHz 1st IF signal.

The 1st IF signal passes through the 1st IF filter (FI2) to suppress out-of-band signals via a matching circuit (R149, C226). The filtered signal is amplified at the 1st IF amplifier (Q41) and is then applied to the 2nd mixer circuit (IC8).

4-1-12 UHF 2ND IF AND DEMODULATOR CIRCUITS

The 1st IF signal from the IF amplifier is applied to the 2nd mixer section of the FM IF IC (IC8, pin 16). The signal is mixed for producing a 450 kHz 2nd IF signal with a 45.6 MHz 2nd LO signal whitch generated by the tripler circuit (L68, L69, C208–C212) using the PLL reference frequency.

The 2nd IF signal from IC8 (pin 3) is passed through the 2nd IF filter (FI6), and is then applied to the limiter amplifier section in IC8 (pin 5). The signal is applied to the FM detector section in IC8 to demodulate into AF signals.

4-1-13 UHF AF AMPLIFIER CIRCUIT

AF signals from IC8 (pin 9) pass through the AF selector (IC21, pins 3, 4), low-pass filter (Q85, R381–R384, C415–C418) and high-pass filter (Q86, R386–R390, C419–C421).

The filtered signals pass through the volume control IC (IC10). And the level adjusted signals are applied to the AF power amplifier (IC12, pin 5) via the U-AF mute switch (Q71).

The output signal from IC12 (pin 7) drives the external speaker (connected at J2), or it is fed back to the input line of the AF power amplifier (IC12, pin 2: VHF AF line).

4-1-14 UHF SQUELCH CIRCUIT

A portion of the AF signals from the FM IF IC (IC8, pin 9) are applied to the active filter section (IC8, pin 8, 7). The active filter section amplifies and filters noise components. The filered signals are applied to the noise detector section. The variable resister (R229) adjusts the input level of the active filter, and the level is used for squelch threshold reference. The detected noise signals are output from pin 14 as the "USQL" signal, and are then applied to the CPU (IC19, pin 95).

The [SQL] (CONTROL unit; R148) controls the input level of the sub-CPU (CONTROL unit; IC10, pin 61) in DC voltage. The sub-CPU reads the angle of the [SQL] rotation, then send the squelch data to the CPU incorporated in the RDATA line. Then the CPU controls U-AF mute switch (Q71) via the "UAMUTE" line.

4-2 TRANSMITTER CIRCUITS

4-2-1 MICROPHONE AMPLIFIER CIRCUIT

The microphone amplifier circuit amplifies audio signals from the microphone to a level needed at the modulation circuit. The microphone amplifier circuit is commonly used for both the VHF and UHF bands.

The AF signals from the microphone pass through the MIC sensitivity control circuit (IC25, D66) and MIC mute switch (IC26), and are then amplified at the microphone amplifier (Q88). The amplified signals are applied to the IDC limiter amplifier (IC23b, pin 6). The output signals from the IDC limiter amplifier (IC23b, pin 7) are passed through the splatter filter (IC23a, pin 3, 1) and then applied to each VCO circuit via the deviation adjustment pot.

4-2-2 VHF MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals.

The audio signals (MOD) from the splatter filter (IC23a) change the reactance of D3 to modulate the oscillated signal at the V-VCO circuit (Q4, Q5) after passing through the frequency deviation control (R2). The modulated signals are amplified at the buffer amplifiers (Q6, Q7), and are then applied to the drive amplifier circuit via the T/R switching circuit (D4).

4-2-3 VHF DRIVE AMPLIFIER CIRCUIT

The drive amplifier circuit amplifies the VCO oscillating signal to a level needed at the power amplifier.

The RF signals from the buffer amplifier (Q7) pass through the low-pass filter (L5, C35, C36), T/R switch (D4) and attenuator (R33–R35). The Tx signal from the attenuator is amplified at the pre-drive (Q11) and drive (Q12, D5, D6) amplifiers to obtain an approximate 400 mW signal level. The amplified signal is then applied to the RF power amplifier (IC1).

4-2-4 VHF POWER AMPLIFIER CIRCUIT

The power amplifier circuit amplifies the driver signal to an output power level.

IC1 is a power module which has amplification output capabilities of about 70 W. The RF signal from the drive amplifier (Q12) is applied to IC1 (pin 1).

The amplified signals from the power amplifier (IC1, pin 4) pass through the APC detector (D7, D8), antenna switching circuit (D9) and low-pass filter (L15, L16, L78, C70–C72), and is then applied to the antenna connector.

Collector voltage for the driver (Q12) and control voltage for the power amplifier (IC1, pin 2) are controlled by the APC circuit to protect the power module from a mismatched condition as well as to stabilize the output power.

4-2-5 VHF APC CIRCUIT

The APC circuit protects the power amplifier from a mismatched output load and stabilizes transmit output power.

The APC detector circuit (L12, D7, D8) detects forward signals and refrection signals at D7 and D8 respectively. The combined voltage is at a minimum level when the antenna impedance is matched at 50 Ω and is increased when it is mismatched.

The detected voltage is applied to the APC amplifier (IC5, pin 3) and compared with a reference voltage which is supplied from the CPU (IC19, pin 68–pin 75) as a D/A control signal.

When antenna impedance is mismatched, the detected voltage exceeds the reference voltage. The output voltage of the APC amplifier (IC5, pin 4) controls the bias voltage of the power module (IC1) and drive amplifeir (Q12) to reduce the output power via the APC controller (Q30, Q31).

4-2-6 UHF MODULATION CIRCUIT

Audio signals from the splatter filter (IC23a) pass through the frequency deviation control (R78), and are then applied to the modulation circuit (D20) to change the reactance of D20 and modulate the oscillated signal at the U-VCO circuit (Q20, Q21). The VCO output is amplified at the buffer amplifiers (Q22, Q24), and is then applied to the T/R switching circuit (D23) via the low-pass filter (L33, C153, C154).

4-2-7 UHF DRIVE AMPLIFIER CIRCUIT

The VCO signals from the T/R switch (D23) are amplified at the buffer-amplifier (Q27), pre-drive amplifier (Q28) and drive (Q29, D24) amplifier to obtain an approximate 400 mW signal level. The amplified signal is then applied to the RF power amplifier (IC4).

4-2-8 UHF POWER AMPLIFIER CIRCUIT

IC4 is a power module which has amplification output capabilities of about 50 W.

The RF signal from the drive amplifier (Q29) is applied to IC4 (pin 5). The amplified signal from the power amplifier (IC4, pin 1) is passed through the antenna switching circuit (D27) and is then applied to the antenna connector via a bandpass filter (L42–L45, L82, C186–C190, C467, C493).

4-2-9 UHF APC CIRCUIT

The APC detector circuit (D25 and D26) detects forward signals and refrection signals respectively. The combined voltage is at a minimum level when the antenna is matched at 50 Ω and increases when it is mismatched.

The combined voltage is applied to the APC amplifier (IC5, pin 3), and the power setting voltage from the CPU (IC19, pin 68–pin 75) as a D/A control signal is applied to the other input (IC5, pin 1) for the reference.

The output voltage from IC5 (pin 4) is applied to the APC control circuit (Q30, Q31) to control the bias voltage of the PA module (IC4) and drive amplifier (Q29).

4-3 PLL CIRCUITS

4-3-1 GENERAL

A PLL circuit provides stable oscillation of the transmit frequency and the receive local frequency. The PLL circuit compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by a crystal oscillator and the divided ratio of the programmable divider. IC2 is a dual PLL IC which controls both VCO circuits for VHF and UHF.

4-3-2 VHF LOOP

The generated signal at the V-VCO (Q4, Q5, D3) enters the PLL IC (IC2, pin 6) via buffer-amplifiers (Q6, Q8) and is divided at the programmable divider section and is then applied to the phase detector section.

The phase detector compares the input signal with a reference frequency, and then outputs the out-of-phase signal (pulse-type signal) from pin 8.

The pulse-type signal is converted into DC voltage (lock voltage) at the loop filter (Q99, Q100, R531, C476–C478), and then applied to the V-VCO to stabilize the oscillated frequency.

4-3-3 UHF LOOP

The generated signal at the U-VCO (Q20, Q21, D20, D21) enters the PLL IC (IC2, pin 15) via buffer-amplifiers (Q22, Q23) and is divided at the programmable divider section and is then applied to the phase detector section.

The phase detector compares the input signal with a reference frequency, and then outputs the out-of-phase signal (pulse-type signal) from pin 13.

The pulse-type signal is converted into DC voltage (lock voltage) at the loop filter (Q101, Q102, R538, C481, C483), and then applied to the U-VCO to stabilize the oscillated frequency.

4-4 POWER SUPPLY CIRCUITS

• VOLTAGE LINE

Line	Description
HV	The 13.8V external DC power from the power connector.
13.8V	The same voltage as the HV line which is controlled by the power switching circuit (Q74, Q75). When the [POWER] switch is pushed, the CPU outputs the “PCTRL” control signal to the power switching circuit to turn the circuit ON.
C5V	Common 5 V for the CPU converted from the HV line by the C5V regulator circuit (IC15). The circuit outputs the voltage regardless of the power ON/OFF condition.
PLL5V	Common 5 V produced from the C5V at the PLL5V regulator circuit (Q13, Q14) using control signal from 8V line.
8V	Common 8 V converted from the 13.8V line by the 8V regulator circuit (IC14).
VT8V	VHF transmit 8 V converted from the 8V line at the VT8V regulator circuit (Q9, Q10).
UT8V	UHF transmit 8V converted from the 8V line at the UT8V regulator circuit (Q25, Q26).
VR8V	Receive VR8V produced from the 8V line at the V-BIAS selector (Q34, Q35).
4R8V	Receive 4R8V produced from the 8V line at the U-BIAS selector (Q34, Q36).
UR8V	Receive UR8V produced from the 4R8V line at the UR8V switching circuit (D28, D29).