## 1. MICROPHONE GAIN SELECT CIRCUIT

The audio signals from the microphone are divided by R209, R219 and R221. The divide ratio is changed by turning Q81 ON/OFF to select the desired microphone gain in 4 steps.

## 2. MICROPHONE AMPLIFIER

The audio signals from the microphone are amplified by IC13b and IC3a. The audio signals are obtained +6 dB/oct of frequency response (pre-emphasis) by R105 and C133 (beside of IC3a), and are removed 3 kHz and higher components.

## 3. VOX AMPLIFIER

The output signals of the microphone AMP (IC13b) are applied to the VOX AMP (IC13a). The output signals of the VOX AMP are rectified by D31 and applied to the A/D port of the CPU. The CPU switches transmitting and receiving according to the applied signal level.

## 4. MUTE/FILTER SW

IC4 is a analog SW which selects the destination of the AF signals; MIC AMP to modulation circuit, RX AF HPF to D/A converter, etc.

## 5. SPLATTER FILTER

IC3c is a splatter filter which also composes the MIC signals and tone signals (CTCSS, DTCS, DTMF, 750Hz tone). And also functions as an LPF while receiving.

## 6. SIGNALING (ENCODING)

Tone signals for signaling are output from the CPU (IC8); DTMF and 1750Hz tone signals from pin3, CTCSS and DTCS from pin 4. These tone signals are applied to the D/A converter (IC10). The CTCSS and DTCS signals are applied to the VCO and also applied to the PLL reference signal oscillator for reliable modulation. The DTCS signals are level-adjusted by the D/A converter (IC10) before being applied to the PLL reference signal oscillator.

## 7. SIGNALING (DECODING)

The CTCSS and DTCS signals contained in the demodulated signals from the IF IC are passed through the LPF (Q53) and applied to the CPU for decoding.

## 8. RX AF CIRCUITS

The demodulated AF signals from the IF IC are passed through the HPF (IC3d) to remove unwanted signals. The filtered AF signals are passed through the LPF (R452, R453, C783) and the analog SW (IC4), then applied to the LPF as the mix AMP (IC3c) which composes beep sounds and DTMF tone (for monitoring). The output signal of the LPF (IC3c) are applied to the D/A converter (IC10) for audio level (=volume) adjustment.

## 9. AF POWER AMPLIFIER

The level-adjusted AF signals from the D/A converter (IC10) are amplified by the AF AMP (IC5) then applied to the speaker. IC5 is a BTL audio amplifier and its output signals are; single-end output when external speaker is connected, or BTL output when internal speaker is used.

## 10. D/A CONVERTER

The parameters such as the temperature which is detected by the thermostat (R182), battery voltage, frequency, etc. is gathered up to the CPU. The CPU analyzes these parameters and controls RF BPFs, deviation, TX output power, squelch sensitivity and audio level, using D/A converter (IC10).

## 11. POWER SUPPLY CIRCUITS

The regulated 5 V from IC12 is supplied to the CPU.

The power supply circuit (Q55, Q56, Q78) provide power supply “SW5V” while the transceiver is activated.

Q21 and Q22 are the power supply switching circuit for each circuit.

The power supply for the AF AMP is independent, and composed by Q15 and Q16.

## 12. PLL/VCO CIRCUITS

The oscillation frequency of the VCO is determined by the variable capacitors (D59, D60), L44, L45. C460. C457 and C456. While transmitting, D58 is ON, and C461 and C462 provide the RF path to the GND. This shifts the oscillating frequency to higher. Adding modulation signals to D61 provides frequency modulation.

The output signals of the VCO are passed through the buffer AMP (Q6), and applied to the buffer AMP (Q5: for PLL feedback) or the buffer AMP (Q4: LO AMP).

The output signals of the buffer AMP (Q5: for PLL feedback) are applied to the PLL IC (IC1). The applied signals are phase-compared with the reference frequency signal from

the TCXO (X1), and the resulting signal is output from the PLL IC as the charge pump output signal, then applied to the VCO as the lock voltage after being passed through the loop filter. Q58 shifts the time constant of the loop filter for shorter PLL lockup time when the transceiver needs to.
The power supply circuit (Q11) of the VCO which is as a ripple filter too, has the capability of fast ON/OFF switching operation that works even when the transceiver is in the power save mode.

### 13. YGA/PA

While transmitting, the diode SW (D3) is ON and it feeds the LO signal to the YGR circuit. The LO signal is amplified by Q3, driver AMP FET (Q2) and final AMP FET (Q1) to obtain TX output power.

### 14. APC CIRCUIT

The TX signal level is detected at the LPF (L4, C287, C278) by being rectified by D32 and D33 to be converted into the DC voltage whose voltage is corresponding to the RF power (TX power) level. The rectified voltage is applied to the APC AMP (IC3b), and compared with the power setting voltage from the D/A converter "T3." The resulting signal of the APC AMP (IC3b) controls the gate voltages of Q1 and Q2 to control the TX output power stable.

### 15. ANT SW /LPF

The TX signal is passed through the TX/RX SW (ANT SW) and the LPF which removes major harmonics, then fed to the antenna.

### 16. RF BPF

The RX signals from the antenna are passed through the LPF which removes major harmonics in transmitting, and the TX/RX SW (ANT SW), then applied to the RX F circuit.
The RX signals are filtered by the BPF (L16, C80, D9) and amplified by the low-noise RF AMP (Q12). The amplified RX signals are filtered by another BPF (L18, L19, D11, C94, C91, C97) to remove image frequency signals, then applied to the 1st mixer (Q13).
Total of three BPFs are tuned to the RX frequency by the adequate tuning voltage from the D/A converter.

### 17. 1ST MIXER

The output signal of the VCO is buffer-amplified by Q4, passed through the diode SW (D4) and the step-up BPF (C100, C101, C102, L21, L29), then applied to the 1st mixer (Q13) as the 1st LO signal. The RX signals from the BPF are mixed with the 1st LO signals to be converted into the 21.70 MHz 1st IF signal.

### 18. 1st IF AMP

The 21.70 MHz 1st IF signal is filtered by the crystal filters (FI1 and FI3), and amplified by the 1st IF AMP (Q14), then applied to the IF demodulator IC (IC2). D62 is a diode which limits the IF signal level.

### 19. IF DET

The reference frequency signal is buffer-amplified by Q7, and applied to the pin 2 of the IF IC (IC2) as the 2nd LO signal, then mixed with the 1st IF signal.
The resulting signal is output from the pin 3 as the 450 kHz 2nd IF signal, and filtered by the ceramic filter (FI2) to remove unwanted signals. The 2nd IF signal is applied to the IF IC (IC2) from pin 5, and demodulated at the internal detector circuit. The detector circuit is a quadrature detector which uses X3 as the phase shifter.
When the RX mode (FM/FM-N) is changed, the detected signal level is also changed. To compensate this, Q83 changes the value of dumping resister of X3.
The demodulated signal is output from pin 9.

### 20. NOISE SQUELCH CIRCUIT

The demodulated signals from the IF IC (IC2) are routed to each circuit; LPF for tone decoding, HPF for RX AF signal and D/A converter (IC10) for noise squelch threshold adjustment.
The output signals of the D/A converter (IC10) are applied to the noise AMP. The noise AMP is an active high-pass filter which is composed by the OP. AMP in the IC2 and some external R and C components, and amplifies signals that are higher than voiceband.
The output signals of the noise AMP are applied to the noise detector circuit in the IC2, and output from pin 13 as the noise pulse signal. The noise pulse signal is applied to the CPU that controls the squelch open/close.

## 21.CLOCK SHIFT CIRCUIT

D13 shifts the CPU clock frequency by changing the capacitive load of the clock oscillator (X2).

## 22. LCD BACKLIGHT CONTROL CIRCUIT

The current regulator circuit (Q25) turns LEDs (DS2 ,DS3) ON/OFF.

## 23. REMAINING BATTERY VOLTAGE DETECTOR CIRCUIT

The remaining battery voltage is detected by applying voltage which is divided by R29 and R31 to the A/D port of the CPU.

## 24. RESET CIRCUIT

IC11 is a reset IC which resets the CPU when the voltage “VDD” crosses the threshold voltage by applying the reset pulse signal (from pin 4) to the CPU.