6.2 Description of the circuitry and devices provided for determining and stabilizing frequency, for suppression of spurious radiation, for limiting modulation, and for limiting power

6.2.1 System Configuration

Fig.6.2.1.1 shows the configuration of FS-1570.

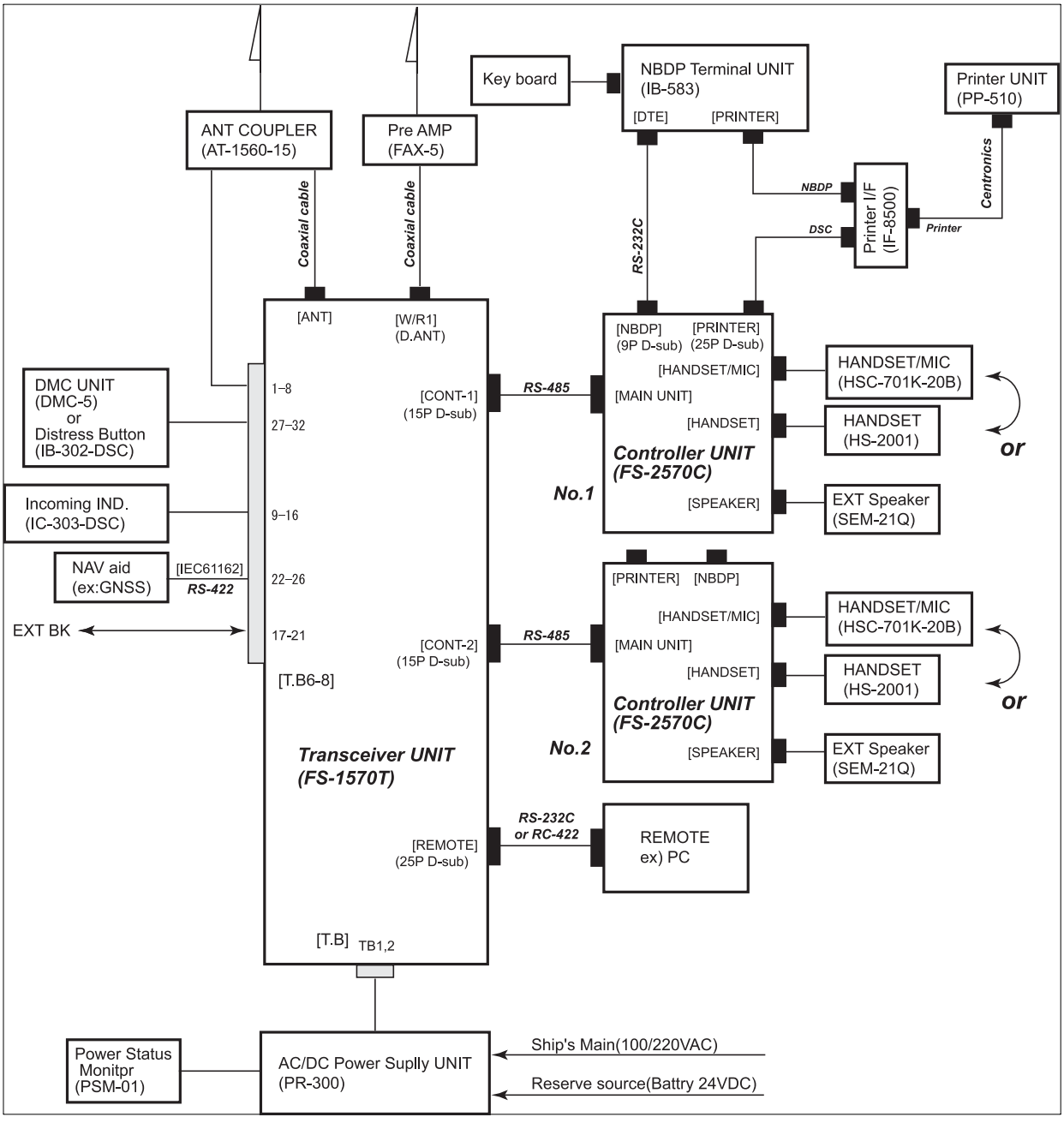


Fig. 6.2.1.1 Configuration of FS-1570

6.2.2 Unit Description

6.2.2.1 Transceiver unit, FS-1570T

Fig.6.2.2.1-1 shows the block diagram of the transceiver unit, FS-1570T.

- DSP board (05P0751) is needed for NBDP communication.
- During the scanning reception of DSC general frequencies by using TX/RX board, radiotelephone and NBDP cannot be used.

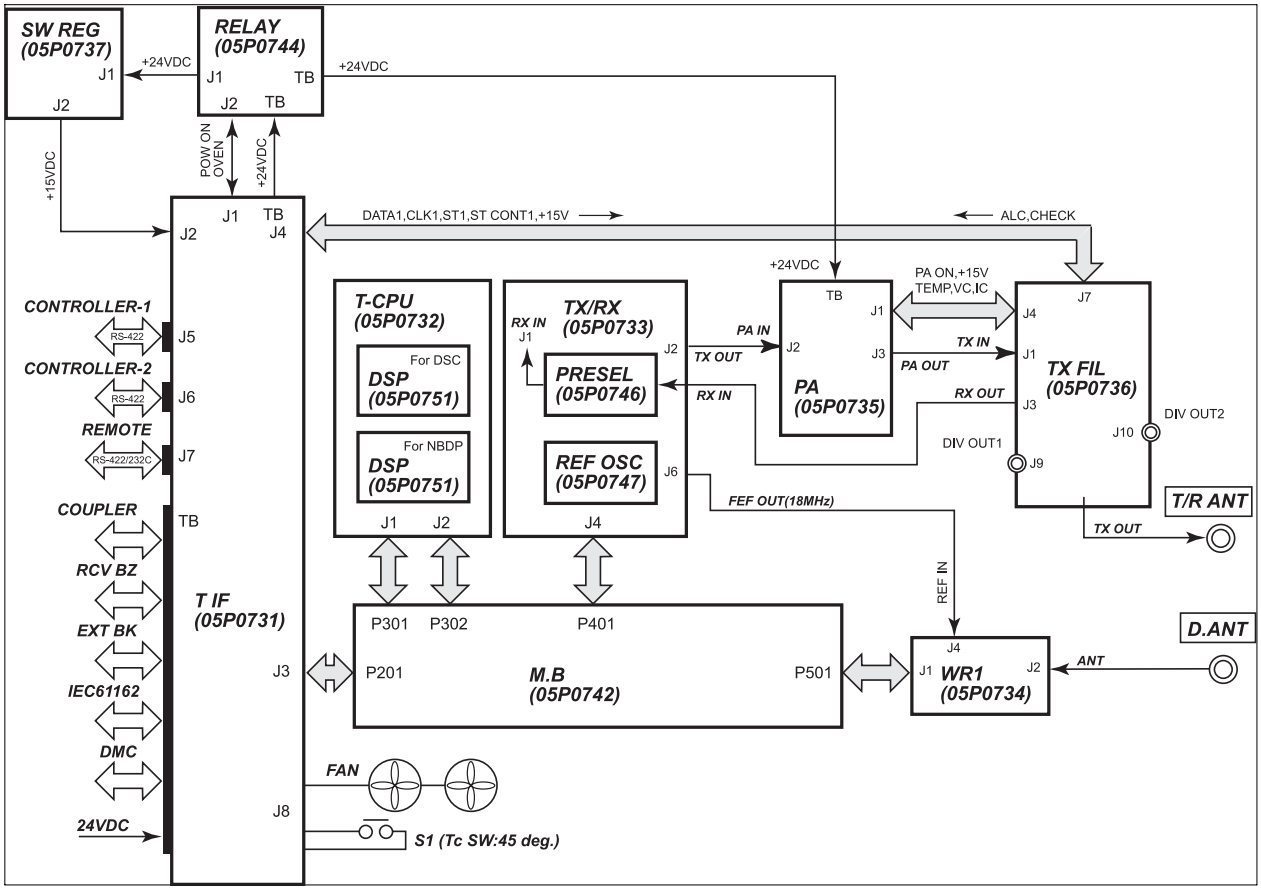


Fig.6.2.2.1-1 Block diagram of FS-1570T

Boards in Transceiver unit

Table 6.2.2.1-1 lists the function of each board in the transceiver unit.

Table 6.2.2.1-1 Boards in Transceiver unit

Board	Type	Function
T-CPU	05P0732	1) Consisting of Main CPU, SUB CPU-1 (I/F), SUB CPU-2 (I/F) and associated circuits.
DSP (For DSC)	05P0751	1) Consisting of DSP, Modem and Flash ROM. 2) DSC program is stored in EEROM. 3) The serial communication is made between the DSC DSP and Main CPU.
DSP (For NBDP)	05P0751	1) Consisting of DSP, Modem and Flash ROM 2) NBDP program is stored in EEROM. 3) NBDP DSP communicates with Main CPU in parallel.
TX/RX	05P0733	1) Consisting of modulator and demodulator for DSC, NBDP and VOICE signals, and local oscillators. AF input/output signal: 600 Ω/ -10 dBm Output power: 0.5 W The board outputs S, RXAF, TXAF and TXOUT (RF) signals to T-CPU board for checking.
PRESEL	05P0746	1) Consisting of 5 filters. 2) 1.45 to 4.99 MHz filter consists of tuning circuits. An adequate capacitor is selected by a relay for the selected frequency. Other four filters is a band pass filter.
REF OSC	05P0747	1) This board is an 18 MHz reference oscillator. 2) The output is sent to T/R and W/R1 boards. When the transceiver unit is supplied 24V, +12 V (oven voltage) is supplied to the oven. TEMP signal is output to T-CPU board. If the TEMP signal is lower than the designed value, the transceiver does not transmit.
W/R1	05P0734	1) This board is a DSC distress safety receiver, consisting of RF amplifier, a demodulator, an AF amplifier and local oscillators. 2) The board uses 18 MHz reference signal from REF OSC board. For self-test, 18 MHz signal is applied to the antenna circuit (RF connection). 3) The T-CPU identifies W/R board with INST signal.
PA	05P0739	1) Two stage push-pull amplifier outputs 150 W signal. Power gain: 27 dB 2) Check signal output to T-CPU: TEMP, VC and IC

Board	Type	Function
TX FIL	05P0736	1) Consisting of 7 band pass filters. 2) The filter eliminates and suppresses unwanted signal generated at PA. Check signal output to T-CPU: IN-Vr/Vf, OUT-Vr/Vf and ALC
SW REG	05P0737	Input voltage: 24 VDC Output voltage: +15 VDC (5 A max) Switching frequency: 220 kHz.
RELAY	05P0744	Consisting of; 1) On/Off relay in 24 V lines for PA 2) 25 A breakers in 24 V lines for PA 3) +12 V AVR 4) 16 V low-voltage protector 5) 35 V over-voltage protector
T-IF	05P0731	Consisting of; 1) Connectors and terminal board for external equipment 2) Amplifiers for LINE IN and LINE OUT signals.
MB	05P0742	Mother board

6.2.2.2 Control unit, FS-2570C

Two control units can be connected to the transceiver unit. The system is turned on and off by the control unit connected to [CONT-1] port on the transceiver unit. The control unit communicates with the transceiver unit, using RS-485. The LINE IN/OUT level between two units is 600 Ω/-10 dBm.
The printer, PP-510 is connected to the control unit for printing DSC and NBDP messages. When IB-581/583 is used as a NBDP terminal, the printer is connected via IF-8500.

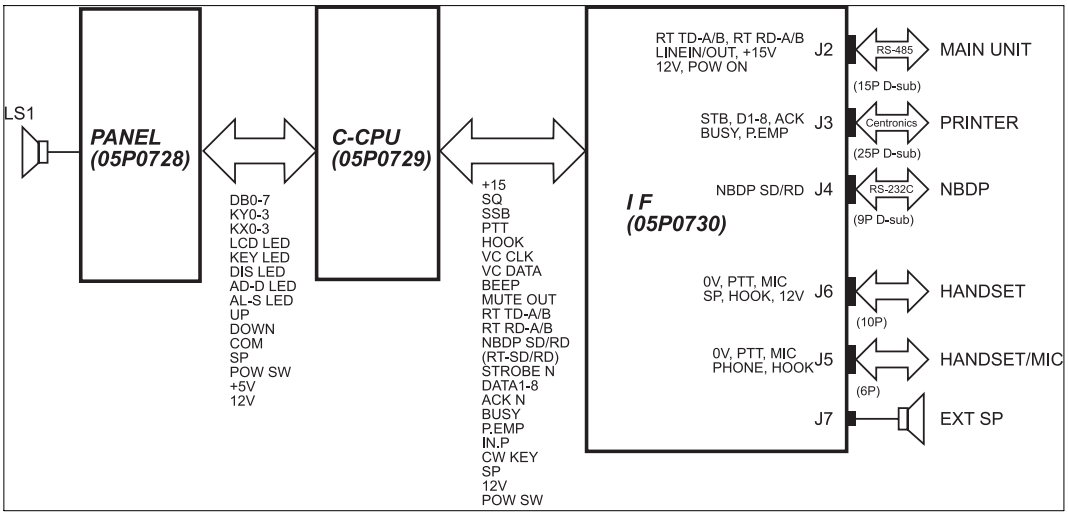


Fig.6.2.2.2-1 Block diagram of FS-2570C

Table 6.2.2.2-1 lists the boards in FS-2570C.

Table 6.2.2.2-1 Boards in FS-2570C

Unit	Board	Type	Function
FS-2570C	C-IF	05P0730	Consisting of; 1) Connectors for external units 2) Volume adjuster 3) Audio power amplifier, TA7752AP
	C-CPU	05P0729	The C-CPU communicates with; 1) TR unit, using RS-485 2) NBDP terminal, using RS-232C 3) Printer, using Centronics 4) Hook and PTT signal detectors
	PANEL	05P0728	Keys and LCD

6.2.2.3 NBDP Terminal unit, IB-581/583 (Option)

IB-583 is a NBDP terminal newly developed for FS-1570. The terminal program for IB-583 differs from one for IB-581. The operation of IB-583 is almost the same as one of DP-6.

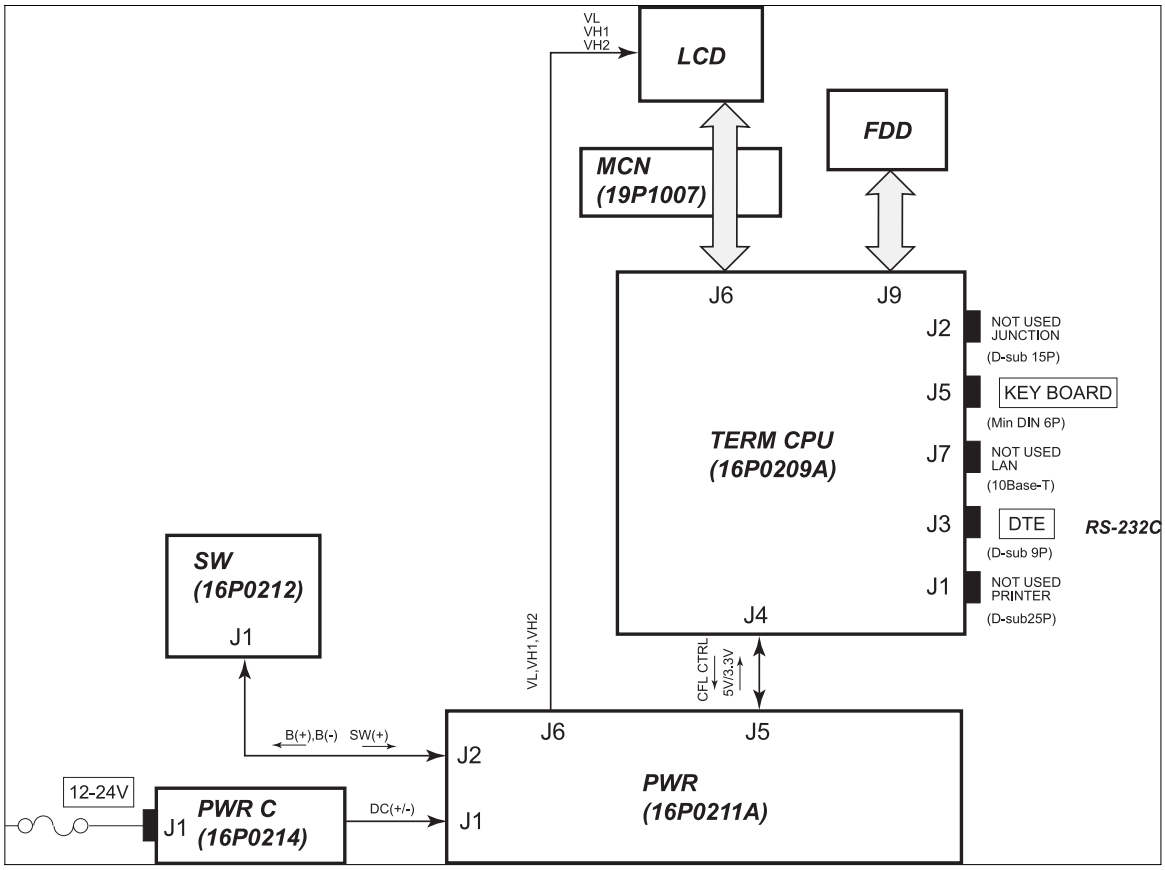


Fig.6.2.2.3-1 Block diagram of IB-583

Table 6.2.2.3-1 Boards in IB-583

Unit	Board	Type	Function
IB-583	TERM CPU	16P0209A	1) Controlling display. 2) Communicating with FS-2570C (RS-232C).
	SW	16P0212	Power switch circuit
	PWR	16P0211A	Generates 6.5 V, 3.3 V, 5 V and power for LCD
	PWR C	16P0214	Power connector and filter
	LCD		NL6448BC33-46
	FDD		JU-226A032FCK2149 (For 2HD)

6.2.2.4 Antenna coupler unit, AT-1560-15

Fig.6.2.2.4-1 shows the block diagram of the AT-1560-15 (for 150 W SSB). When the system is switched off, the antenna is grounded via the dummy board.

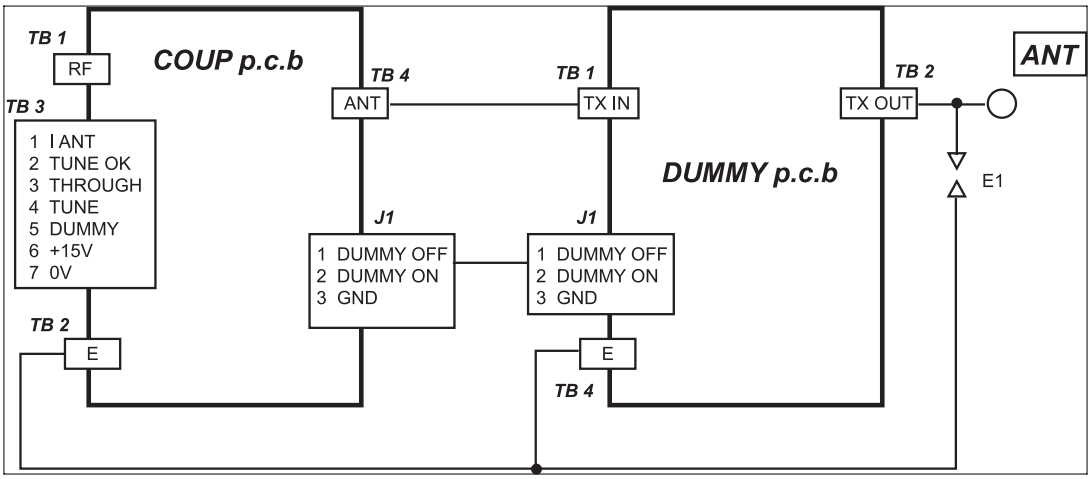


Fig.6.2.2.4-1 Block diagram of AT-1560-15

Table 6.2.2.4-1 Boards in AT-1560-15

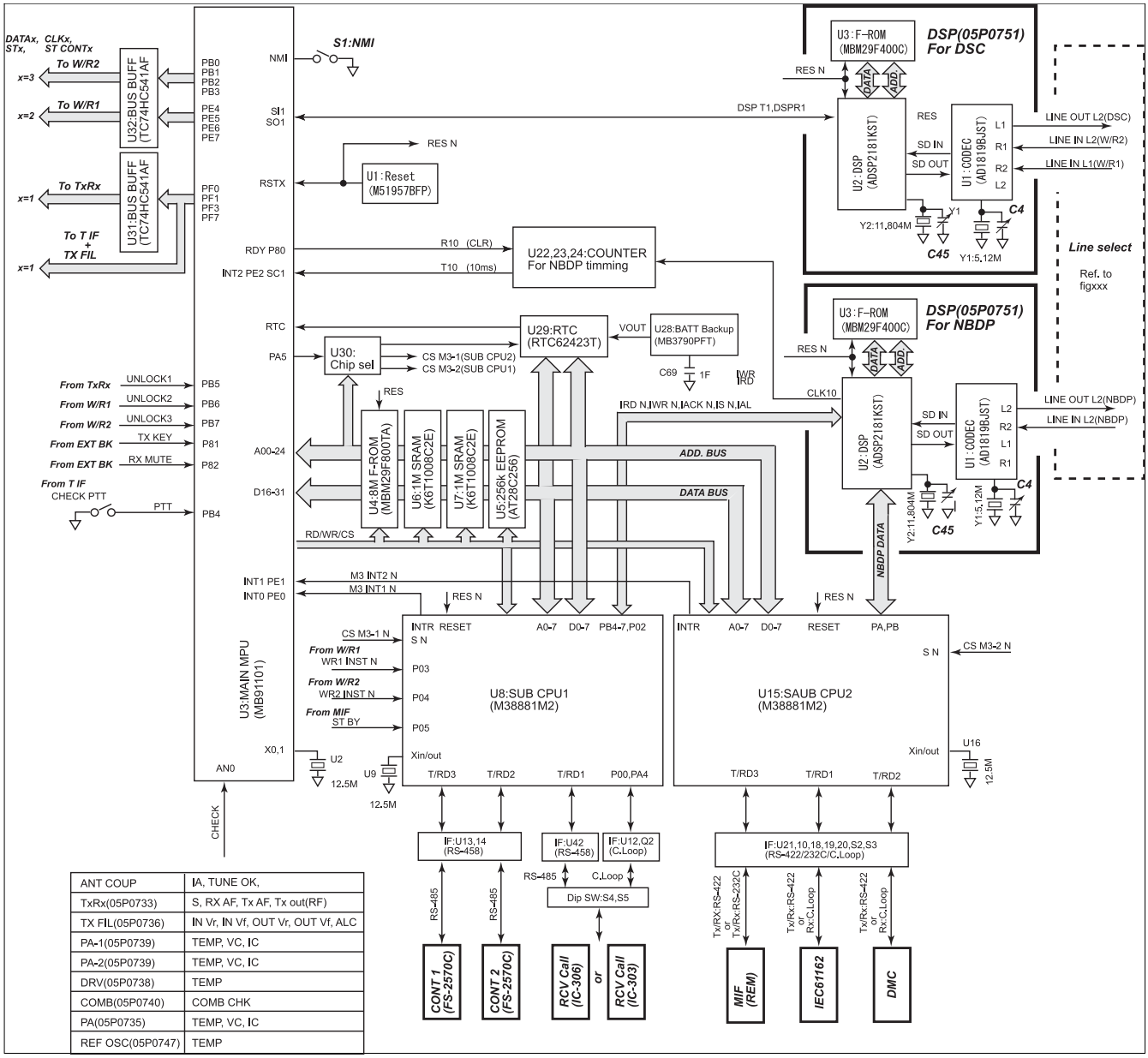
Board	Type	Function
COUP	05P0528	Antenna matching, capability of 7 m antenna connection
DUMMY	05P0543	10 Ω+250 pF, 100 W dummy load

6.2.3 Board description

6.2.3.1 Transceiver unit, FS-1570T

(1) T-CPU board （05P0732）

Fig.6.2.3.1-1 shows the block diagram of the T-CPU board.



ANT COUP	IA, TUNE OK,
TxRx(05P0733)	S, RX AF, Tx AF, Tx out(RF)
TX FIL(05P0736)	IN Vr, IN Vf, OUT Vr, OUT Vf, ALC
PA-1(05P0739)	TEMP, VC, IC
PA-2(05P0739)	TEMP, VC, IC
DRV(05P0738)	TEMP
COMB(05P0740)	COMB CHK
PA(05P0735)	TEMP, VC, IC
REF OSC(05P0747)	TEMP

Fig.6.2.3.1-1 Block diagram of T-CPU （05P0732）

(1.a) Function of CPU

Three CPUs, 32-bit MAIN CPU, 8-bit SUB CPU-1 (I/O) and 8-bit SUB CPU-2 (I/O) work as shown in Table 5.3.1.

Table 6.2.3.1-1 Function of CPU

CPU	Function
MAIN CPU (U3, MB91101)	1) Communicates with SUB CPU-1, SUB CPU-2, FS-2570C, MIF interface units and DMC 2) Encoding and decoding of DSC and NBDP messages 3) Decides the timing for NBDP communication 4) Interfaces with DSC DSP and NBDP DSP 5) Reads check signals 6) Controls external BK, antenna coupler and IC-302/IC-303-DSC 7) Receives NMEA signal
SUB CPU-1 (I/O) (U8, M38881M2)	1) Communicates with Main CPU 2) Interfaces with Incoming Indicator, No.1 and No.2 FS-2570C 3) Detects the absence of W/R1 and W/R 2
SUB CPU-2 (I/O) (U15, M38881M2)	1) Communicates with Main CPU 2) Interfaces with IEC61162 device, DMC-5, IC-302, NBDP DSP and MIF devices

(1.b) Memory

Table 6.2.3.1-2 shows the memory contents.

Table 6.2.3.1-2 Memory contents

Memory	Contents
8 Mbit Flash ROM (U4, MBM29F800TA)	1) RT, DSC and NBDP programs 2) Default settings of DSC system setup menu 3) Default settings of RT system setup menu 4) ITU channels
256 kbit EEROM (U5, AT28C256)	1) Settings of DSC system setup menu 2) Settings of RT system setup menu 3) MMSI and model 4) User channels 5) Communication log
1 Mbit SRAM (U6 and U7, K6T1008C2E)	Used by MAIN CPU as working memory

(1.c) Control signals

Control signals generated by the T-CPU are sent to TX FIL, T-IF, TX/RX and W/R boards after serial-to-parallel conversion using shift registers in each board. Data 1 is delivered to TX FIL, TX-IF and TX/RX boards, Data 2 to W/R1 board and Data 3 to W/R2 board. Tables 6.2.3.1-3 to 6.2.3.1-6 list the signals derived from Data 1 to 3.

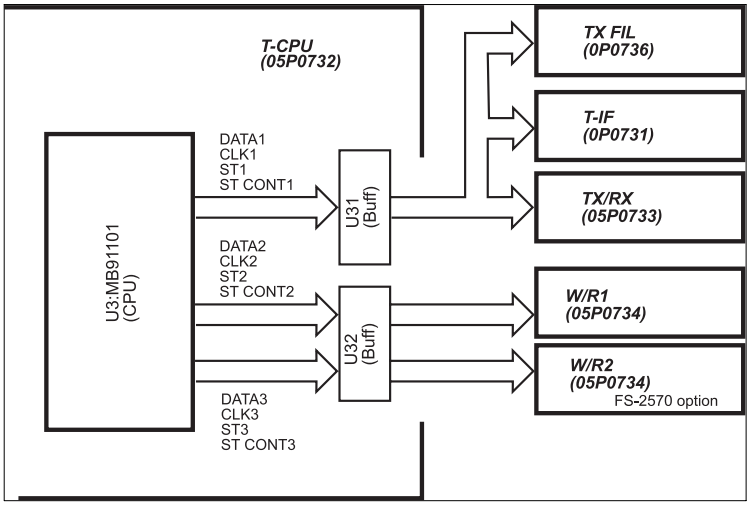


Fig.6.2.3.1-2 Output circuit of Control signals

Table 6.2.3.1-3 Signals generated by DATA 1 on TX FIL Board

TX FIL	Pin No. & Name		Order of execution	Signal name	Function
U1	-		**1**-8	N.C	Not used
U2	-		9-16	N.C	Not used
U4	#16	Q1	17	PA ON1, PA ON2	Turns on/off Power amplifier on PA board (05P0735)
	#15	Q2	18	DA ON	Turns on/off Driver on DRV board (05P0738)
	#14	Q3	19	N.C	
	#13	Q4	20	A	Selects following check signals connected to U5 and U6 in order 1) ALC, CHK, OUTVf, OUTVr, INVf and INVr from TX FIL (05P0736) 2) VC1, IC1 and TEMP1 from PA (05P0735) 3) VC1, IC1, TEMP1, VC2, IC2 and TEMP2 from PA (05P0739) 4) DA TEMP from DRV (05P0738) 5) COMB CHK from COMB (05P0740)
	#12	Q5	21	B	
	#11	Q6	22	C	
	#10	Q7	23	INH 1	
	#9	Q8	24	INH 2	
U3	#16	Q1	17	18 to 30 MHz LPF	Selects low pass filter on TX FIL board (05P0736)
	#15	Q2	18	12 to 18 MHz LPF	
	#14	Q3	19	8 to 12 MHz LPF	
	#13	Q4	20	5.4 to 8 MHz LPF	
	#12	Q5	21	3.6 to 5.4 MHz LPF	
	#11	Q6	22	2.4 to 3.6 MHz LPF	
	#10	Q7	23	1.6 to 2.4 MHz LPF	
	#9	Q8	24	BK RL CONT	Switches 50 ohm BK relay, K15 on TX FIL board (05P0736)

Table 6.2.3.1-4 Signals generated by DATA 1 on TX/RX board

TX/ RX	Pin No. & Name		Order of execution	Signal name	Function
U1	#15	QA	1	ST1 (NOR: ST CONT1)	ST signal to U44 for VCO frequency band selection
	#1	QB	2	ST2	ST signal to DDS (U42)
	#2	QC	3	ST3	ST signal to DDS (U45)
	#3	QD	4	ST (NOR: ST CONT1)	Used to generate latch timing signal for U3 to U8
	#4	QE	5	ST (NOR: ST CONT1)	ST signal to PLL (U43)
	#5	QF	6	N.C	
	#6	QG	7	N.C	
	#7	QH	8	N.C	
U2			9-16	N.C	Not used
U3	#15	QA	17	POWER data-1	D/A converted by R88 and sent to Automatic Power Control (APC) circuit to control output power
	#1	QB	18	POWER data-2	
	#2	QC	19	POWER data-3	
	#3	QD	20	POWER data-4	
	#4	QE	21	POWER data-5	
	#5	QF	22	POWER data-6	
	#6	QG	23	POWER data-7	
	#7	QH	24	POWER data-8	
U4	#15	QA	25	**N.C**	
	#1	QB	26	**N.C**	
	#2	QC	27	RF GAIN data-1	D/A converted by R138 for RF AGC voltage control
	#3	QD	28	RF GAIN data-2	
	#4	QE	29	RF GAIN data-3	
	#5	QF	30	RF GAIN data-4	
	#6	QG	31	RF GAIN data-5	
	#7	QH	32	RF GAIN data-6	
U5	#16	Q1	33	PR8	Selects capacitors in the tuning circuit for 1.45 to 4.99 MHz band on PRESEL board (05P0746)
	#15	Q2	34	PR7	
	#14	Q3	35	PR6	
	#13	Q4	36	PR5	
	#12	Q5	37	PR4	
	#11	Q6	38	PR3	
	#10	Q7	39	PR2	
	#9	Q8	40	PR1	
U6	#16	Q1	41	BPF2 (1.45 to 4.99 MHz)	Selects a filter (BPF) on PRESEL board (05P0746)
	#15	Q2	42	BPF5 (18 to 30 MHz)	
	#14	Q3	43	BPF4 (8 to 18 MHz)	
	#13	Q4	44	BPF3 (5 to 8 MHz)	
	#12	Q5	45	BPF1 (0.1 to 1.45 MHz)	
	#11	Q6	46	N.C	
	#10	Q7	47	N.C	
	#9	Q8	48	N.C	

(Cont'd)

TX/ RX	Pin No. & Name		Order of execution	Signal name	Function
U7	#16	Q1	49	TX	Generates TX signal (+12 V)
	#15	Q2	50	RX	Generates RX signal (+12 V)
	#14	Q3	51	N J3E	Switches between J3E and H3E demodulators
	#13	Q4	52	N H3E	
	#12	Q5	53	N.C	
	#11	Q6	54	N: Narrow (FL4: 450 Hz)	Selects bandwidth of IF filter (455 kHz)
	#10	Q7	55	M: Middle (FIL3: 2.4 k)	
	#9	Q8	56	W: Wide (FIL2: 6 k)	
U8	#16	Q1	57	AGC FAST	Sets AGC decay time to FAST
	#15	Q2	58	N.B CONT	Switches on/off Noise Blanker (U16)
	#14	Q3	59	AGC OFF	Sets AGO to OFF
	#13	Q4	60	TX H3E	Adds carrier signal at H3E transmission
	#12	Q5	61	A	Selects following check signals connected to U9. 1) S, RX AF CHK, TX AF CHK and TX OUT CHK from TX/RX (05P0733) 2) TEMP from REF OSC (05P0747)
	#11	Q6	62	B	
	#10	Q7	63	C	
	#9	Q8	64	INH	
U43	#5			PLL data	PLL data for PLL IC (U43)
U42	#8			1DDS data	DDS data for DDS IC (U42)
U45	#8			2DDS data	DDS data for DDS IC (U45)
U44	#16	Q1	17	BAND-1	Selects PLL Band, 100 kHz to 6 MHz
	#15	Q2	18	BAND-2	Selects PLL Band, 6 to 13.5 MHz
	#14	Q3	18	BAND-3	Selects PLL Band, 13.5 to 21.5MHz
	#13	Q4	20	BAND-4	Selects PLL Ban, 21.5 to 30 MHz
	#12	Q5	21	H/L	Divides each PLL band into two bands
	#11	Q6	22	N.C	
	#10	Q7	23	N.C	
	#9	Q8	24	TEST	Outputs receiver self-test signal (18 MHz)

Table 6.2.3.1-5 Signals generated by DATA 1 on T-IF board

T-IF	Pin No. & Name		Order of execution	Signal name	Function
U2			1-8	N.C	
U3	#15	QA	9	N.C	
	#1	QB	10	N.C	
	#2	QC	11	U4 ST (NOR: ST CONT1)	Used to generate latch signal for U4 by NOR gate U12 with ST CONT1 signal
	#3	QD	12	U5 ST (NOR: ST CONT1)	Used to generate latch signal for U5 by NOR gate U12 with ST CONT 1 signal
	#4	QE	13	N.C	
	#5	QF	14	N.C	
	#6	QG	15	N.C	
	#7	QH	16	N.C	
U4	#16	Q1	17	N.C	
	#15	Q2	18	N.C	
	#14	Q3	19	N.C	
	#13	Q4	20	N.C	
	#12	Q5	21	N.C	
	#11	Q6	22	MIF AF	
	#10	Q7	23	INT C	Selects LINE-IN signal from No.1 or No.2 FS-2570C, using analog switch U8 (TX AF OUT signal)
	#9	Q8	24	REM 1__2	Selects LINE-IN signal from No.1 or No.2 FS-2570C, using analog switch U8 (LINE OUT signal)
U5	#16	Q1	17	TX KEYED	Controls External BK, isolated with photocoupler U14, Driver Q4 provided
	#15	Q2	18	DUMMY	Controls antenna coupler
	#14	Q3	19	TUNE	
	#13	Q4	20	THROUGH	
	#12	Q5	21	A	Selects IA and TUNE OK signals from the coupler, using U6
	#11	Q6	22	B	
	#10	Q7	23	C	
	#9	Q8	24	INH	

Table 6.2.3.1-6 Signals generated by DATA 2 on W/R board

W/R1	Pin No. & Name		Order of execution	Signal name	Function
U502				PLL data	PLL data for PLL IC (U502)
U504	#15	QA	1	DDS2 LOAD A	LOAD signal for U506 (DDS2, 456.7 kHz)
	#1	QB	2	DDS1 LOAD B	LOAD signal for U501 (DDS1, 6 MHz PLL Ref)
	#2	QC	3	U503 ST (NOR: ST CONT2)	Used to generate latch signal for U503 by NOR gate ST CONT2 signal
	#3	QD	4	U502 ST (NOR: ST CONT2)	Used to generate latch signal for U502 by NOR gate ST CONT2 signal
	#4	QE	5	N.C	
	#5	QF	6	N.C	
	#6	QG	7	N.C	
	#7	QH	8	N.C	
U503	#16	Q1	9	BAND-1	PLL BAND selection （1.6 to 6 MHz）
	#15	Q2	10	BAND-2	PLL BAND selection （6 to 13.5 MHz）
	#14	Q3	11	BAND-3	PLL BAND selection （13.5 to 21.5 MHz）
	#13	Q4	12	BAND-4	PLL BAND selection （21.5 to 27.5 MHz）
	#12	Q5	13	H/L	Divides each band into 2 bands
	#11	Q6	14	TEST	Outputs W/R-1 self-test signal (18 MHz)
	#10	Q7	15	LPF 1	RF filter selection （1.6 to 13.2 MHz）
	#9	Q8	16	LPF 2	RF filter selection （13.2 to 27.5 MHz）

(1.d) Digital Signal Processor (DSP)

Fig.6.2.3.1-3 shows the DSP input/output circuits.

DSP (05P0751) boards for NBDP and DSC are the same in hardware, but different in software. The LINE signals (AF) are switched by the analog switches. DSC distress safety receiver (W/R 1) is directly connected to DSP board for continuous watch. The MIC signal (AF-IN) from T-IF board is sent to TX/RX board through the analog switch T/R. The MIC signal connected to NBDP DSP is for future use.

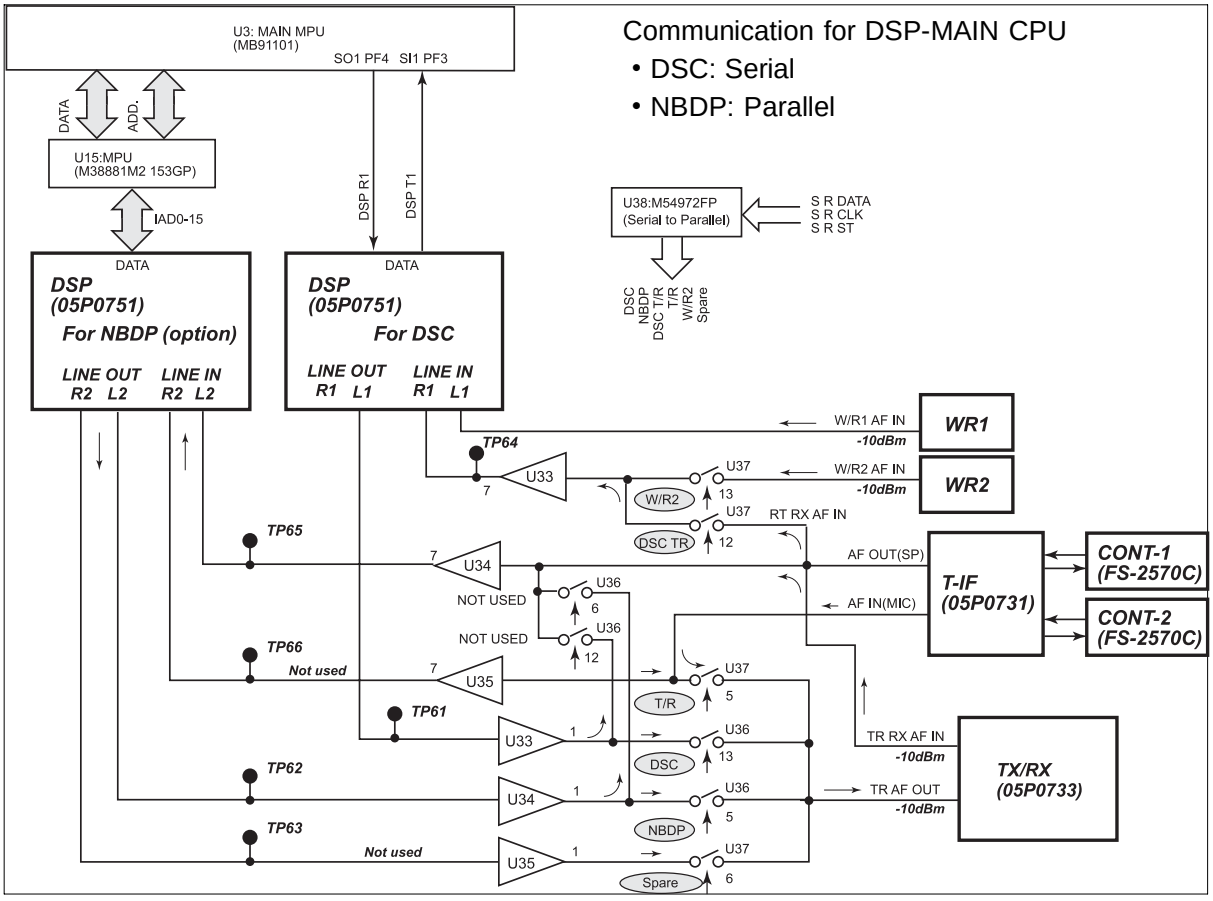


Fig.6.2.3.1-3 DSP input/output circuit

(2) TX/RX Board (05P0733)

(2.a) Block diagram

Fig.6.2.3.1-4 shows the block diagram of TX/RX board (05P0733).

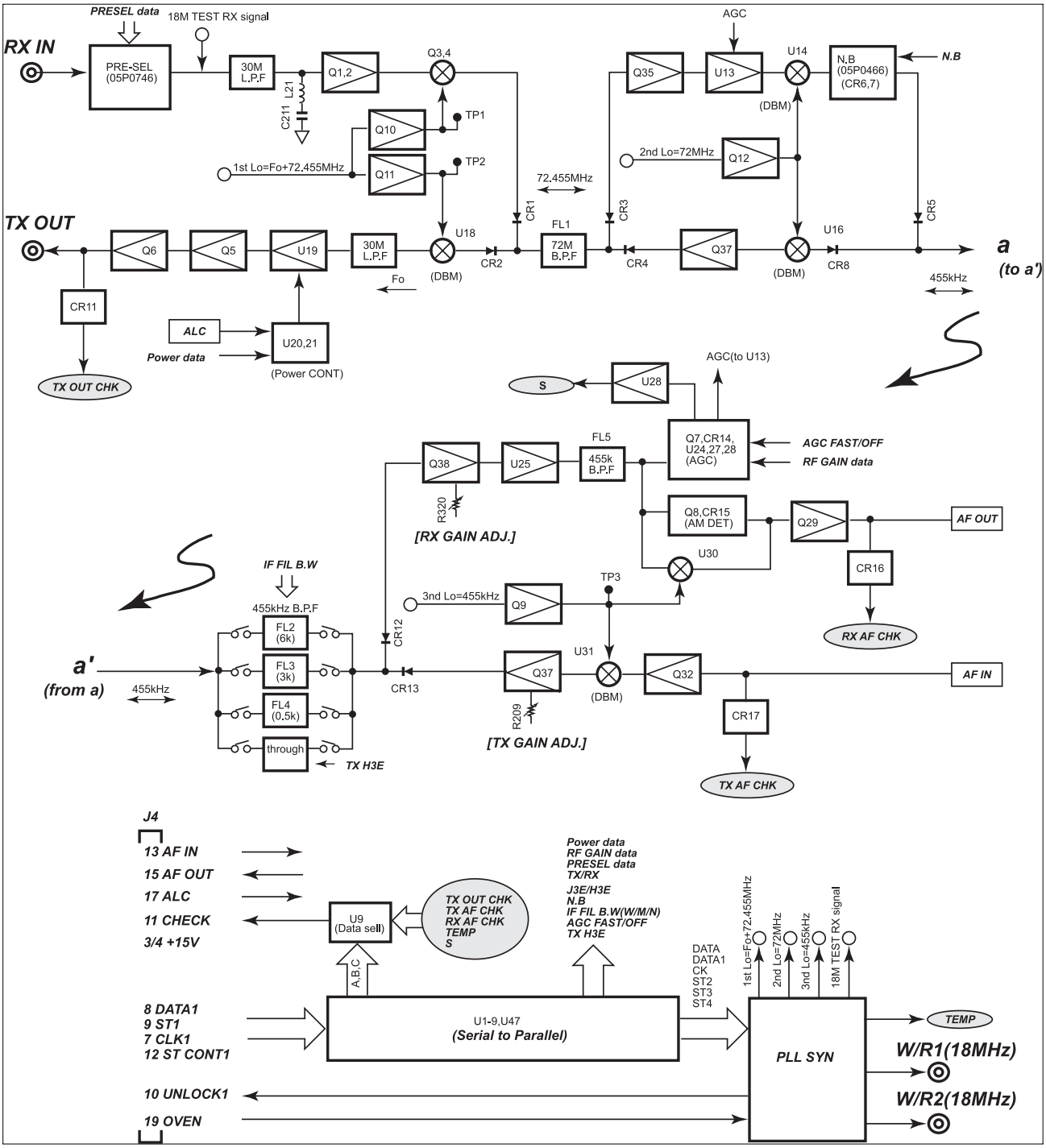


Fig.6.2.3.1-4 Block diagram of TX/RX board (05P0733)

(2.b) Local oscillator

Fig.6.2.3.1-5 shows the block diagram of local oscillator on TX/RX board (05P0733).

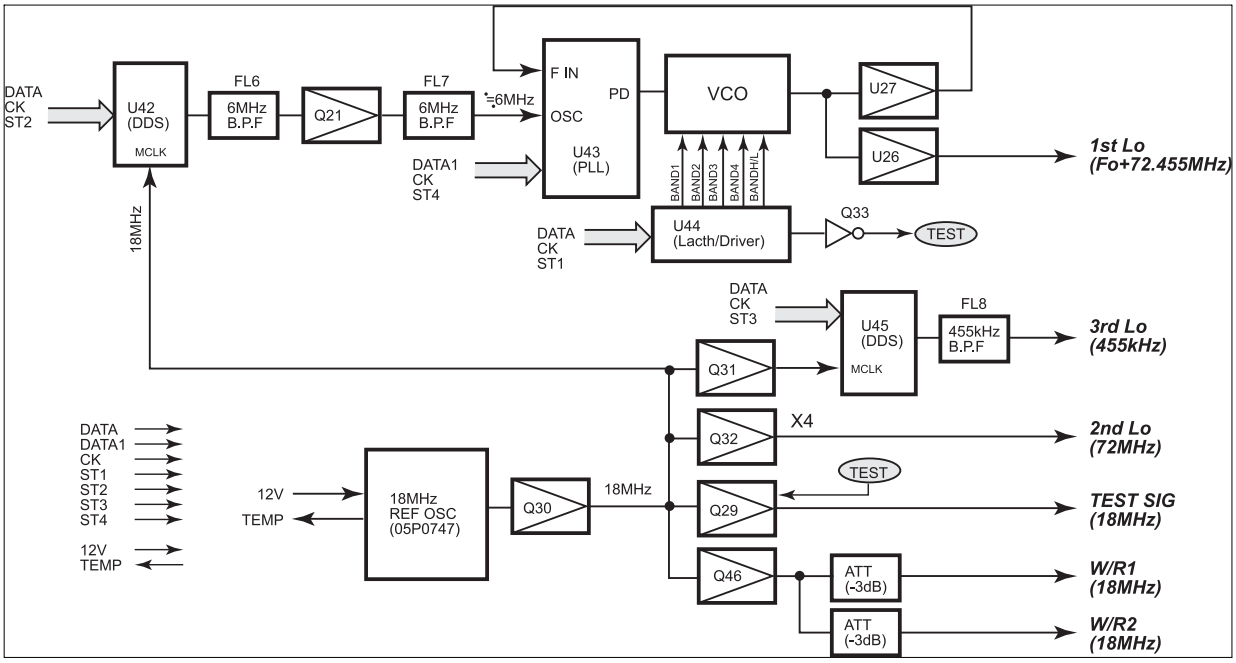


Fig.6.2.3.1-5 Block diagram of local oscillator

(2.c) Reference oscillator

The local oscillator on TX/RX board uses 18 MHz reference signal generated by REF OSC board (05P0747). The reference signal is also used in PLL circuit on W/R board. Y1 is an oven-controlled crystal oscillator. The oscillation frequency is adjusted to 18 MHz ± 5 Hz by the trimmer on Y1.

TEMP Signal

T-CPU board receives TEMP signal from REF OSC board to detect the oven temperature. When the temperature lowers to the designed one, no transmission is made, because the frequency deviates more than ±10 Hz. The message, “OVEN COLD /TX NOT READY: WAIT” appears.

(2.d) Oscillation frequency

First, second and third local oscillators generate F+72.455 MHz, 72 MHz and 455 kHz respectively. The 1st local oscillator consists of PLL and DDS circuits. The PLL circuit uses the output of the DDS circuit as a reference signal. The local oscillator frequency varies according to emission modes as shown in Table 6.2.3.1-7.

Table 6.2.3.1-7 Oscillation frequency of local oscillator

MODE		1st Lo	2nd Lo	3rd Lo
USB		F+72.455 MHz+1.5 kHz	72 MHz	456.5 kHz
LSB		F+72.455 MHz－1.5 kHz		453.5 kHz
H3E	Tx	F+72.455 MHz		456.5 kHz
	Rx			–
TLX				456.7 kHz
FAX				456.9 kHz

The PLL circuit includes four oscillation coils, T11, T12, T13 and T14 for 30 MHz frequency range. These coils are selected depending on frequency setting. Each oscillation circuit is used in lower and upper bands.

Table 6.2.3.1-8 PLL oscillation frequency

BAND	Oscillation coil	Setting frequency (MHz)	VCO frequency (MHz)
1-L	T11	0.1 to 2.99999	72.55500 to 75.45499
1-H		3.0 to 5.99999	75.45500 to 78.45499
2-L	T12	6.0 to 9.49999	78.45500 to 81.94599
2-H		9.5 to 13.49999	81.95500 to 85.95499
3-L	T13	13.5 to 17.49999	85.95500 to 89.95499
3-H		17.5 to 21.49999	89.95500 to 93.95499
4-L	T14	21.5 to 25.49999	93.95500 to 97.95499
4-H		25.5 to 29.99999	97.95500 to 102.45499

Offset frequency: 0 kHz (Mode: H3E, TLX, FAX)

SSB (USB) mode: add 1.5 kHz

(2.e) Transmitter/Receiver circuit

(i) AF circuit

The audio signal from the control unit is connected to TX/RX board via T-IF and T-CPU boards.

Main CPU on T-CPU board sends DSC and NBDP messages to DSP for AFSK (Audio Frequency Shift Keying) modulation or to generate 1700 Hz±85 Hz signal. The modulated DSC and NBDP signal is supplied to TX/RX board. For reception, the signal flows in reverse.

The AF signal or LINE IN and LINE OUT signals to and from TX/RX board is –10 dBm/600 Ω.

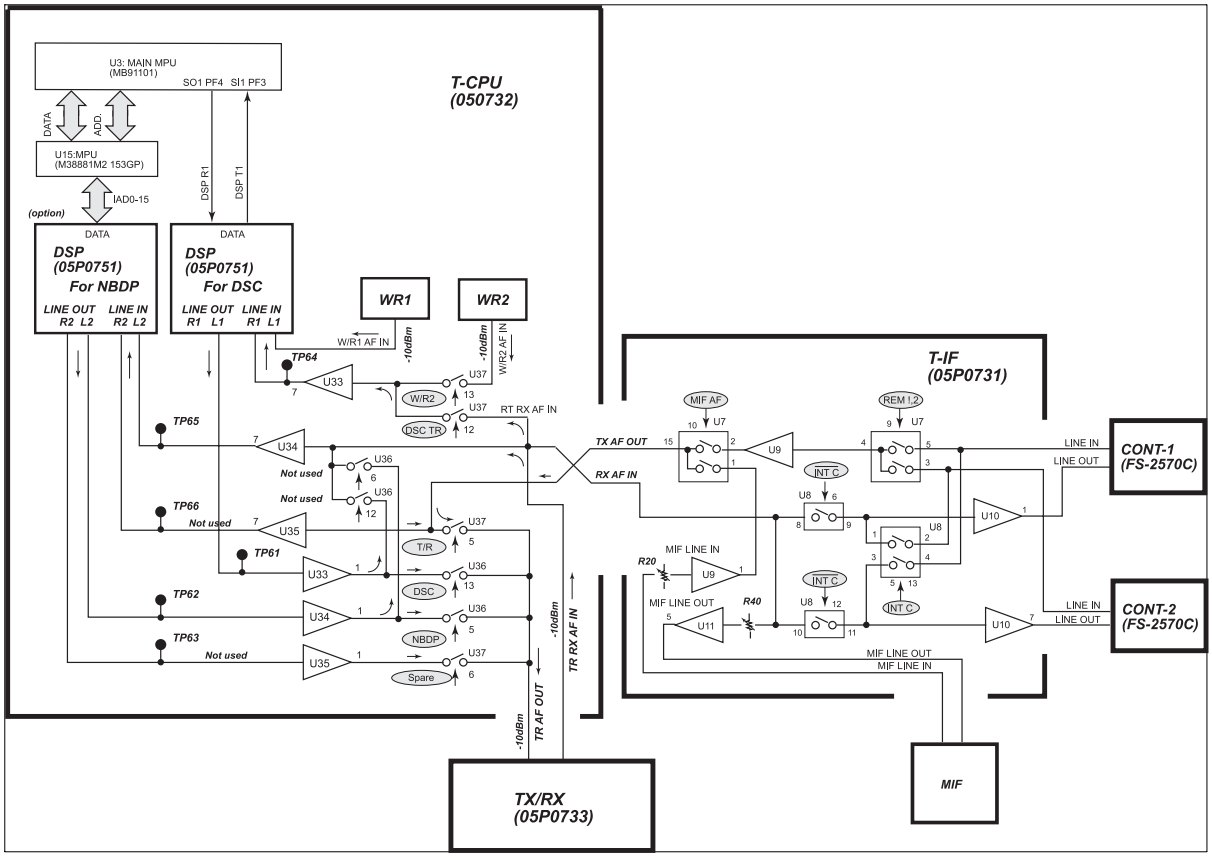


Fig.6.2.3.1-6 Block diagram of LINE IN/OUT circuit

(ii) Transmitting circuit

Fig.6.2.3.1-7 shows the block diagram of the transmitter on TX/RX board, 05P0733.
AF IN signal is converted to RF signal, and then, output to PA circuit from TX OUT connector. The maximum output level is +27 dBm (0.5 W)/50 Ω.
R209, TX GAIN ADJ adjusts the output power from the transceiver unit. With microphone input of -55 dBm and power data of 240, the output from the transceiver unit is set to a quarter of the rated T/R output power. For example, the output power from the transceiver unit is set to about 40 W. The rated T/R output power is adjusted by R76 (ALC) on TX FIL board.

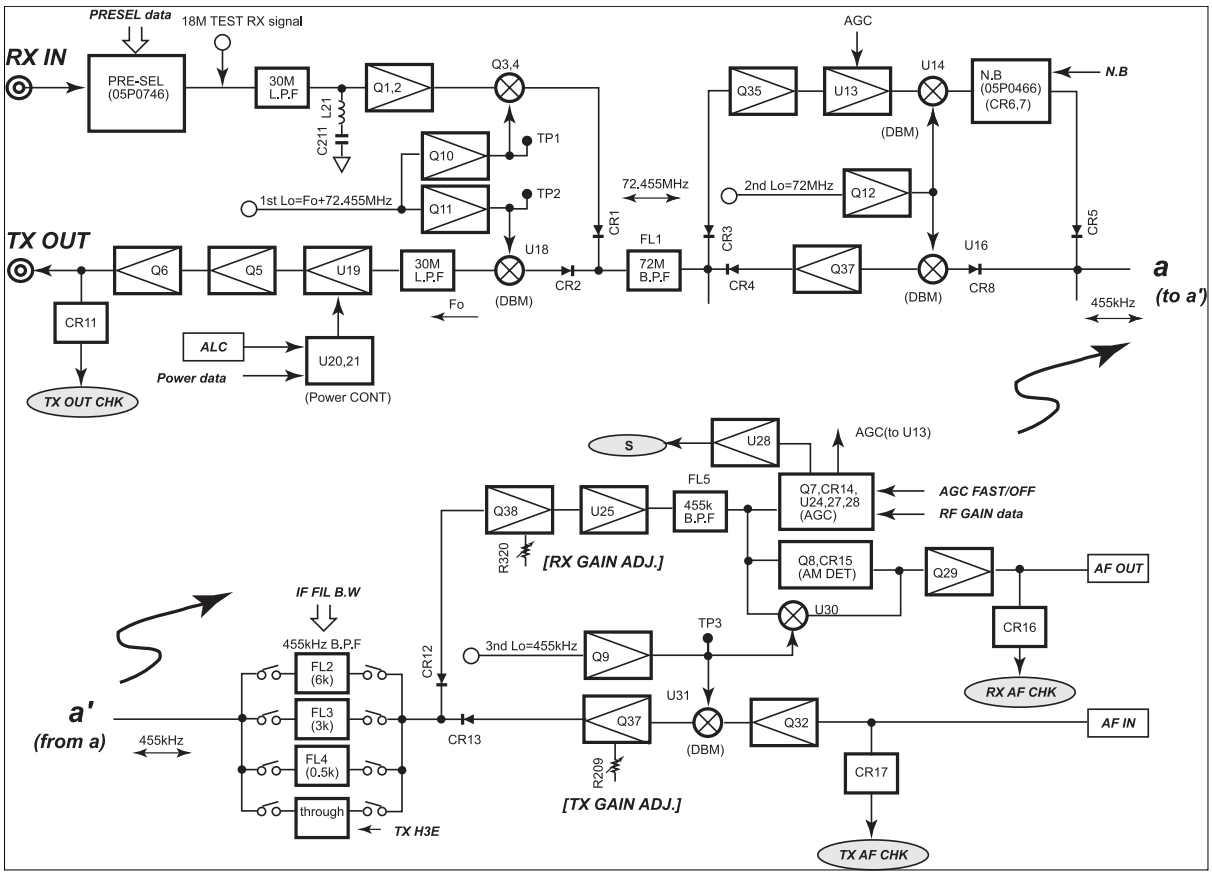


Fig. 6.2.3.1-7 Block diagram of TX/RX board (05P0733)

In J3E mode, AF signal is frequency-converted to RF signal as shown in Table 6.2.3.1-9.

Table 6.2.3.1-9 Frequency converter and Transmitter IF frequency (J3E)

Frequency converter		Local frequency	IF signal
1st mixer	U31 (NJM1496V)	456.5 kHz (3rd Lo)	455 kHz
2nd mixer	U16 (NJM1496V)	72 MHz (2nd Lo)	72.455 MHz
3rd mixer	U18 (NJM1496V)	F0+72.455 kHz+1.5 MHz (3rd Lo)	F0+1.5 kHz

Power control circuit

U19, AD603AR is a variable-gain amplifier in power control circuit ((ALC). The control signal is generated based on the power data and ALC signal from TX FIL board, and sent to pin1 (GPOS) of U19. The ALC signal decreases antenna output power to maintain the rated output power.

Check signal

TX OUT CHK signal is sent to T-CPU board. With the absence of TX OUT CHK signal, “RF” line in TX self-test result display is NG. TX AF CHK signal is not used.

(iii) Filter circuit

The received signal is input to PRESEL board (05P0746) to prevent signals at unwanted frequencies from getting through and optimize the slectivity of a receiver. PRESEL board includes four bandpass filters and a low-pass filter, insertion loss of 2 to 3 dB. 0.1 to 1.45 MHz signal passes through the low-pass filter. BPF2 allows signals at frequency range from 1.45 to 4.99 MHz to pass. BPF2 is made up of LC tuned circuits. Capacitors in BPF2 are selected by relays, receiving PR1 to PR2 data.

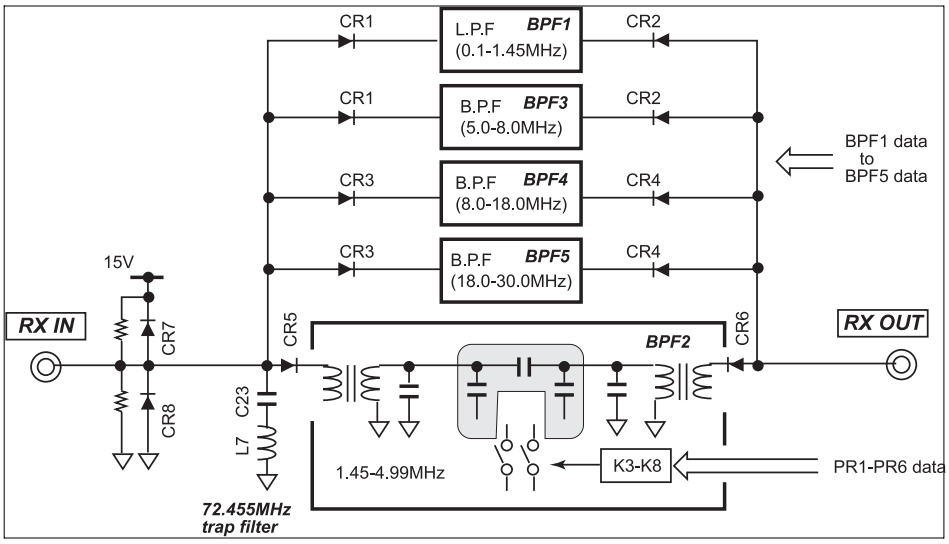


Fig.6.2.3.1-8 Block diagram of PRESEL Board (05P0746)

BPF2 tunes the signal at frequency bands tabulated in Table 5.2.3.1-10. CR7 and CR8 is a receiver protector which protects receiver front-end circuits from damage when an input signal of 15 Vp-p or more is present. C23 and L7 is a 72.455 kHz trap circuit which allows IF signal not to leak from the antenna.

Table 6.2.3.1-10 Tune circuits in BPF2

Tuning frequencies (MHz)					
1.45 to 1.49999	1.8 to 1.84999	2.15 to 2.19999	2.5 to 2.54999	3.1 to 3.19999	4.3 to 4.59999
1.5 to 1.54999	1.85 to 1.89999	2.2 to 2.24999	2.55 to 2.5999	3.2 to 3.29999	4.6 to 4.99999
1.55 to 1.59999	1.9 to 1.94999	2.25 to 2.29999	2.6 to 2.69999	3.3 to 3.39999	
1.6 to 1.64999	1.95 to 1.99999	2.3 to 2.34999	2.7 to 2.79999	3.4 to 3.59999	
1.65 to 1.69999	2.0 to 2.04999	2.35 to 2.39999	2.8 to 2.89999	3.6 to 3.79999	
1.7 to 1.74999	2.05 to 2.09999	2.4 to 2.44999	2.9 to 2.99999	3.8 to 3.99999	
1.75 to 1.79999	2.1 to 2.14999	2.45 to 2.49999	3.0 to 3.09999	4.0 to 4.29999	

(iv) Receiving circuit

Fig.6.2.3.1-10 shows the block diagram of the receiver on TX/RX board, 05P0753. The signal from PRESEL board is supplied to IF (72.455 kHz) trap circuit consisting of C211 and L21 via 30 MHz LPF (Low Pass Filter). Q1 and Q2 are RF amplifiers, gain of 10 dB. The signal is down-converted, amplified and demodulated. AF signal is output from TX/RX board as “AF OUT” signal.

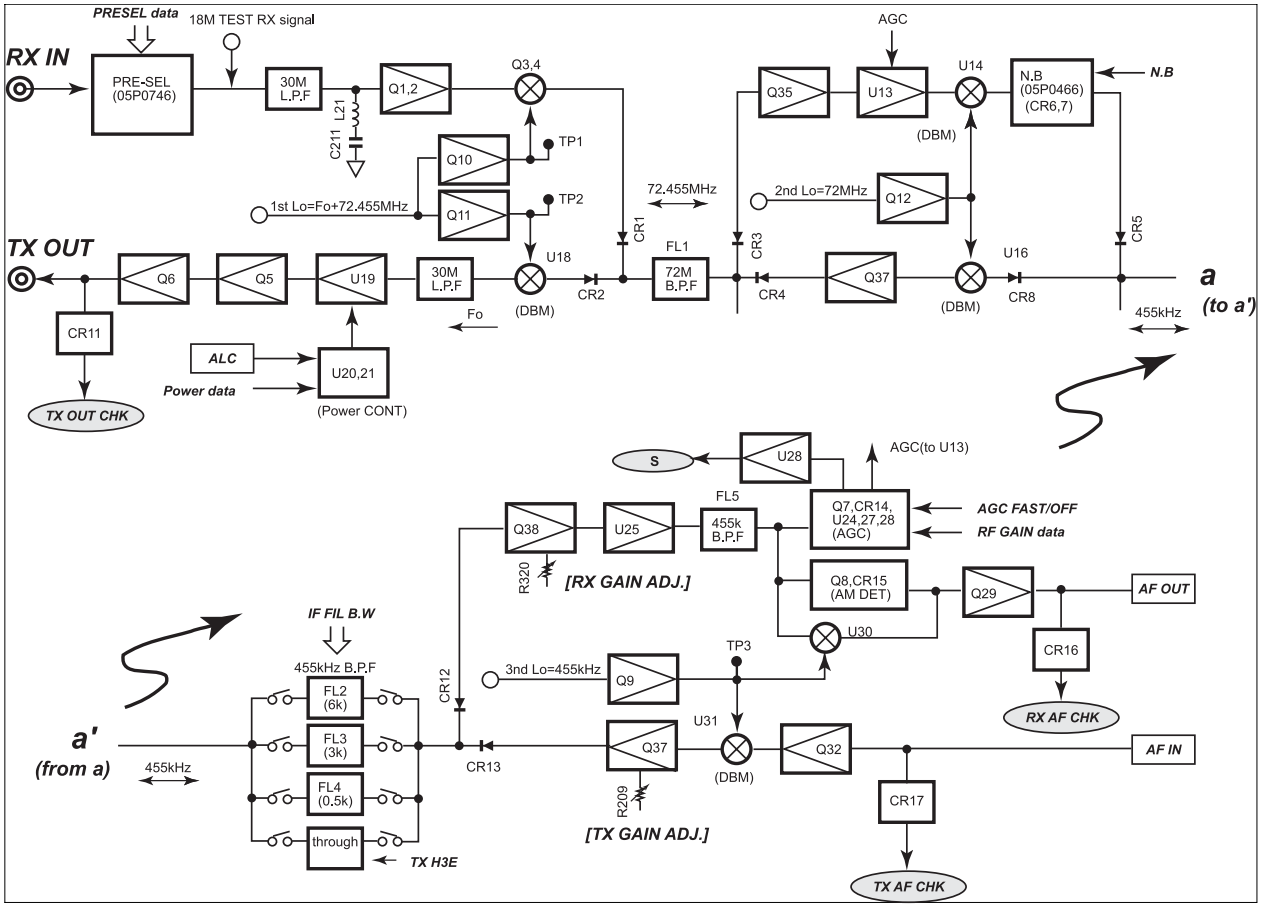


Fig. 6.2.3.1-9 Block diagram of TX/RX circuit

In J3E mode, received signal is frequency-converted as shown in Table 6.2.3.1-11.

Table 6.2.3.1-11 Frequency converter and Receiver IF frequency (J3E)

Frequency converter		Local frequency	Converted signal
1st mixer	Q3, 4 (PMBFJ310)	F0+72.455 kHz+1.5 MHz (3rd Lo)	72.455 MHz
2nd mixer	U14 (NJM1496V)	72 MHz (2nd Lo)	455 kHz
3rd mixer	U30 (NJM1496V)	456.5 kHz (3rd Lo)	1.5 kHz

The receiver sensitivity from RX IN connector on TX/RX board to AF output terminal on the control unit is;

1) SINAD 20dB
   J3E: +3 dBuV
   H3E: +18 dBuV

2) AF output(SP) 4W
   -0±3dBuV

3) Minimum AGC level (Minimum AGC operating level is the same level as that S meter starts defecting.)
   +12 dBuV

(3) Power Amplifier (PA) - PA board (05P0735)

The amplifier circuit on PA board consists of drivers, Q1 and Q2 and push-pull amplifiers Q3 and Q4. The gain is about 27 dB. 0.3 W (about 10 Vp-p) RF signal from TX/RX board is boosted up to 150 W.

PA bias current is adjusted to 200 mA by R25. When measuring the current, the ammeter is placed in series to L4 in PA Vc circuit.

The driver bias current is about 30 to 40 mA. No adjuster is provided. To check the bias current, measure the voltage across R27 (0.22 _) and use formula, $I_{BIAS}=V_{R27}/0.22$.

The ground of PA board is isolated by C39, C40 and C50 from chassis ground. When measuring voltage, use the ground on PA board.

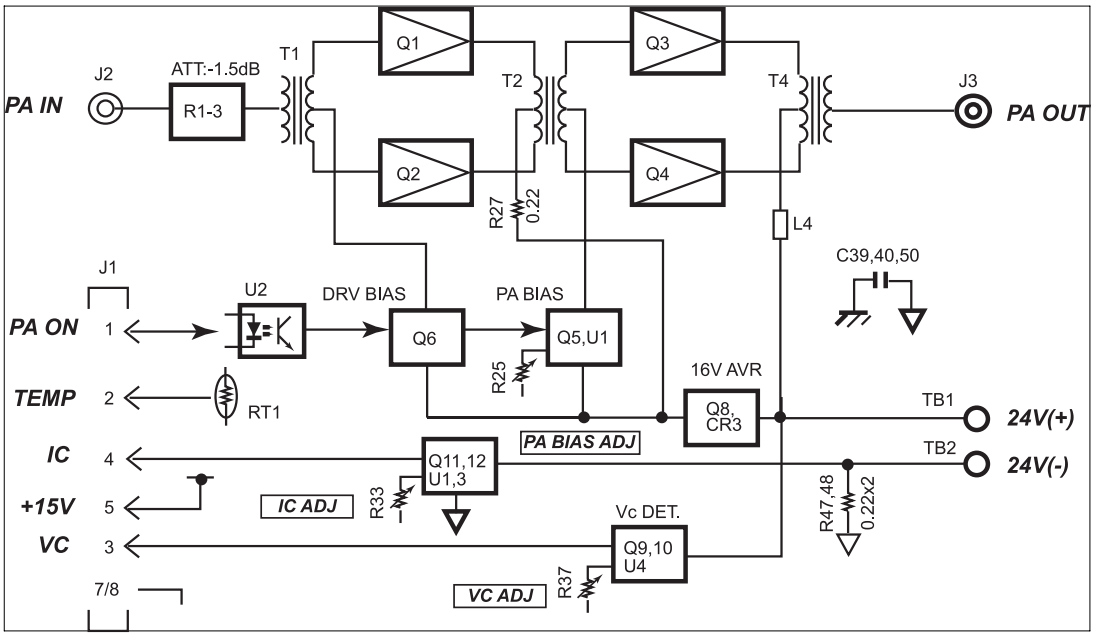


Fig. 6.2.3.1-10 Block diagram of FS-1570 PA board

VC and IC signals

PA collector voltage (VC) is adjusted by R37. The VC detector detects the voltage and sends it to TX FIL board. VC is displayed numerically in Power SET UP menu. PA collector current (IC) is adjusted by R37. The current is detected by R47 and R48 and displayed in Power SETUP menu as “IC”.

TEMP signal

The thermistor RT1 detects the temperature of power amplifier. When the temperature increases up to about 80°C, ”TX POW REDUCED MAIN AMP HEATED” appears and the power is reduced automatically.

PA ON signal

PA ON signal switches on/off the bias circuit on PA board.

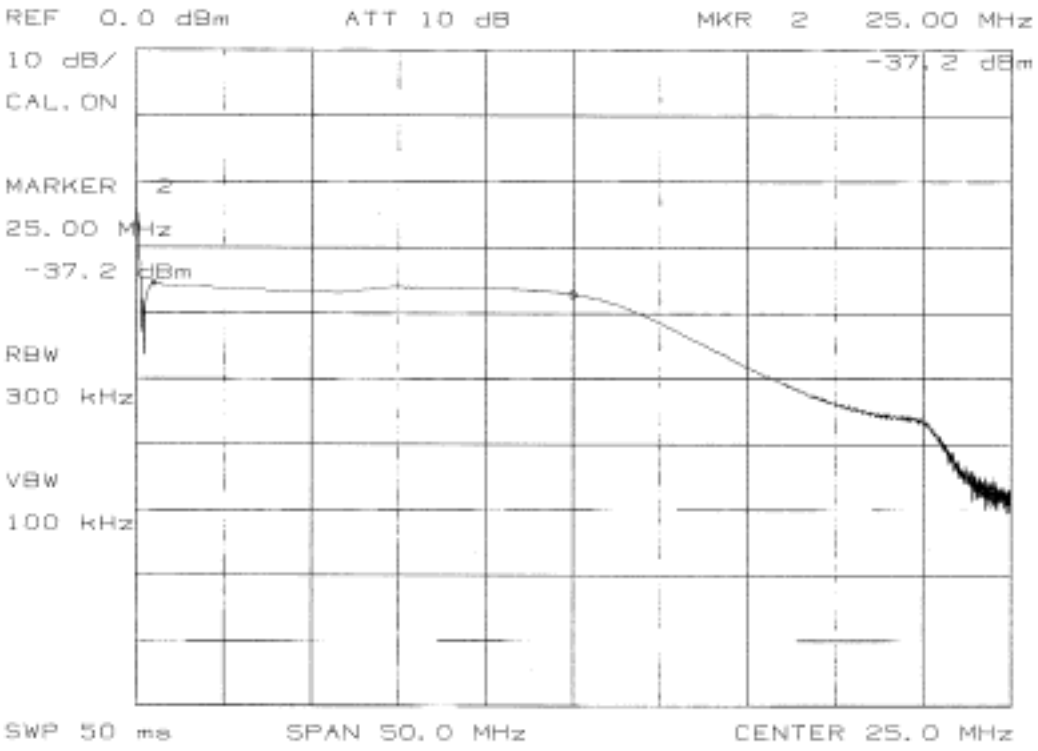


Fig.6.2.3.1-11 PA frequency characteristic of FS-1570

(4) TX FIL board (05P0736)

The TX FIL board, consisting of L.P.Fs, eliminates and suppresses the higher harmonics included in the signal from PA board. The insertion loss is -0.5 dB or less.
T1 and T2, placed in the input and output circuits of the L.P.F, are VSWR detectors. At self-test, the CPU decides that TX FIL board is normal if detectors detect the forward signal. The signal detected by T2 is also used to generate Automatic Level Control (ALC) signal. The ALC signal is sent to “POWER CONT“ circuit on TX/RX board and compared with power data. The T-CPU does not use ALC signal received. R76 adjusts output power.

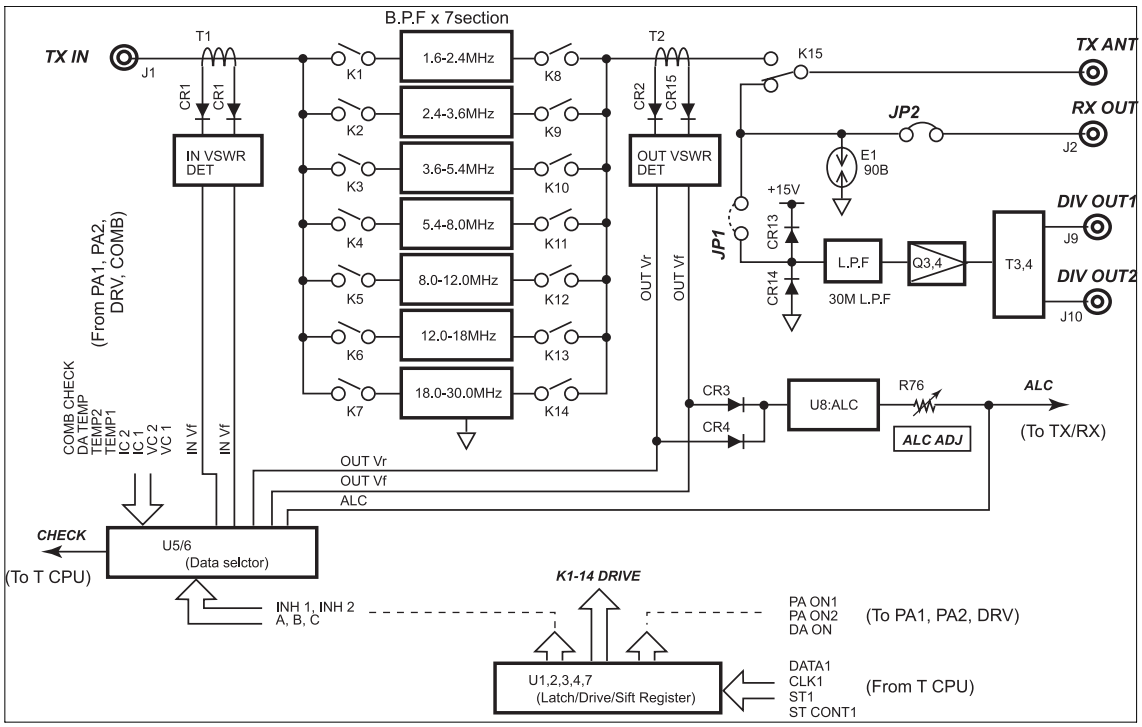


Fig.6.2.3.1-12 Block diagram of TX FIL board

Receiving circuit

The signal received by the antenna is delivered to TX ANT connector via the antenna coupler, and then PRESEL board from RX ANT connector via 50 ohm BK relay, K15.
When DSC general frequency receiver board uses the TX/RX antenna, JP2 is set to “open” and JP1 to “short”.
The received signal is amplified by Q3 and Q4, and applied to DIV OUT 1 and DIV OUT 2 ports via T3 and T4. The OUT 1 and OUT 2 are connected to PRESEL and W/R 2 boards respectively. The signal at DIV OUT ports is 3 dB or more higher than RX OUT port.

(5) W/R board (05P0734)

W/R board (05P0734) is a DSC receiver board: W/R 1 is a DSC distress safety frequency receiver board and W/R 2 DSC general frequency receiver board. Both are identical.
The W/R board consists of RF amplifier, DSC signal demodulator and PLL synthesizer local oscillator. The 18 MHz reference signal used in the PLL circuit is generated by REF OSC board. The frequency error of AFSK signal, 1700 Hz±85 Hz is within ±10 Hz.

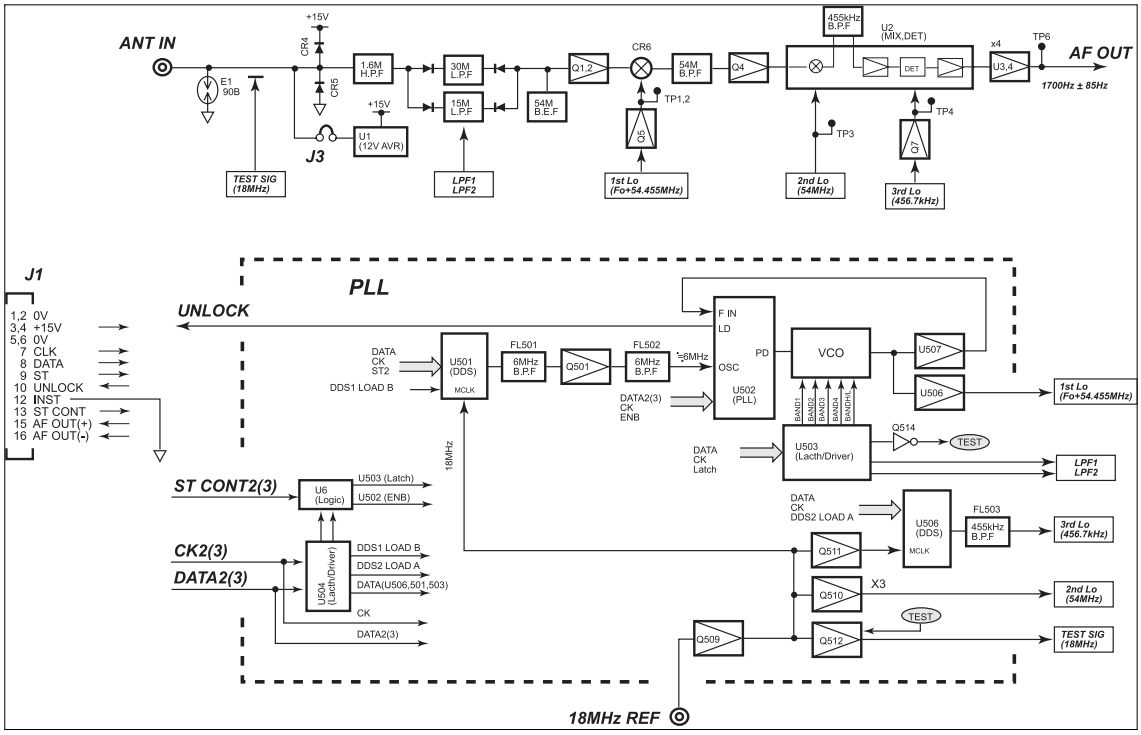


Fig.6.2.3.1-13 Block diagram of W/R board

Specification of W/R board

Antenna impedance: 50 Ω
Receiver type: Double super heterodyne
Receiver sensitivity: Character error rate is 1 % or less with receiver input voltage of 1 uV.
Local oscillator: 1st: F+54455 kHz; 2nd: 54000 kHz; 3rd: 456.7 kHz
Intermediate frequency: 1st IF: 54455 kHz; 2nd IF: 455 kHz
Output level: -10 dBm/600 Ω
Scanning reception: 6 channels (max.) within 2 seconds

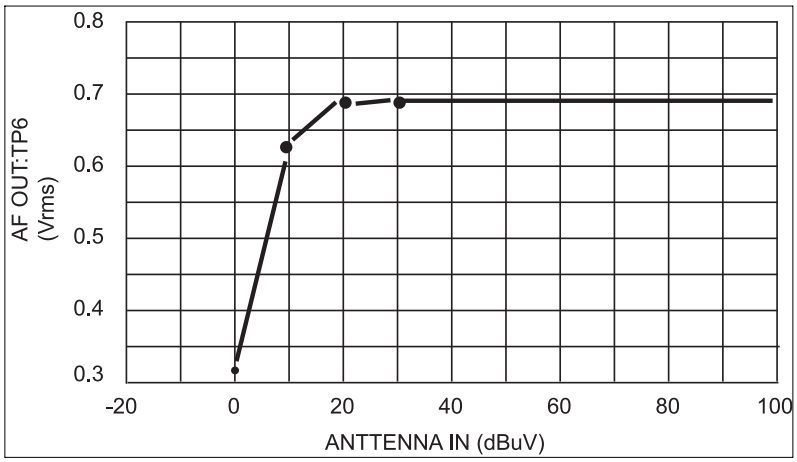


Fig.6.2.3.1-14 Input vs. output on W/R Board

PLL circuit

The PLL circuit consisting of DDS and PLL, operates with the reference signal of 18 MHz from REF OSC board.
The PLL oscillates at the frequency range from 56.0615 to 81.955 MHz, using four oscillation coils, T501 to T504. The oscillation frequency depends on the frequency setting. BAND H/C signal selects the VCO circuit for the lower or higher frequency range in each band.

Table 6.2.3.1-12 PLL oscillation frequencies

BAND	Setting frequency (MHz)	Oscillation frequency (MHz)
1-L	1.6065 to 2.99999	56.06150 to 57.45499
1-H	3.0 to 5.99999	57.45500 to 60.45499
2-L	6.0 to 9.49999	60.45500 to 63.95499
2-H	9.5 to 13.49999	63.95500 to 67.95499
3-L	13.5 to 17.49999	67.95500 to 71.95499
3-H	17.5 to 21.49999	71.95500 to 75.95499
4-L	21.5 to 25.49999	75.95500 to 79.95499
4-H	25.5 to 27.50000	79.95500 to 81.95500

Receiver circuit

The receiver is protected by an arrester, CR4 and CR5 from 30 Vrms signal being applied for more than 15 minutes.
When the preamplifier FAX-5 is used, jumper block J3 is put between #1 and #2 to supply +12V to the preamplifier.

INST Signal

The T-CPU recognizes the presence of the W/R 2 board by receiving INST signal. Table 5.2.3.1-13 lists DSC operation with and without W/R 2 board.

Table 6.2.3.1-13 Functions with and without W/R2

W/R 2	INST signal	DSC scan	DSC ACK reception	DSC self-test result display
Mounted	Yes	W/R2 board	W/R2 board	RECV-2: OK/NG
Not mounted	No	TX/RX board	TX/RX board	Blank

Self test

18 MHz test signal, modulated by mark and space signals, is applied to ANT IN line. The stray capacitance between patterns on the board couples the test signal. The level is equal to SSG output of 70 to 80 dBuV. The receiver on DSC DSP board is also tested by this signal.

Monitor sound of DSC signal

When the dot pattern is detected regardless of the call type, “IN COMING” appears in the display. Then, AF MUTE signal is set to OFF to output the DSC receiving sound from the loudspeaker. If the call is failed to receive or the unrelated call to the own station is sent, the DSC receiving sound is set to MUTE.
DSC DSP always checks DSC signal.

Synchronization to DSC signal

Recognition of DSC signal: By 5 bit dot pattern

Synchronization to DSC signal: The synchronization starts by receiving one of the following synchronizing sequence signal patterns.

- 2 DX signals and 1 RX signal
- 1 DX signal and 2 RX signals
- 3 RX signals

6.2.3.2 Control unit, FS-2570C

(1) C-CPU Board (05P0729)/C-IF Board (05P0730)

Fig.6.2.3.2-1 shows the block diagram of control unit, FS-2570C.

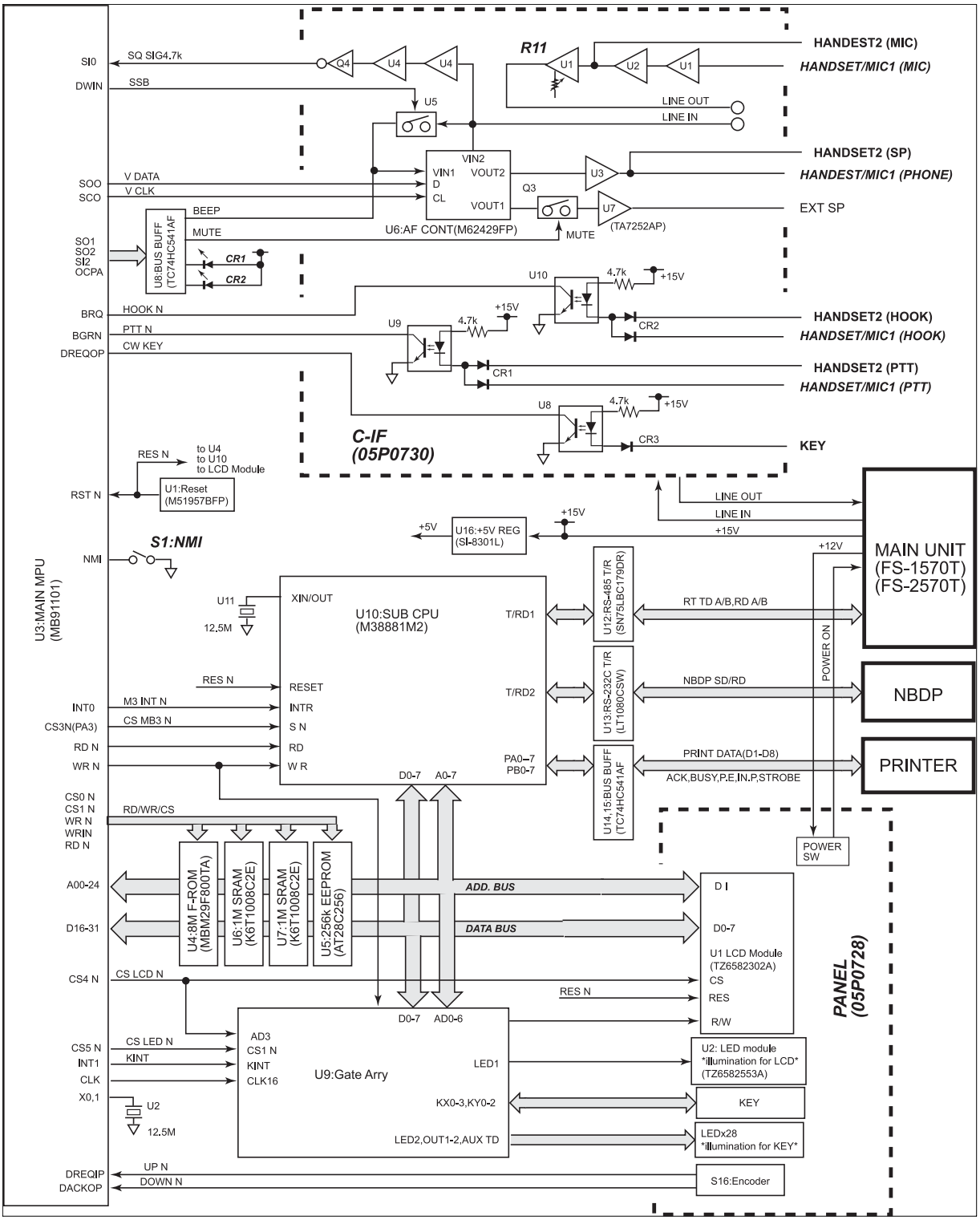


Fig. 6.2.3.2-1 Block diagram of Control unit, FS-2570C

(1.a) C-CPU Board (05P0729)

(i) CPU

32 bit Main CPU and 8 bit CPU locate on C-CPU board.

Table 6.2.3.2-1 C-CPU

MAIN CPU (U3, MB91101)	SUB CPU (U10, M38881M2)	Gate Array (U9, LZ9GF18)
Heart of the control unit	Used to expand serial ports of Main CPU (For NBDP and T-CPU connection)	Controls key input, display and brilliance.

(ii) Memory

Table 6.2.3.2-2 lists the memories on C-CPU board.

Table 6.2.3.2-2 Memories

8 Mbit Flash ROM (U4, MBM29F800TA)	256 kbit EEROM (U5, AT28C256)	**1** Mbit SRAM (U6 andU7, K6T1008C2E)
FS-2570C program is stored.	Backup of contrast/dimmer, and AF/RF volume and SQ settings	Used by C-CPU as working memory

(iii) LED

CR1 and CR2 are not used. These are normally on.

(iv) NMI SW

Not used.

(2) C-IF Board (05P0730)

C-IF board consists of microphone amplifier, audio control circuit, AF amplifier and PTT and HOOK signal detectors. The board receives AF signal, –10 dBm/600 Ω from the transceiver unit as “LINE IN” signal. U6 sets AF output level to the loudspeaker.
The AF signal or LINE IN signal is also input to U3 on C-CPU board as SQ SIG. This signal is used to generate MUTE signal according to SQ FRQ setting in system setting menu. The MUTE signal controls external speaker (EXT SP). The AF line of the handset is not controlled by SQ signal.

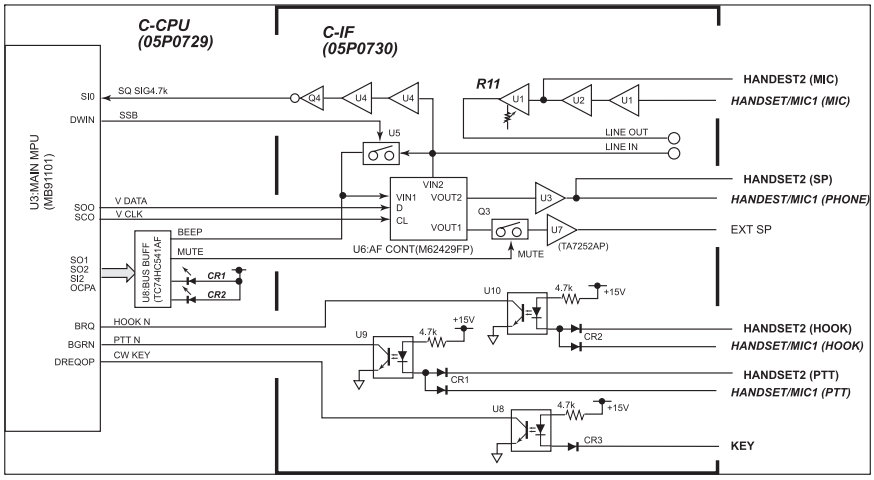


Fig.6.2.3.2-2 Block diagram of C-IF board

Table 6.2.3.2-3 Input/output level

Port	Input/output level of C-IF board			Remarks
		Input	Output	
HANDSET	MIC	-10 dBm/150 Ω	-10 dBm/600 Ω	For the condenser microphone, HS2001
	SP			
HANDSET/MIC	MIC	-46 dBm/600 Ω	-10 dBm/600 Ω	For the dynamic microphone, HSC-701K-20B
	SP			

Note
The control unit provides two handset connection ports, [HANDSET]: HS2001 and [HANDSET/MIC]: HSC-701K-20B. Do not use these ports at a time. Hook and PTT lines on two handsets are connected in parallel.

HOOK signal

OFF HOOK signal is generated when the handset is off-hook. With OFF HOOK signal;
1) DSC AUTO ACK function does not work.
2) "Occupied Another Controller" message appears on the other control unit. No.1 control unit can be used with this message, but No.2 control unit cannot.

KEY signal

Not used.

(3) Handset

The standard handset for FS-1570 is a condenser microphone HS-2001 with amplifiers which amplify –43 dBm/2 kΩ signal to –10 dBm/600 Ω. SP signal of –10 dBm/600 Ω is also amplified to 2.5 mW/150 Ω.
Hall IC, U5 detects Hook signal.

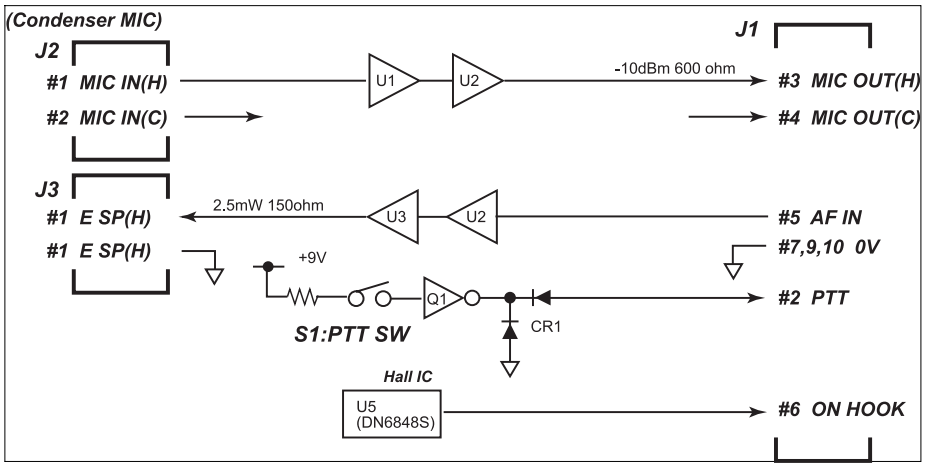


Fig.6.2.3.2-3 Block diagram of Handset, HS-2001

5.2.3.3 Antenna coupler, AT-1560-15

Fig.6.2.3.3-1 shows the block diagram of COUP board in antenna coupler.

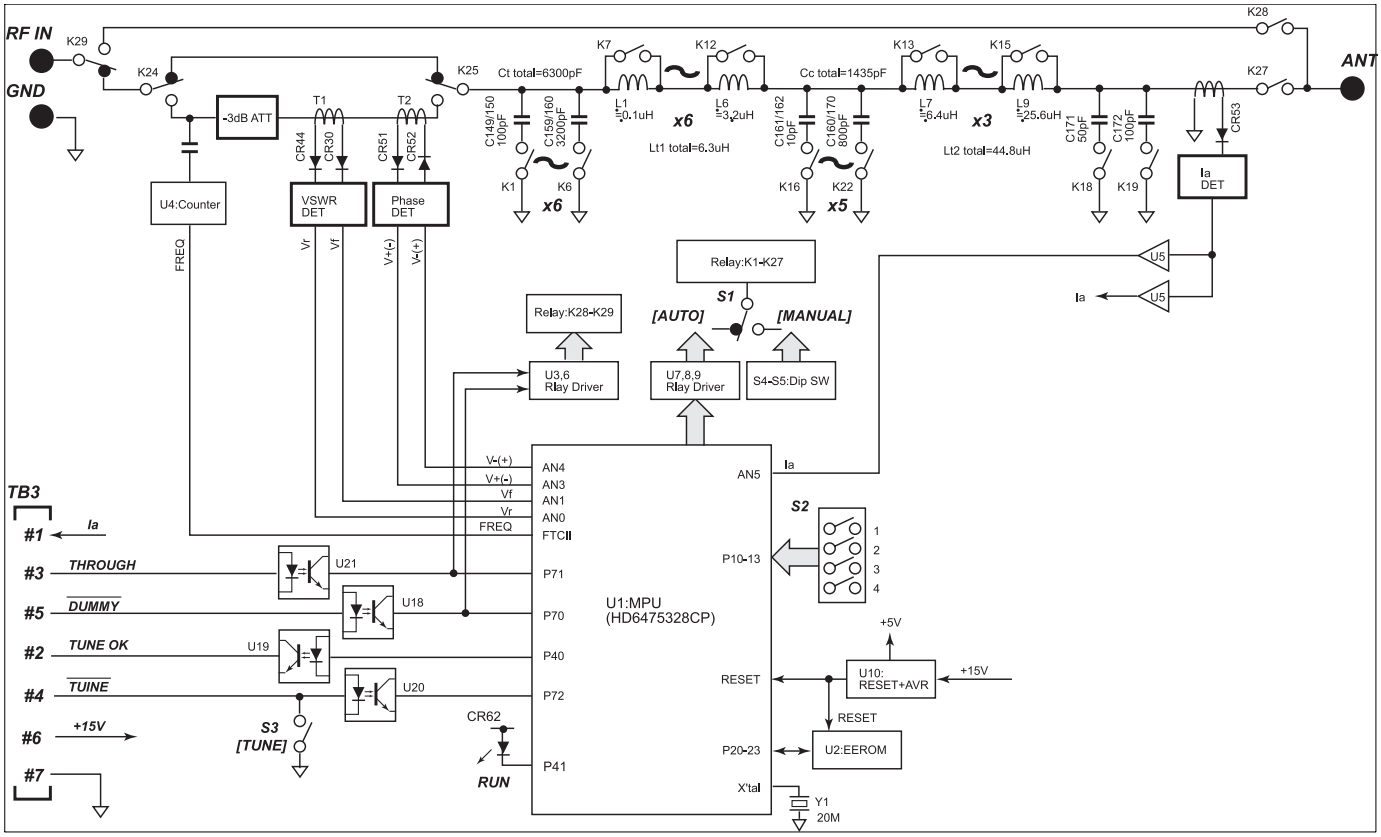


Fig.6.2.3.3-1 Block diagram of COUP board (05P0528)

Timing of control signal

Tuning is made by receiving “TUNE” signal. Fig.6.2.3.3-2 is the timing chart for generating TUNE OK signal. When tuning is made successfully, TUNE OK (H) signal is generated. If not, TUNE ERROR (L) signal is generated. Pressing TUNE switch, S3 also tunes the antenna matching circuit.

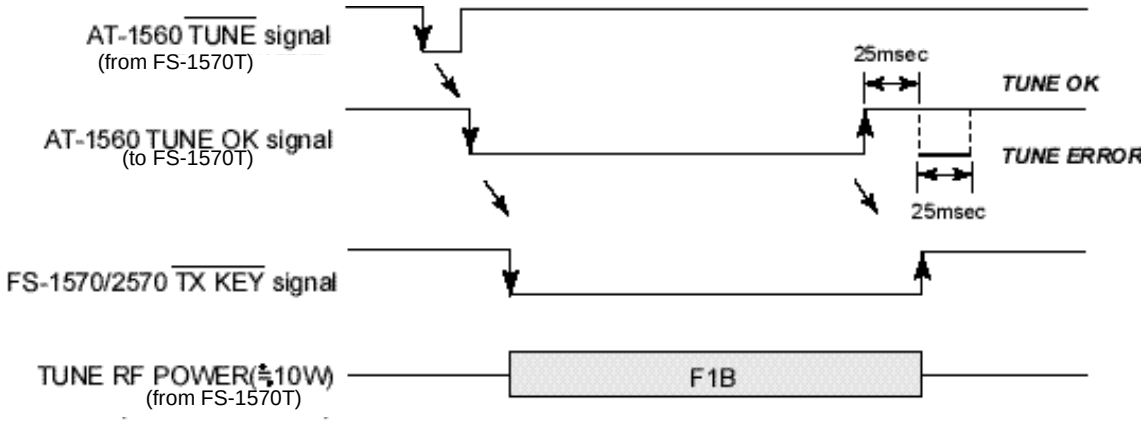


Fig.6.2.3.3-2 Timing of control signals

TROUGH signal

“Through signal” is used to decide whether the receiving signal bypasses the antenna matching circuit or not.
When COUPLER THROU in the RT system setting menu is set to “DIFF”, and the transmission frequency and the receiving frequency are different, the receiving signal bypasses the tuning circuit;

1) If the receiving frequency is 1.6 MHz or less.
2) If the receiving frequency is less than 4 MHz and different from the transmission frequency.
3) If the receiving frequency is 4 MHz or more and different 1.2 MHz from the transmission frequency.
4) During the RT scanning.

Generally, when the transmission frequency and the receiving frequency are different, the receiving signal does not pass through the matching circuit so that the signal is not attenuated.

Matching circuit

The following signals control the antenna matching circuit. Either gamma or pi matching circuit is selected.

- FREQ signal (U4, Counter)
  U4 measures the frequency of the input signal to the matching circuit which tunes 1.6 MHz to 30 MHz signal. The frequency data is also used to store the matching data.
- Vr and Vf (T1, VSWR detector)
  Forward power (Vf) and return power (Vr) are used to calculate VSWR. The matching circuit of the minimum VSWR is selected.
- V+ and V- (T2, Phase detector)
  The phase sensor detects the phase of antenna impedance, capacitive or inductive reactance of an impedance matching network.
- Ia (T3, Ia detector)
  Antenna current, Ia is used for Ia indication and monitoring the matching condition.

Table 6.2.3.3-1 Matching Condition

Frequency	Tune OK		Tune NG	
3.36 MHz or less	VSWR < 3.0	Matching data is memorized.	VSWR > 3.0	Matching circuit short circuits.
3.36 MHz or more	VSWR < 2.0		VSWR > 2.0	

The maximum inductance of the matching circuit is about 50 uH. To tune 2 MHz baud signal to about 7m antenna, most coils in the matching circuit are used. C171 and C172 are used when the antenna capacitance is 40 pF or less and when the supplied voltage to the antenna is 6 kV or more.

Matching circuit

Gamma matching

The gamma matching circuit, Fig.6.2.3.3-3 is used in MF band.
Fig.6.2.3.3-4 shows approximate values of Ct and Lt in the circuit for typical bands.

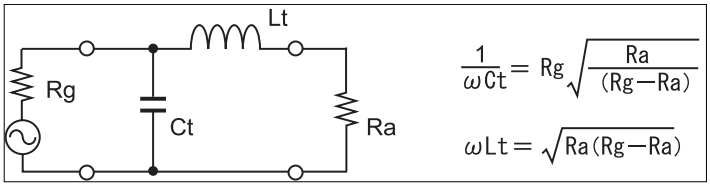


Fig.6.2.3.3-3 Gamma matching circuit

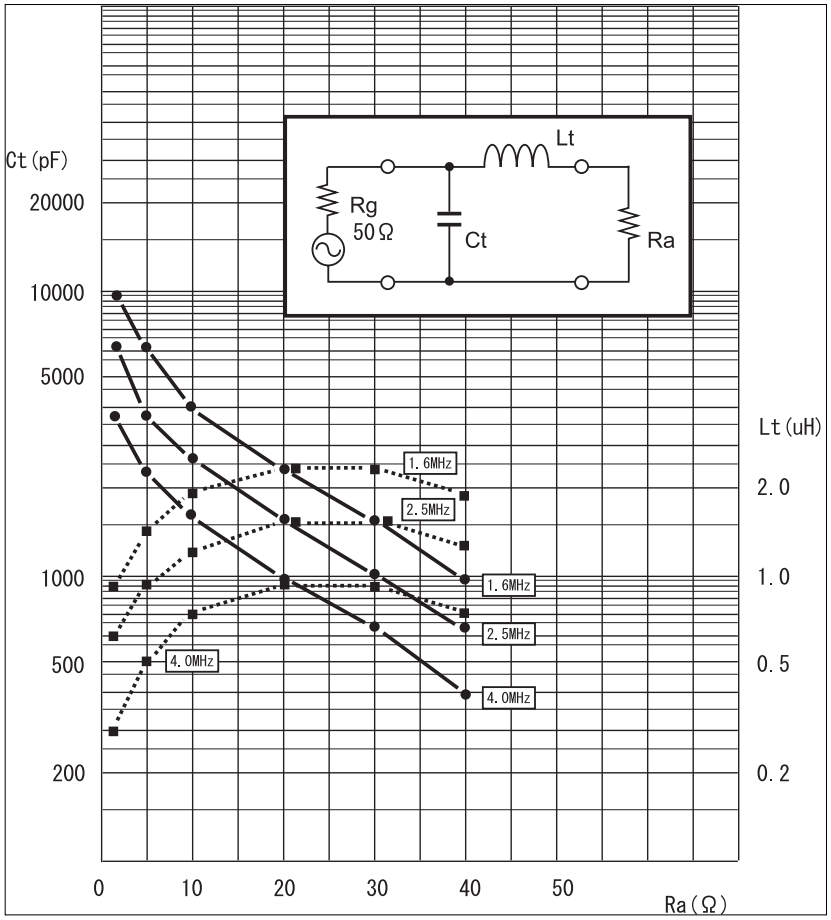


Fig.6.2.3.3-4 Ct and Lt in Gamma matching circuit

The antenna includes resistance, Ra and reactance components. As the wavelength of MF band is longer than the antenna length, the antenna becomes capacitive. The matching circuit needs to cancel the capacitance by adjusting the coil inductance. The coil is called the loading coil. The inductance in the matching circuit is the sum of the matching inductance and inductivity of the reactance coil.

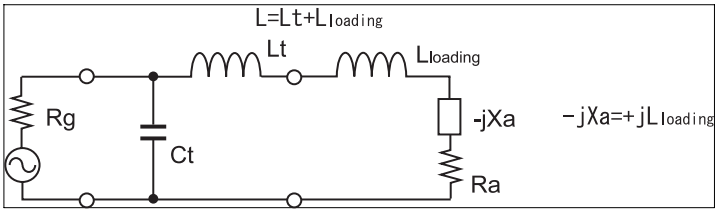


Fig.6.2.3.3-5 Antenna equivalent circuit

Fig.6.2.3.3-6 shows inductances necessary in the matching circuit to cancel the antenna capacitance.

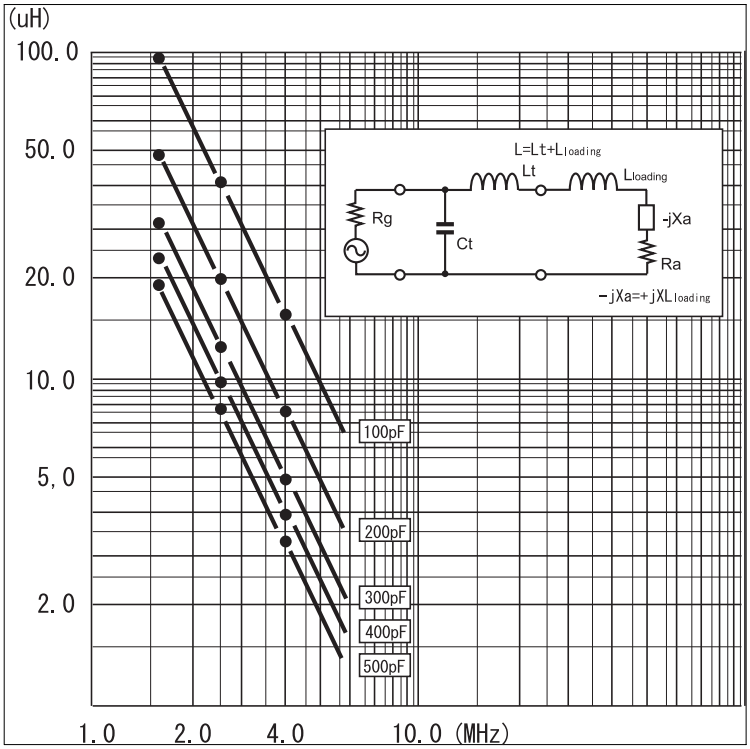


Fig.6.2.3.3-6

Pi matching

Pi matching circuit is used in the HF band. Fig.6.2.3.3-7 shows pi matching and the equivalent circuits.

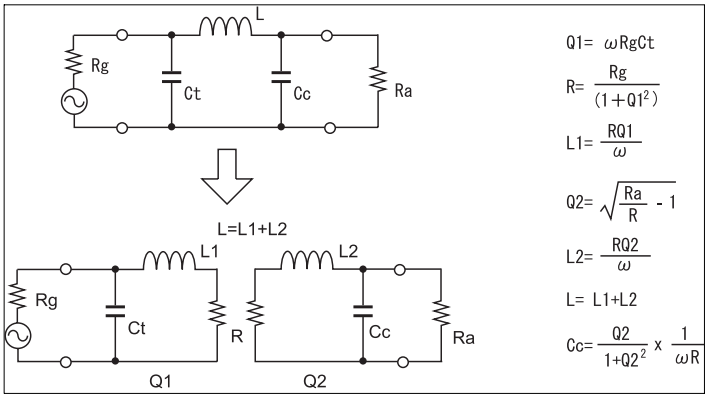


Fig.6.2.3.3-7 Pi matching circuit

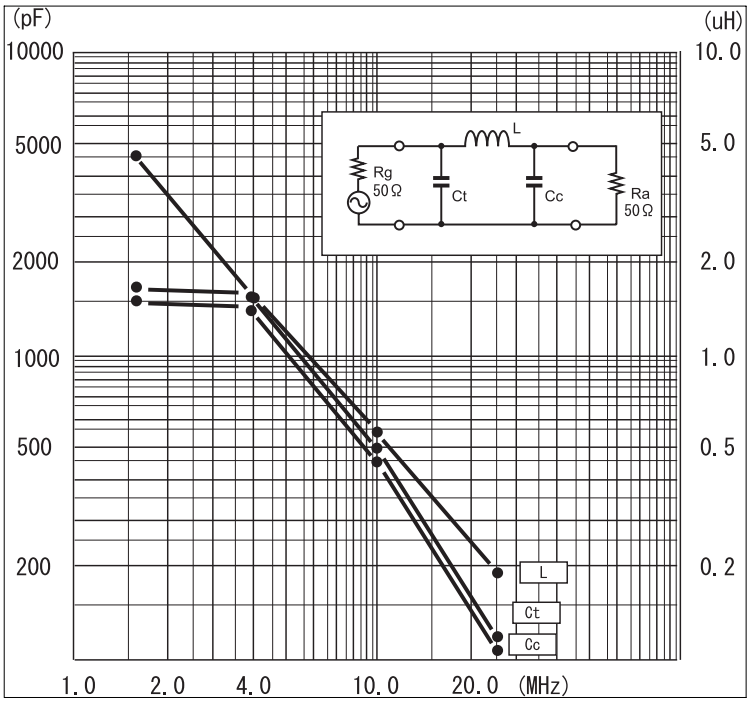
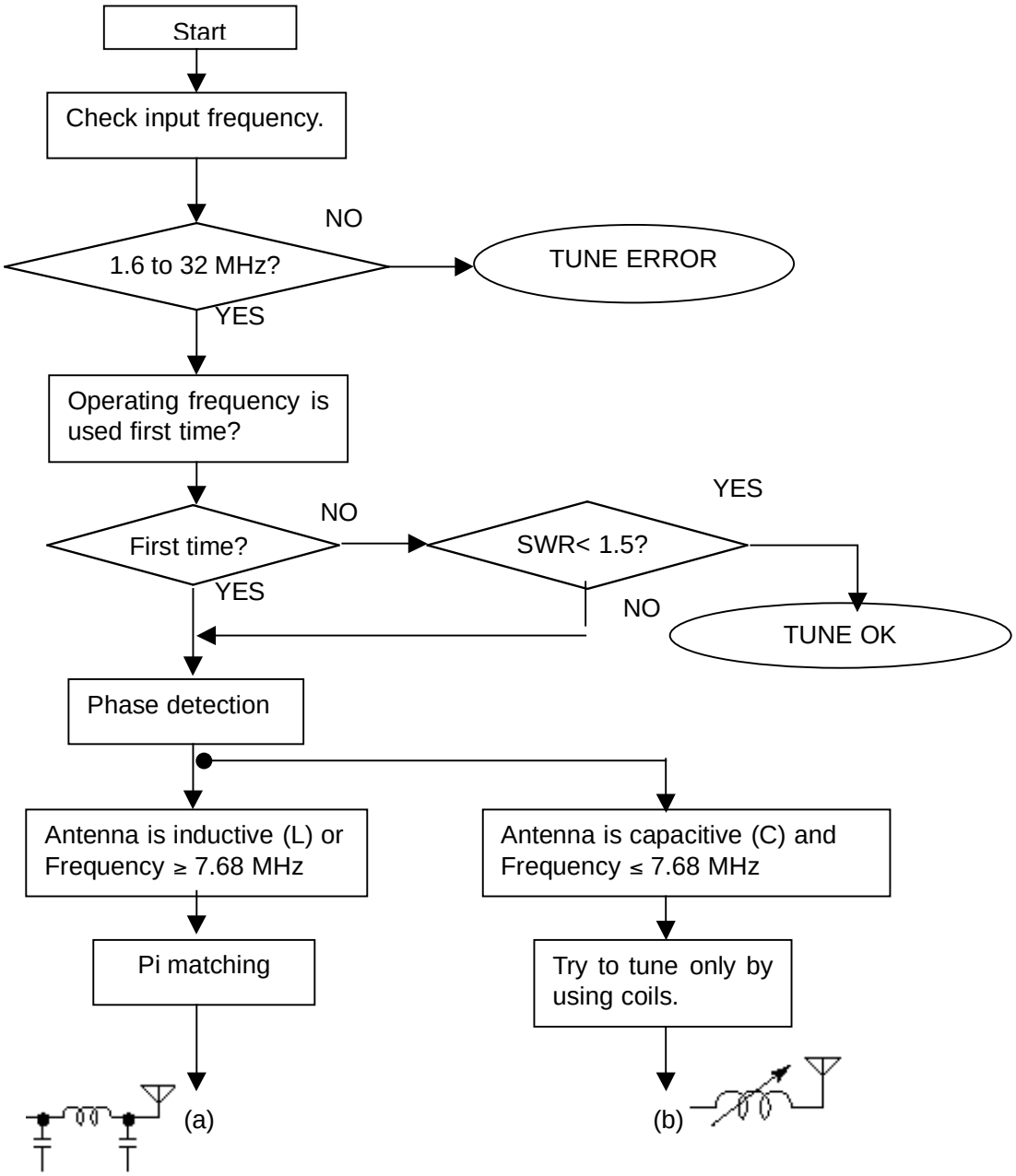


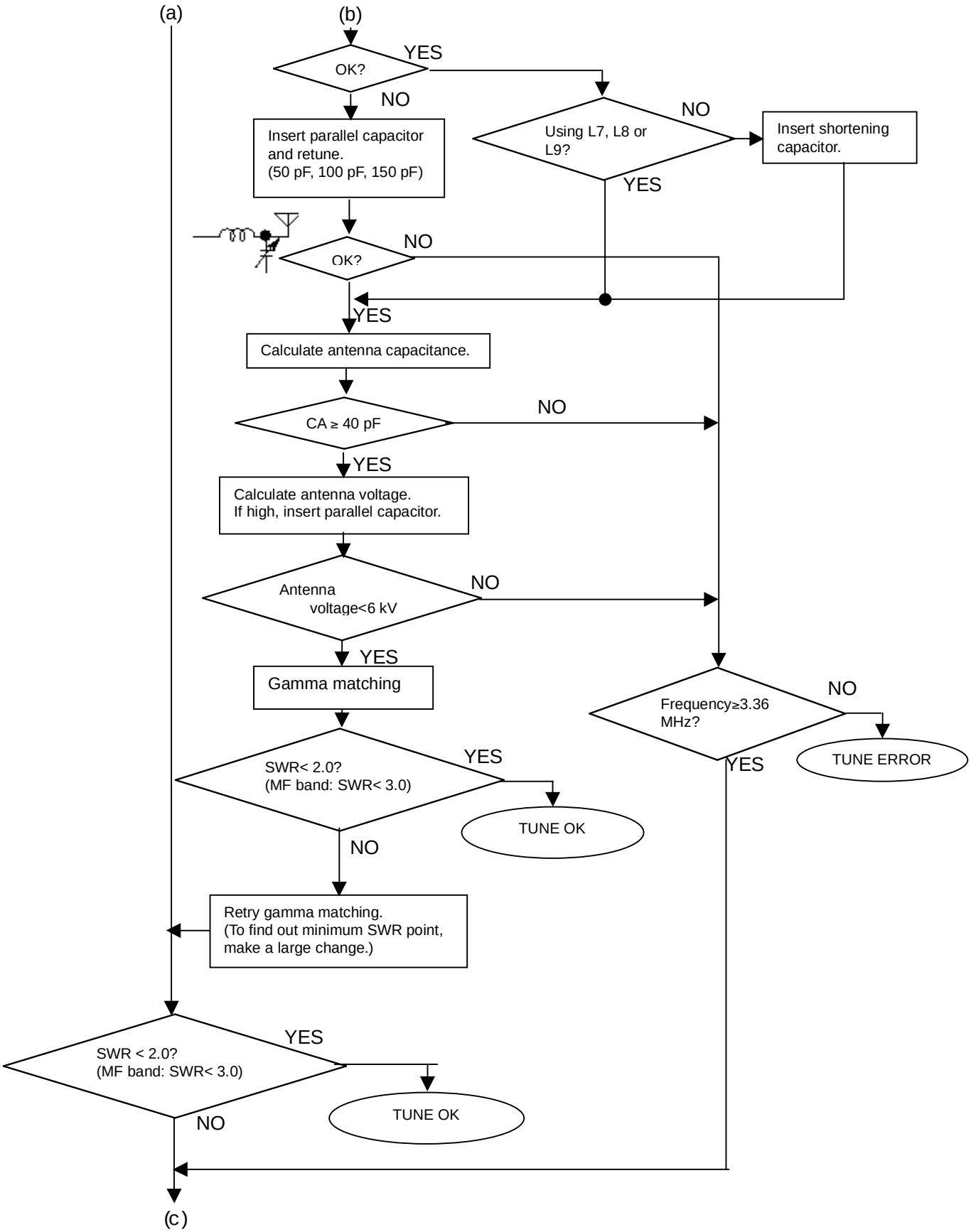
Fig.6.2.3.3-8 C and L in Pi matching circuit for 50-ohm load

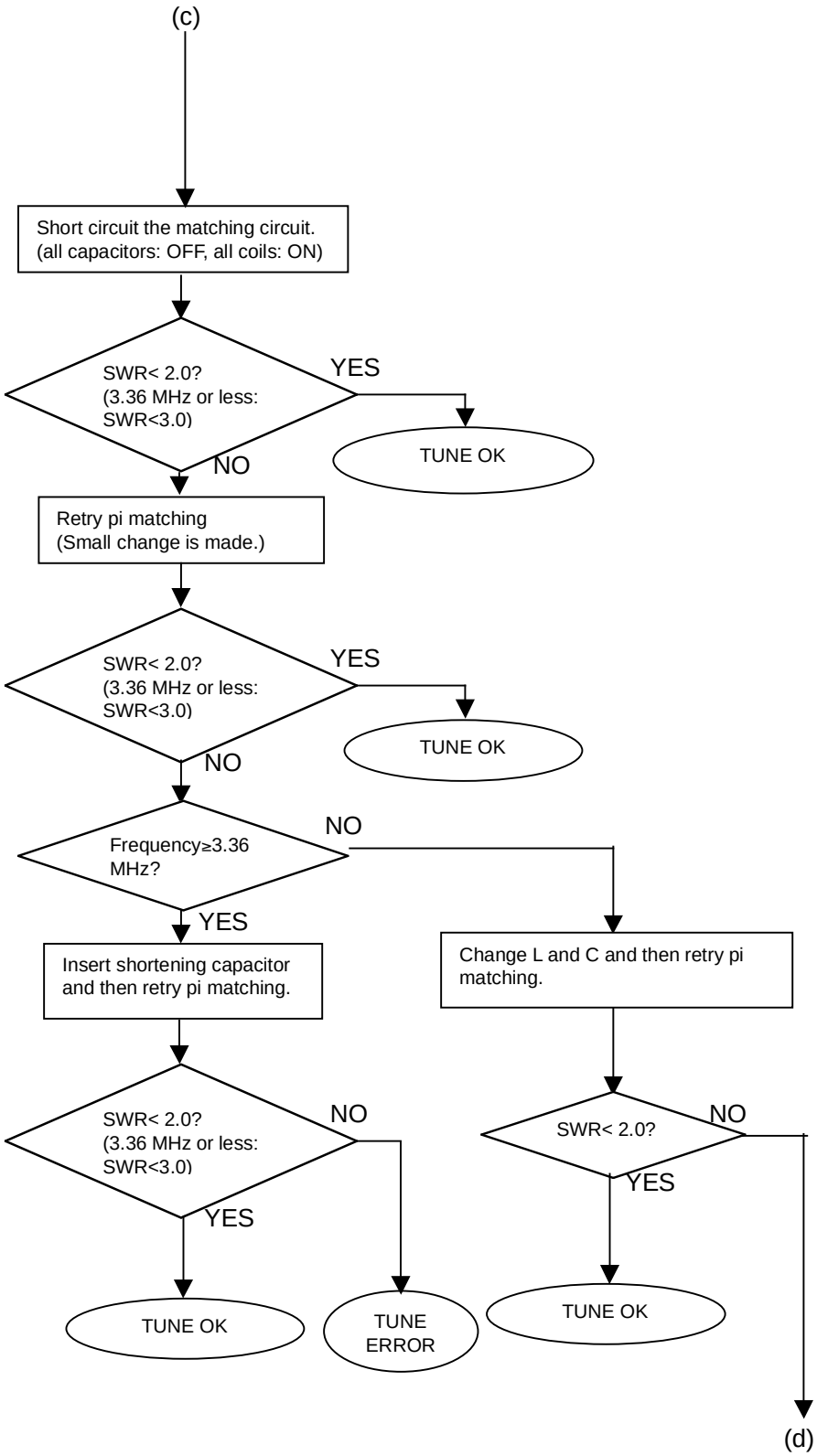
(1) Antenna tuning operation

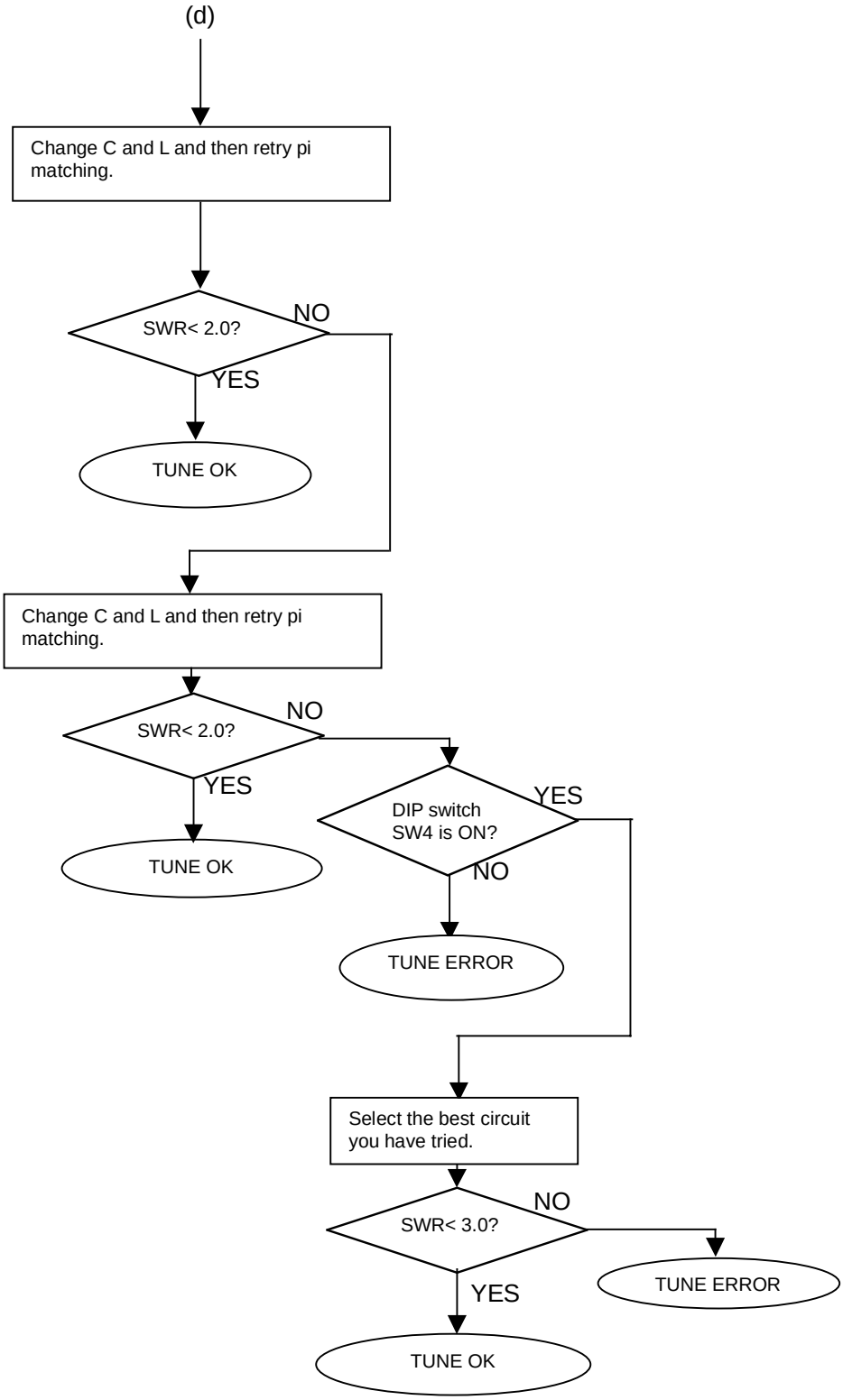


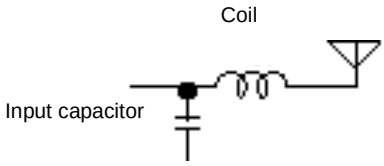
TUNE OK: “TUNE OK” signal is sent to the transceiver unit and relay on/off condition is memorized onto EEPROM.

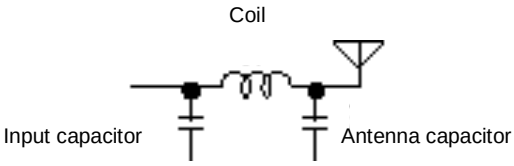
TUNE ERROR: “TUNE ERROR” signal is sent to the transceiver unit while the matching circuit is bypassed.

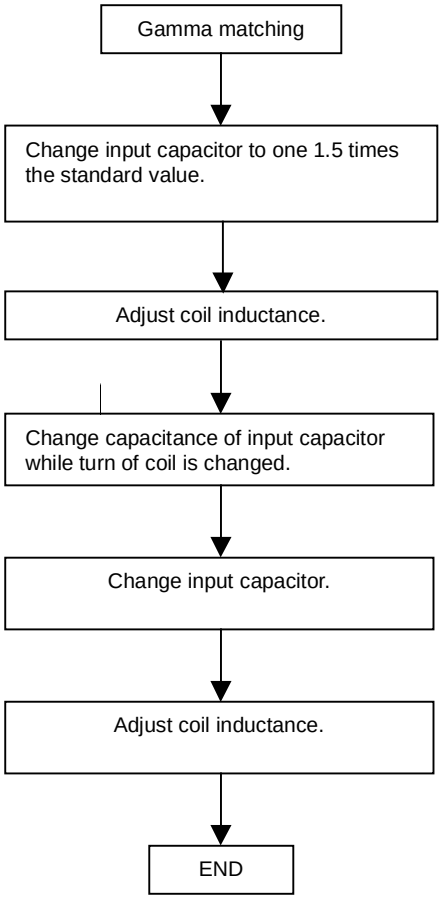

(a)
(b)
OK?
YES
NO
Insert parallel capacitor and retune.
(50 pF, 100 pF, 150 pF)
Using L7, L8 or L9?
NO
YES
Insert shortening capacitor.
OK?
NO
YES
Calculate antenna capacitance.
CA ≥ 40 pF
NO
YES
Calculate antenna voltage.
If high, insert parallel capacitor.
Antenna voltage<6 kV
NO
YES
Gamma matching
Frequency≥3.36 MHz?
NO
YES
TUNE ERROR
SWR< 2.0?
(MF band: SWR< 3.0)
YES
TUNE OK
NO
Retry gamma matching.
(To find out minimum SWR point, make a large change.)
SWR < 2.0?
(MF band: SWR< 3.0)
YES
TUNE OK
NO
(c)

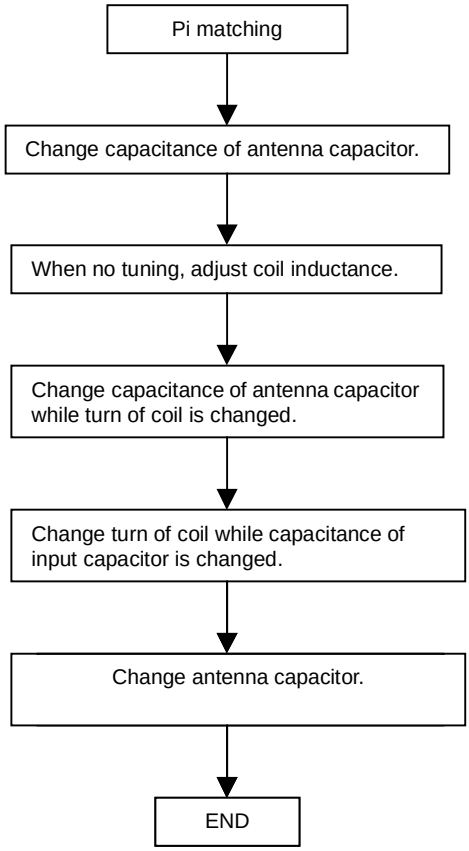

(c)
Short circuit the matching circuit.
(all capacitors: OFF, all coils: ON)
SWR< 2.0?
(3.36 MHz or less:
SWR<3.0)
YES
TUNE OK
NO
Retry pi matching
(Small change is made.)
SWR< 2.0?
(3.36 MHz or less:
SWR<3.0)
YES
TUNE OK
NO
Frequency≥3.36
MHz?
NO
YES
Insert shortening capacitor
and then retry pi matching.
Change L and C and then retry pi
matching.
SWR< 2.0?
(3.36 MHz or less:
SWR<3.0)
NO
YES
SWR< 2.0?
NO
YES
TUNE OK
TUNE
ERROR
TUNE OK
(d)


(d)
Change C and L and then retry pi matching.
SWR< 2.0?
NO
YES
TUNE OK
Change C and L and then retry pi matching.
SWR< 2.0?
NO
YES
TUNE OK
DIP switch SW4 is ON?
YES
NO
TUNE ERROR
Select the best circuit you have tried.
SWR< 3.0?
NO
YES
TUNE ERROR
TUNE OK


Coil
Input capacitor


Coil
Input capacitor
Antenna capacitor


Gamma matching
Change input capacitor to one 1.5 times the standard value.
Adjust coil inductance.
Change capacitance of input capacitor while turn of coil is changed.
Change input capacitor.
Adjust coil inductance.
END


Pi matching
Change capacitance of antenna capacitor.
When no tuning, adjust coil inductance.
Change capacitance of antenna capacitor while turn of coil is changed.
Change turn of coil while capacitance of input capacitor is changed.
Change antenna capacitor.
END

6.2.3.4 IB-583

IB-583 is a NBDP terminal newly developed for FS-1570.

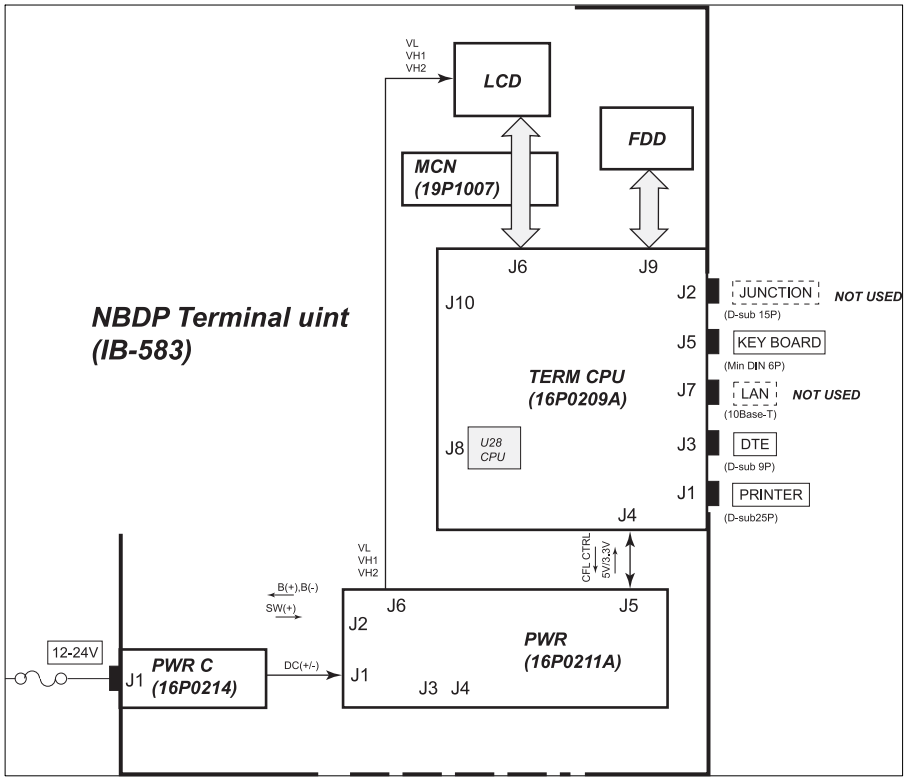


Fig.6.2.3.4-1 Block diagram of IB-583

Major function

1) Communication with RF CON/CPU board (RS-232C, asynchronous, No command)
   Baud rate: 9600
   Data length: 8 bit
   Stop bit: 1 bit
   Parity: No parity
   Flow control: None
   Communication control: None (Only TX/RX data)

2) LCD display (U12) control
3) Backup by lithium battery
4) Key board connection (U7)
5) FDD (U7): 2HD

The IB-583 does not support MIF communication.

(1) TERM CPU board (16P0209A)

Fig.6.2.3.4-2 shows the block diagram of TERM CPU board.

Memory

Table 6.2.3.4-1 lists the memory contents.

Table 6.2.3.4-1 Memory contents

U3 and 4 (S-RAM backupped)	U14 (Flash ROM)
・ AAB/ID ・ USER CH ・ Station List ・ Scan Group ・ Timer OP ・ System data	Program （Including ITU-CH table）

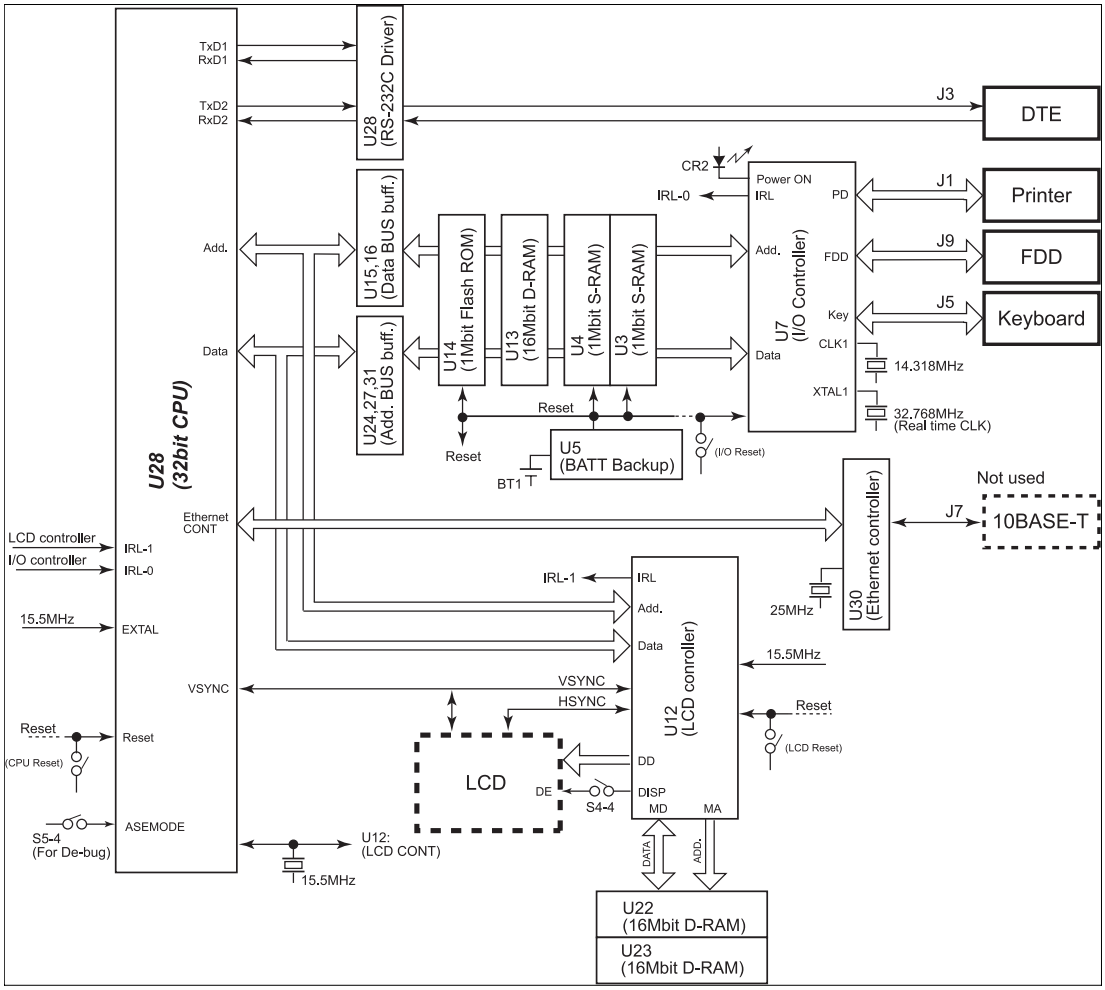


Fig.6.2.3.4-2 Block diagram of TERM CPU Board