6 FM-3000 CIRCUIT DESCRIPTION

1 RECEIVER CIRCUITS

1-1 ANTENNA SWITCHING CIRCUIT (MAIN UNIT)

The antenna switching circuit functions as a low-pass filter while receiving and as resonator circuit while transmitting. The circuit does not allow transmit signals to enter receiver circuits.

Received signals enter the MAIN unit from the antenna connector and pass through the low-pass filter (L21, L22, C1, C127, C130). The signals are then applied to the RF circuit via the antenna switching circuit (D22, D23, R142, R144).

1-2 RF CIRCUIT (MAIN UNIT)

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals.

The signals from the antenna switching circuit pass through a tunable bandpass filter (D25, L35, C149–C152) where the object signals are led to the RF amplifier circuit (Q21).

The amplified signals at Q21 are applied to the other tunable bandpass filter (D26–D31, L36–L39, C161, C162, C164, C165, C173–C178, C182) to suppress unwanted signals and improve the selectivity. The signals are then applied to the 1st mixer circuit.

D25–D31 employ varactor diodes, that are controlled by the PLL lock voltage, to track the band pass filters.

1-3 1ST MIXER AND 1ST IF CIRCUITS (MAIN UNIT)

The 1st mixer circuit converts the received signal into a fixed frequency of the 1st IF signal with a 1st LO (VCO output) frequency. By changing the 1st LO frequency, only the desired frequency will pass through a pair of crystal filters at the next stage of the mixer.

The signals from the RF circuit are mixed with the VCO signals at the 1st mixer circuit (Q22) to produce a 21.7 MHz 1st IF signal.

The 1st IF signal is applied to a pair of crystal filters (FI1, FI2) to suppress out-of-band signals and is then amplified at the IF amplifier (Q23). The amplified signal is applied to the 2nd mixer circuit (IC5).

1-4 2ND IF AND DEMODULATOR CIRCUITS (MAIN UNIT)

The 2nd mixer circuit converts the 1st IF signal into a 2nd IF signal. A double superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain.

The FM IF IC (IC5) contains the 2nd local oscillator, 2nd mixer, limiter amplifier, quadrature detector, and noise detector circuits, etc.

The 1st IF signal from Q23 is applied to the 2nd mixer section of IC5 (pin 16), and is mixed with a 21.25 MHz 2nd LO signal generated at the PLL circuit using the reference frequency (21.25 MHz) to produce a 450 kHz 2nd IF signal.
The 2nd IF signal from IC5 (pin 3) is passed through the ceramic filter (FI3), where unwanted signals are suppressed, and is then applied to the 2nd IF (limiter) amplifier in IC5 (pin 5). The signal is applied to the FM detector section in IC5 for demodulation into AF signals.

The FM detector circuit employs a quadrature detection method (linear phase detection), which uses a ceramic discriminator (X2) for phase delay to obtain a non-adjusting circuit. The detected signal from IC5 (pin 9) is applied to the AF circuit.

1-5 AF AMPLIFIER CIRCUIT (MAIN AND FRONT UNITS, VOL BOARD)

The AF amplifier circuit amplifies the detected signals to drive a speaker. The AF circuit includes an AF mute circuit for the squelch.

AF signals from IC5 (pin 9) are passed through the analog switch (IC16, pins 10, 11), and are applied to the de-emphasis circuit (R291, C291). The de-emphasis circuit is an integrated circuit with frequency characteristic of –6 dB/octave.

The integrated signals are applied to the active filters (Q35, Q36). Q35 functions as a high-pass filter to suppress unwanted lower noise signals and Q36 functions as a low-pass filter to suppress higher noise signals.

The filtered signals are passed through the [VOLUME] control on the VOL board, and are then applied to the AF power amplifier (IC14, pin 1). The output signal from IC14 (pin 4) drives the internal (external) speaker (FRONT unit).

1-6 SQUELCH CIRCUIT (MAIN UNIT)

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch circuit switches the AF mute switch.

A portion of the AF signals from the FM IF IC (IC5, pin 9) pass through the squelch adjustment pot (R214), and are then applied to the active filter section (IC5, pin 8). The active filter section amplifies and filters noise components. The filtered signals are applied to the noise detector section and output from pin 14. The signal is amplified at the SQL amplifier (IC6) and applied to the CPU (IC19, pin 39) as the “SQL” signal. The CPU analyzes the noise condition and outputs the “RMUTM”, “RMUTS” signals to toggle the AF mute switches (Q37, Q38).

2 TRANSMITTER CIRCUITS

2-1 MICROPHONE AMPLIFIER CIRCUIT (MAIN UNIT)

The microphone amplifier circuit amplifies audio signals with +6 dB/octave pre-emphasis from the microphone to a level needed at the modulation circuit.

The AF signals from the microphone are amplified at the microphone amplifier (IC15a, pin 2) via the analog switch (IC13, pins 11, 10). A capacitor (C367) and resistor (R369) are connected to the amplifier to obtain the pre-emphasis characteristics.

The amplified signals are applied to the IDC amplifier (IC17a, pin 2) via the analog switch (IC16, pins 9, 8 and pins 4, 3) and are passed through the splatter filter (IC17b) to suppress unwanted 3 kHz or higher signals. The filtered signals are then applied to the modulation circuit.

2-2 MODULATION CIRCUIT (MAIN UNIT)

The modulation circuit modulates the VCO oscillating signal (RF signal) using the microphone audio signals.

Audio signals from the splatter filter (IC17b) pass through the frequency deviation adjustment pot (R381) and are then applied to the modulation circuit (D1–D3) to change the reactance of D3, and modulate the oscillated signal at the TX-VCO (Q4).

2-3 DRIVE AMPLIFIER CIRCUIT (MAIN UNIT)

The drive amplifier circuit amplifies the VCO oscillating signal to a level needed at the power amplifier.

The VCO output is buffer-amplified by Q6 and Q7, and is then applied to the Tx/Rx switch (D7, D8). The transmit signal from the Tx/Rx switch is amplified to the pre-drive (Q10) and YGR (Q12) amplifiers to obtain an approximate 50 mW signal level. The amplified signal is then applied to the RF power amplifier (IC3).

2-4 POWER AMPLIFIER CIRCUIT (MAIN UNIT)

The power amplifier circuit amplifies the driver signal to an output power level.

IC3 is a power module which has amplification output capabilities of about 35 W with 50 mW input. The output from IC3 (pin 4) is passed through the antenna switching circuit (D14) and is then applied to the antenna connector via the low-pass filter.

2-5 APC CIRCUIT (MAIN UNIT)

The APC circuit stabilizes transmit output power.

The RF output signal from the power amplifier (IC3) is detected at the power detector circuit (D12, D13). The detected signal is applied to the APC control circuit (Q13, Q16, D11) (one of the detected signal is applied to the CPU (IC19, pin 44) as comparison voltage via the "TXDET" signal). The signal from the APC control circuit is applied to the power amplifier's gate bias voltage (IC3). Thus, the APC circuit maintains a constant output power.

3 PLL CIRCUITS

3-1 GENERAL (MAIN UNIT)

The PLL circuit provides stable oscillation of the transmit frequency and receive 1st LO frequency. The PLL circuit compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by a crystal oscillator and the divided ratio of the programmable divider.

IC1 is a dual PLL IC which controls both VCO circuits for Tx and Rx, and contains a prescaler, programmable counter, programmable divider phase detector, charge pomp and etc.

The PLL circuit, using a one chip PLL IC (IC1), directly generates the transmit frequency and receive 1st IF frequency with VCOs. The PLL sets the divided ratio based on serial data from the CPU and compares the phases of VCO signals with the reference oscillator frequency. The PLL IC detects the out-of-step phase and output from pins 8 and 13 for Tx and Rx, respectively. The reference frequency (21.25 MHz) is oscillated at X1.

3-2 TX LOOP (MAIN UNIT)

The generated signal at the TX-VCO (Q4, D1–D3) enters the PLL IC (IC1, pin 2) and is divided at the programmable divider section and is then applied to the phase detector section.

The phase detector compares the input signal with a reference frequency, and then outputs the out-of-phase signal (pulse-type signal) from IC1, pin 8.

The pulse-type signal is converted into DC voltage (lock voltage) at the loop filter (L3, C41, R5), and is then applied to varactor diodes (D1–D3) of the TX-VCO to stabilize the oscillated frequency.

3-3 RX LOOP (MAIN UNIT)

The generated signal at the RX-VCO (Q8, D4, D5) enters the PLL IC (IC1, pin 19) and is divided at the programmable divider section and is then applied to the phase detector section.

The phase detector compares the input signal with a reference frequency, and then outputs the out-of-phase signal (pulse-type signal) from IC1, pin 13.

The pulse-type signal is converted into DC voltage (lock voltage) at the loop filter (L8, R61, C61), and is then applied to varactor diodes (D4, D5) of the RX-VCO to stabilize the oscillated frequency. The lock voltage is also used for the receiver circuit for the bandpass filter center frequency. The lock voltage from the loop filter is amplified at the buffer-amplifier (Q6) and then applied to the RF circuit.

3-4 VCO CIRCUIT (MAIN UNIT)

The VCO outputs from TX-VCO (Q4) and RX-VCO (Q8) are amplified at the buffer amplifiers (Q6 and Q7), and are then sent to the Tx/Rx switch (D7, D8). The receive LO signal is applied to the 1st mixer circuit (Q22) through a low-pass filter, and the transmit signal is applied to the pre-drive amplifier (Q10). A portion of the VCO output is reapplied to the PLL IC (IC1, pin 2 or pin 19) via the buffer amplifier (Q3).

4 DSC CIRCUITS

4-1 DSC ENCODE CIRCUIT (MAIN UNIT)

The DSC signal is created at CPU (IC19, pin 30), is passed through the buffer amplifier (Q51) and applied to the analog switch (IC16, pin 1, 2). The analog switch (IC16) is a modulation switch that switches between the microphone audio signal and the DSC signal.

4-2 DSC DECODE CIRCUIT (MAIN UNIT)

The AF signals from FM IF IC (IC5, pin 9) are filtered at the bandpass filter (IC7) with +18 dB/octave characteristics. IC7b functions as a low-pass filter to suppress unwanted higher noise signals and IC7a functions as a high-pass filter to suppress lower noise signals. The filtered signals are converted analog signals into digital signals at DSC decoder IC (IC8), and are then applied to the CPU (IC19, pin 45) via the "DSDEC" signal after shaping waveform at IC9.

5 LOGIC CIRCUITS

5-1 LOGIC BOARD

• CPU

IC1 is an 8 bit single chip micro-computer and contains LCD driver, serial I/O, timer, A/D converter, programmable I/O, ROM and RAM. The CPU controls to display characters on the LCD too.

• SYSTEM CLOCK CIRCUIT

X1 is a ceramic oscillator and oscillates a 4.91 MHz system clock for the CPU (IC1).

• LCD DRIVER

IC2 is a LCD driver to control dot matrix part on the LCD (DS1).

• DIMMER CIRCUIT

CPU (IC1) and Q2, Q3, Q8 compose dimmer circuit. The circuit controls 8 steps the LCD backlight (DS2–DS17) brightness.

• CONTRAST CIRCUIT

CPU (IC1) and Q1, Q4 compose contrast circuit. The circuit controls 8 steps segment and dot LCD contrast.