5.2 Description of the circuitry and devices provided for determining and stabilizing frequency, for suppression of spurious radiation, for limiting modulation, and for limiting power

5.2.1 Block Description

This unit FA-150 consists of the Transponder Unit FA-1501, the Monitor Unit FA-1502 and the VHF/GPS Antennas.

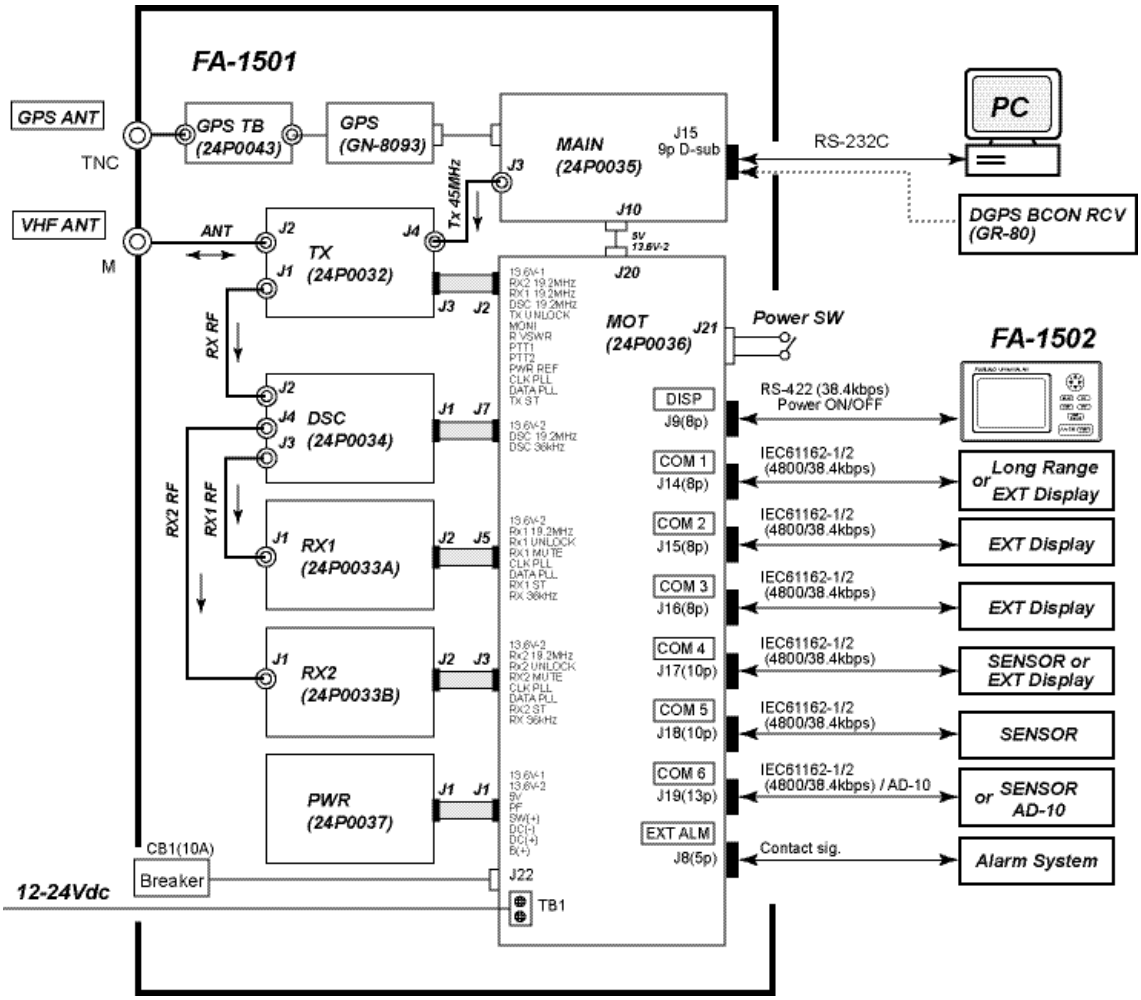
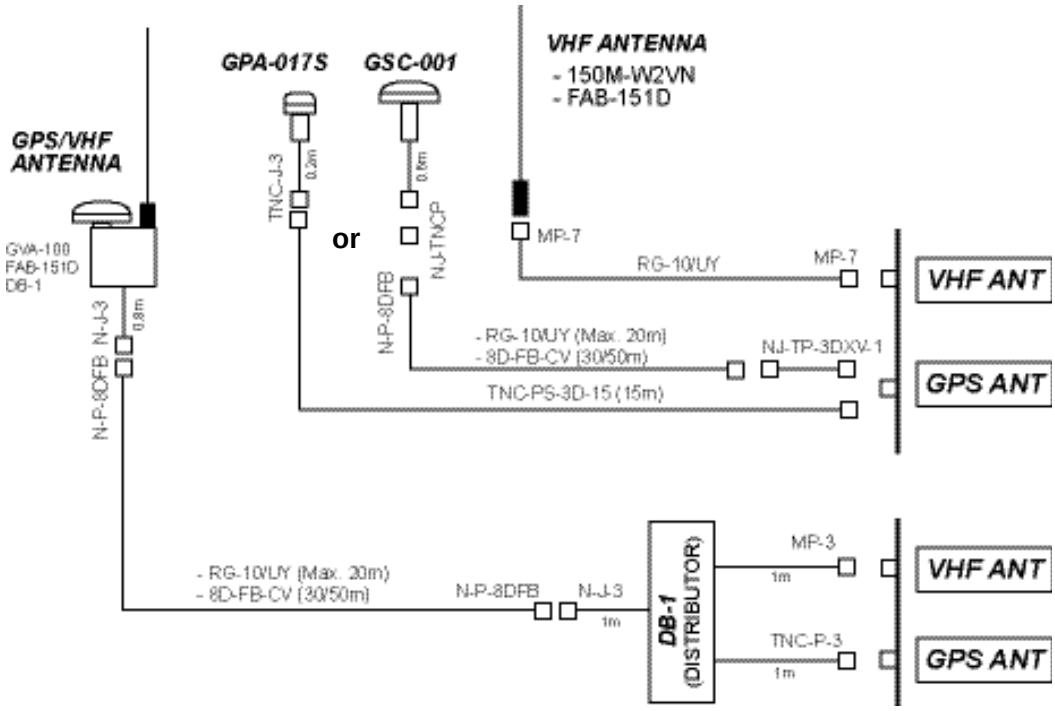


Figure 5.2.1 Block Diagram of FA-1501



VHF separate antenna selection	GPS separate antenna selection	GPS/VHF combined antenna configuration
FAB-151D	GSC-001	GVA-100 + FAB-151D + DB-1
150M-W2VN	GPS-017S	

Figure 5.2.2 VHF/GPS Antenna System of FA-150

5.2.2 Function of major circuits

5.2.2.1 FA-1501

Table 5.2.2.1 Outline of FA-1501

Board name	Outline
MAIN (24P0035)	Consists of MAIN CPU, SUB CPU and its peripheral circuits. Controlling/Processing of AIS (DSC) Communications and I/O interfacing are done by the MAIN CPU. Modulation/Demodulation processing of TDMA/DSC and the analogue-interfacing with the radio parts are done by the SUB CPU.
TX (24P0032)	GMSK-modulated signal of 45 MHz is input from the MAIN Board and converted into the transmitting frequency and power-amplified. RF Power (HPA) Module U1 (RA35H1516M) amplifies the transmitting signal into 12.5 W.
DSC (24P0034)	DSC receiving signal is converted into the 36 kHz IF signal. The receiving frequency is CH70: 156.525 MHz.
RX1 (24P0033A)	AIS receiving signal (TDMA) is converted into the 36 kHz IF signal. Circuit configuration is almost same as those for RX2 Board. Receiving frequencies of CH-A are allocated for RX1 Board.
RX2 (24P0033B)	AIS receiving signal (TDMA) is converted into the 36 kHz IF signal. Circuit configuration is almost same as those for RX1 Board. Receiving frequencies of CH-B are allocated for RX2 Board.
PWR (24P0037)	Consists of switching regulators to convert the input voltages of 12 to 24 VDC to output voltages of 13.6 VDC x 2 and 5 VDC for use in each Board.
MOT (24P0036)	Mother Board for MAIN, RX1, RX2, DSC and PWR Boards. External equipment such as Sensors and Radars are connected to WAGO terminals of the Board.
GPS (GN-8093)	GPS module for receiving the GPS signal of L1: 1575.42 MHz. Number of receiving channels are 12 parallel (12-satellite tracking).
GPS TB (24P0043)	For relaying the GPS receiving signal.

5.2.2.2 FA-1502

Table 5.2.2.2 Outline of FA-1502

Board name	Outline
CPU (24P0062)	AIS information display (MKD) and the system setting-up. Communications interface of RS-422 with FA-1501 is used with the speed of 38.4 kbps.

5.3 FA-1501 Block Description

5.3.1 TX Board (24P0032)

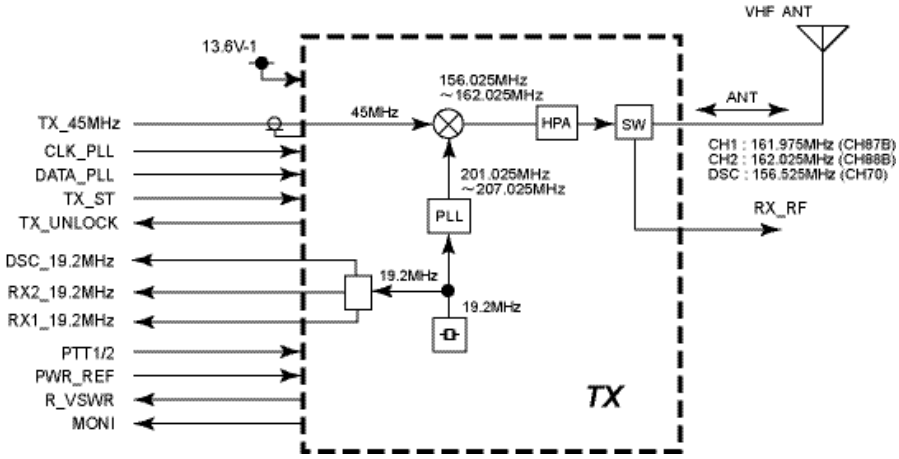


Figure 5.3.1 Outline of TX Board

The TX Board consists of Reference Oscillator, Frequency converter, TX PLL circuits, Power amplifier and TX/RX Antenna switching circuits.
Modulated signal of 45 MHz input from MAIN Board is converted to TX frequency of 150 MHz band, and then amplified into 12.5 W in the HPA module.
Reference oscillation frequency of 19.2 MHz is used as the PLL reference frequency for DSC, RX1 and RX2 Boards in addition to TX Board.

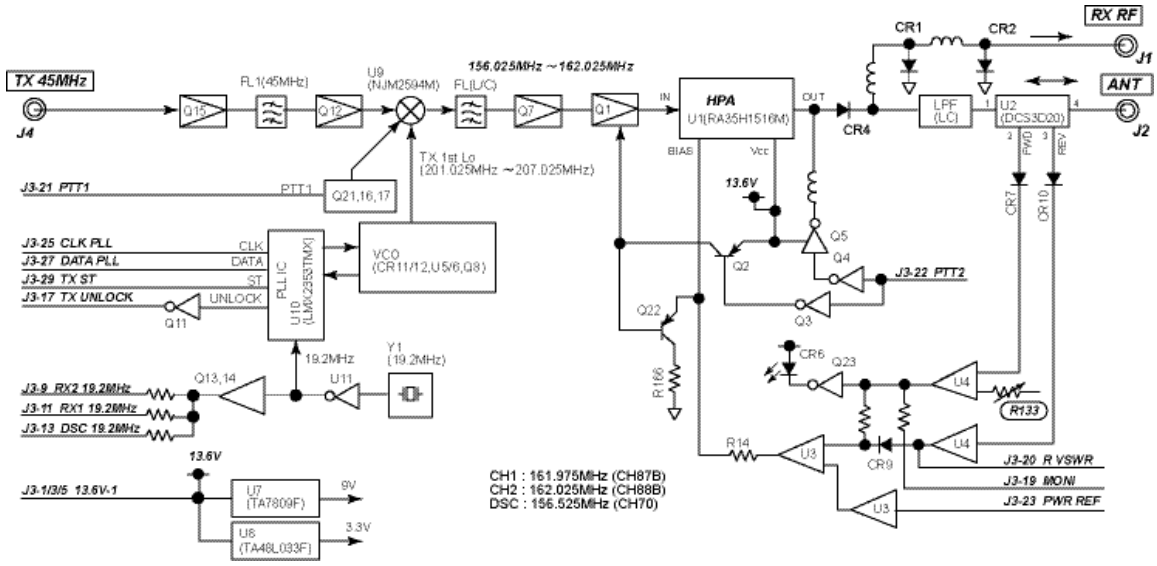


Figure 5.3.2 Block Diagram of TX Board

TX 45 MHz modulated signal coming from the MAIN Board is input to U9 via Q15, FL1 and Q12. FL1 is the BPF (Passband width: ±10 kHz), and reducing the spurious components included in the TX modulated signal.

At U9 TX 45 MHz modulated signal is mixed with the 1st Local oscillation frequency of 201.025 MHz to 207.025 MHz, and then converted to the transmitting frequency of 156.025 MHz to 162.025 MHz. Next stage FL1 is the BPF with the L/C circuits, reducing the spurious components generated by the frequency conversion.

U1 is of HPA module (Gain: 30 dB or more) and holds TX Power output of 12.5 W.

The output of HPA is of the spurious components attenuated by an LPF made of L/C circuits, and is delivered to the VHF ANT terminal via U2: CM Coupler.

Y1 is the 19.2 MHz reference oscillator for the PLL circuits of TX Board, and has an accuracy of ±1 ppm, maintaining the VHF transmitting frequency tolerance within ±500 Hz.

Main Control and Detection signals

R VSWR

Detects the reflected (reverse) wave voltage (REV) from U2.

Activates to transmit the error message “ANT” for announcing the abnormality of the VHF ANT circuits when VSWR reaches 3 or above.

MONI

Detects the forward wave voltage (FWD) from U2.

Activates to transmit the error message “TX” for announcing the TX abnormality when no detecting the voltage during TX operation. The LED CR6 goes on during TX operation.

PWR REF

For setting up the TX Power output to 0, 1, 2 or 12.5 W. The level setting of TX Power output is done by controlling the “BIAS” level of the HPA by using “FWD” signal from U2 and “PWR REF” signal.

TX Power is set to 12.5 W by adjusting the Potentiometer R133 when TX Power selection of 12.5 W is made.

PTT1, PTT2

PTT1 signal controls U9, and PTT2 controls the HPA peripheral circuits. Both are the control signals for switching TX/RX and have the same control timing.

TX UNLOCK

Activates to transmit the error message “TX” for announcing the TX abnormality when the TX PLL circuits operation becomes unlocked.

Distribution of 19.2 MHz Reference Oscillation frequency of Y1

19.2 MHz Reference Oscillation frequency of Y1 in TX Board is distributed to RX1 and RX2 Boards as the reference of the PLL circuits, and to DSC Board as the reference to generate 2nd Local Oscillation.

Frequency adjustment is not necessary for Y1.

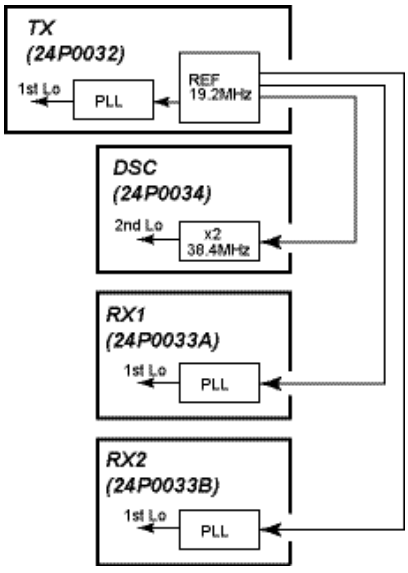


Figure 5.3.3 Distribution of 19.2 MHz reference oscillation frequency

5.3.2 RX-1 Board (24P0033A) and RX-2 Board (24P0033B)

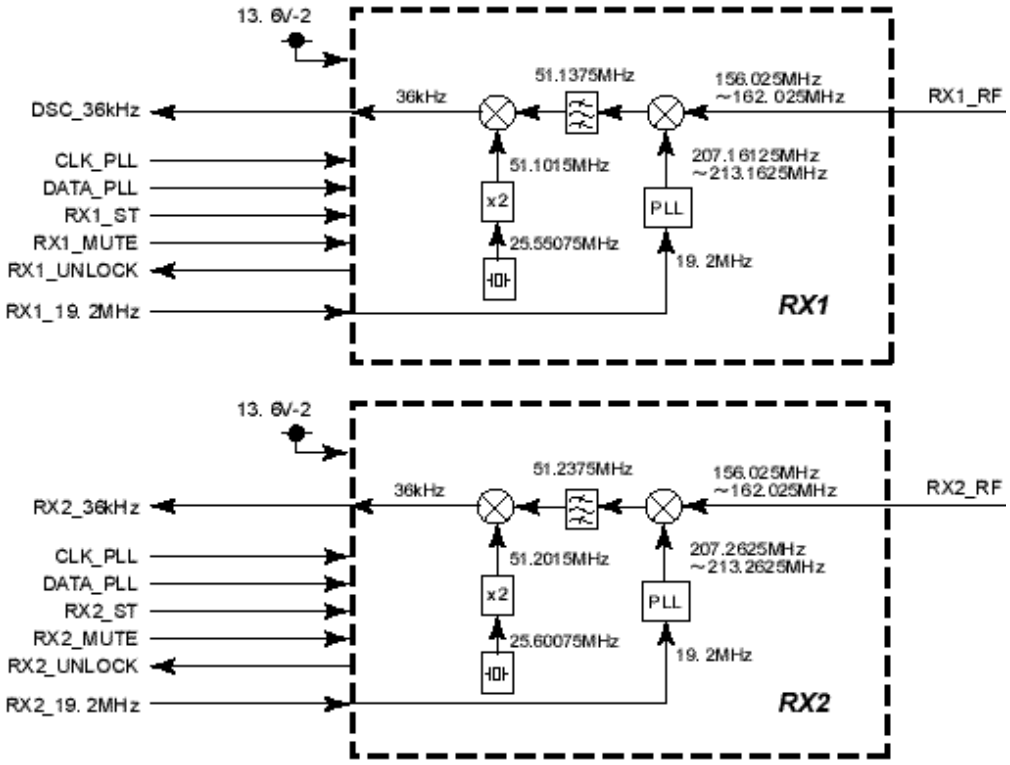


Figure 5.3.4 Outline of RX1 and RX2 Boards

This board converts AIS receiving signal (TDMA) to 36 kHz IF signal. RX1 and RX2 circuits are almost same except for the 1st IF frequency and the 2nd Local oscillation frequency. Receiving frequencies of CH-A are allocated for RX1 Board and CH-B for RX2 Board.

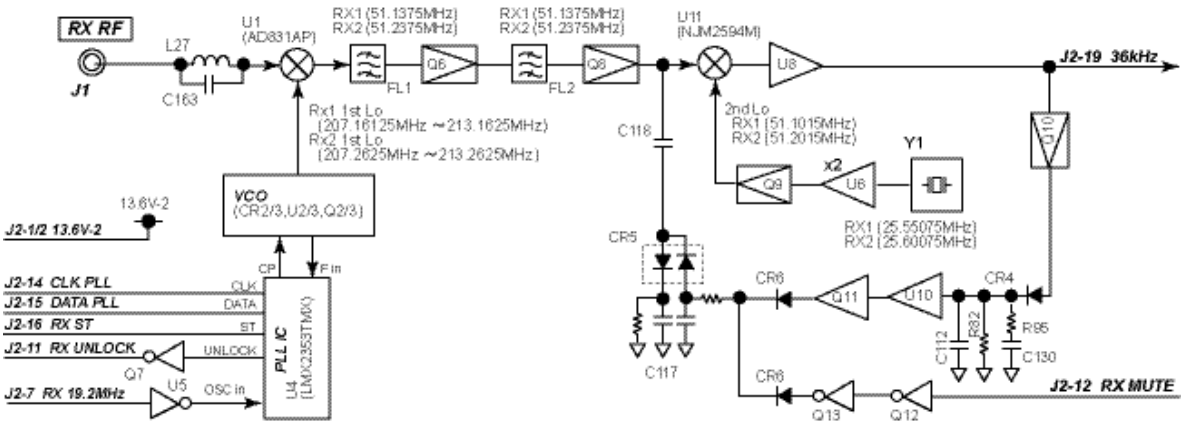


Figure 5.3.5 Block Diagram of RX1 and RX2 Boards

AIS Receiving Signal is fed to U1 via L27 and C163 composing the 200 MHz band-trap filter for eliminating the leakage of the 1st local frequency components toward the “RX RF” terminal.
At U1, 150 MHz band AIS Receiving Signal is mixed with the 1st local frequency of 201 MHz to 213 MHz, and converted to 51 MHz 1st IF signal.
Next stage, FL1 is the BPF (Passband width: ±4.5 kHz), and FL2 is also the BPF (Passband width: ±10 kHz) and reducing the spurious components generated by the frequency conversion.
Y1 is the 25.55075 MHz for RX1 (25.60075 MHz for RX2) reference oscillator, and has an accuracy of ±2.5 ppm.

Y1 output frequency is converted to the 2nd Local oscillation frequency of 51.1015 MHz for RX1 (51.2015 MHz for RX2) by the frequency doubler U6.
At U11 the 51 MHz 1st IF signal is mixed with the 2nd Local frequency and converted to 36 kHz signal fed to MAIN Board. Antenna Input signal of 50 Ω/-107 dBm corresponds to the 36 kHz signal of 600Ω/+60 dBμV.
Q10, CR4, U10 and Q11 compose the AGC circuits. Input signal level fed to U11 is controlled by the CR5 PIN diode operation which is controlled by the AGC output voltage.
AGC operation is activated for the Antenna Input level of -50 dBm or more.

Main Control and Detection signals

RX UNLOCK

Activates to transmit the error message “CH1” and/or “CH2” for announcing the RX abnormality when the RX PLL circuits operation becomes unlocked.

RX MUTE

Not used.

5.3.3 DSC Board (24P0034)

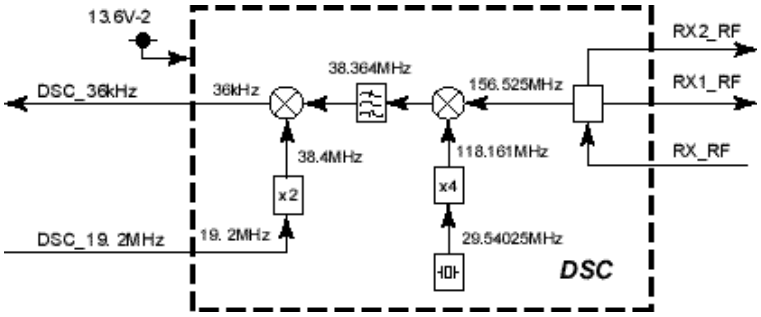


Figure 5.3.6 Outline of DSC Board

CH70 DSC Receiving signal of 156.525 MHz is converted to 36 kHz IF signal.

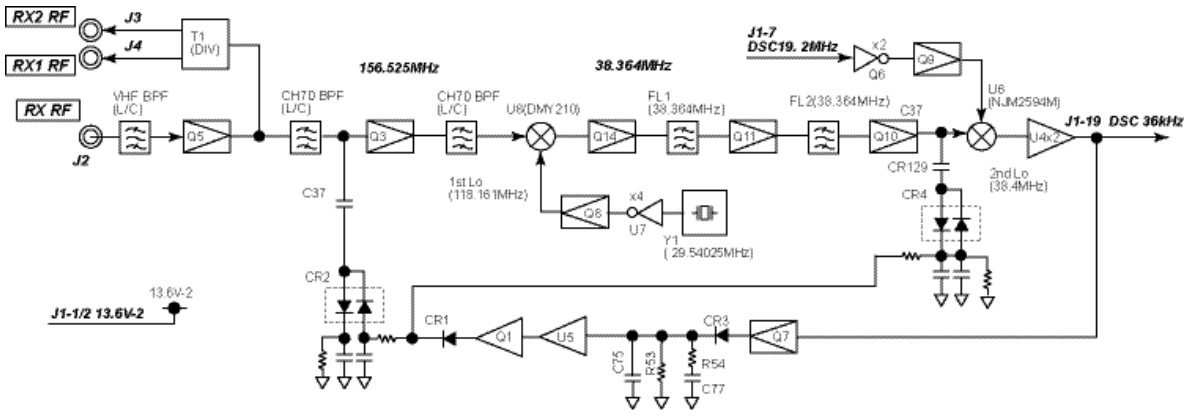


Figure 5.3.7 Block Diagram of DSC Board

CH70 DSC Receiving signal is input to VHF band BPF with the L/C circuits, Q5 and then T1 for distributing the signal to RX1 and RX2 Boards. Q5 is a 6 dB amplifier that compensates the distribution loss of T1.
And also Q5 output signal is fed to U8 via CH70 BPF with L/C circuits and Q8.
Y1 is 29.54025 MHz oscillator having an accuracy of ± 2.5 ppm.
At U7 the oscillated output frequency is multiplied by 4 into the 1st local oscillation frequency of 118.161 MHz.
At U8 CH70 DSC receiving signal is mixed with the 1st local frequency and converted to 38.364 MHz 1st IF signal.
FL1 and FL2 are the BPFs (Passband width: ± 10 kHz) reducing the spurious components generated by the frequency conversion.

DSC 19.2 MHz Signal from TX Board is converted to the 2nd Local oscillation frequency of 38.4 MHz by the frequency doubler Q6.

At U6 the 1st IF signal is mixed with the 2nd Local oscillation frequency and converted to 36 kHz signal fed to MAIN Board. Antenna input signal of 50 Ω/-107 dBm corresponds to the 36 kHz signal of 600 Ω/+60 dBμV.

Q7, CR3, U5 and Q1 compose the AGC circuits having 2 lines controlling for RF and IF circuits. For RF circuits, Input signal level to Q3 is controlled by the CR2 PIN diode operation which is controlled by the AGC output voltage.
For IF circuits, Input signal level to U6 is also controlled by the CR4 PIN diode.
AGC operation is activated for the Antenna Input level of -50 dBm or more.

5.3.4 MAIN Board (26P0035)

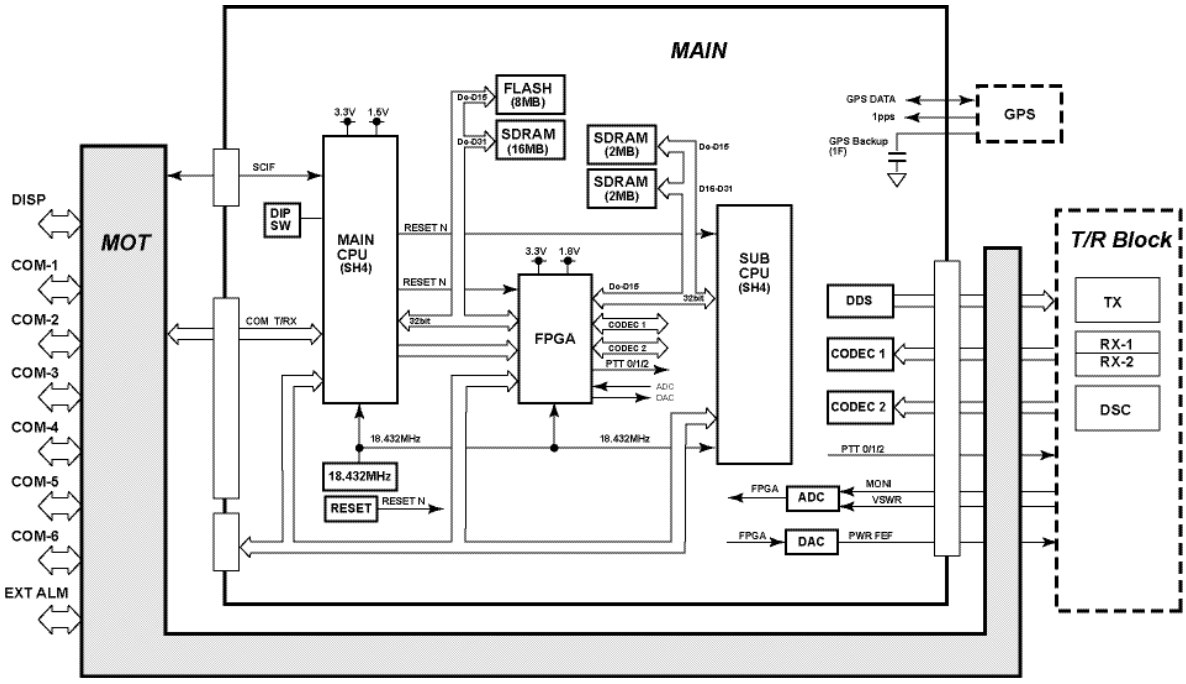


Figure 5.3.8 Block Diagram of MAIN Board

This board contains MAIN CPU, SUB CPU and peripheral circuits. Main functions are as follows:

MAIN CPU

For controlling and processing of AIS (DSC) communications system and I/O interfacing.

SUB CPU

For the TDMA/DSC signal processing and the analog-interfacing with the radio parts.

FPGA

For the asynchronous serial communication with the external equipment, the timing control of the AIS(TDMA) communications, the TDMA slot forming, and interfacing with the CODEC I/O, DDS Output, MAIN CPU and SUB CPU.

DDS

45 MHz GMSK modulated signal of AIS (TDMA) or FM modulated signal (DSC) generated by SUB CPU are fed to TX Board by using DDS.

CODEC 1

36 kHz AIS(TDMA) receiving signals are input from RX1 and RX2 Boards, AD-converted, fed to SUB CPU via FPGA, and demodulated.

CODEC 2

36 kHz DSC receiving signal is input from DSC Board, AD-converted, fed to SUB CPU via FPGA, and demodulated.

5.3.5 MOT Board (24P0036)

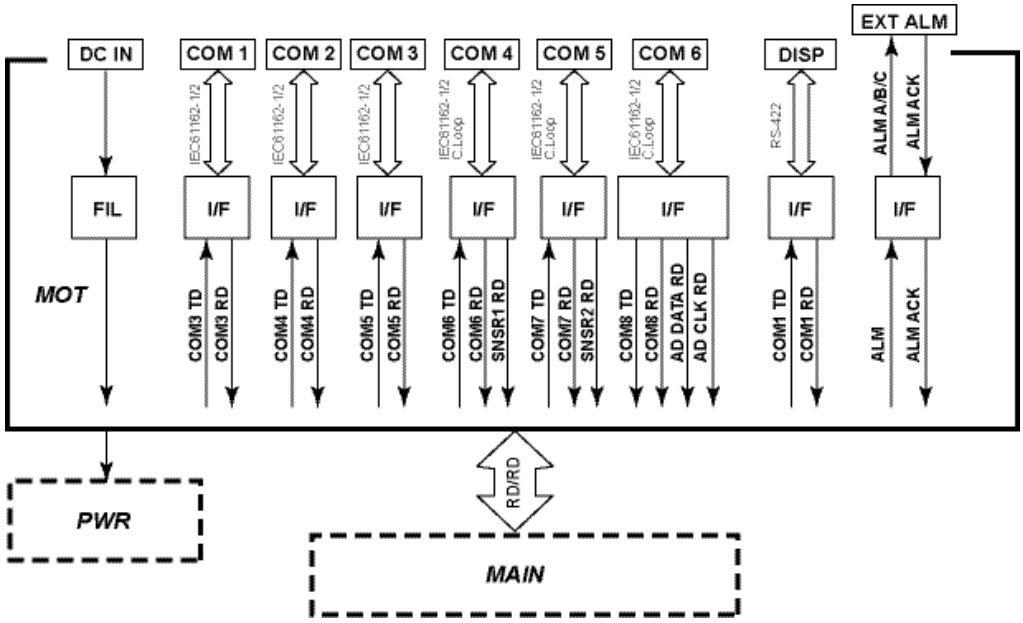


Figure 5.3.9 Block Diagram of MOT Board

The following figure shows the I/F of COM1 Port. The I/F of other ports consists of the same circuits. For example, the I/O circuits of COM1 Port are electrically separated by U2 for complying with the Standard IEC 61162-2 and for communicating with the external equipment.

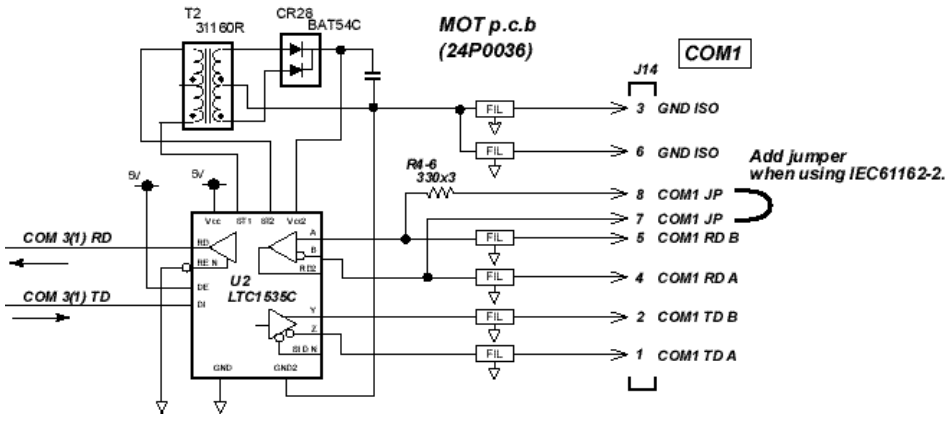


Figure 5.3.10 I/F of COM1 Port